Keysight U7232D DisplayPort Electrical Performance Compliance Test Application

Methods of Implementation

KEYSIGHT TECHNOLOGIES

Notices

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Keysight Technologies, Inc.
1900 Garden of the Gods Road
Colorado Springs, CO 80907 USA

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DisplayPort Automated Testing—At A Glance

The Keysight U7232D DisplayPort Electrical Performance Compliance Test Application helps you verify compliance of the DisplayPort devices to DisplayPort specifications using Keysight Infiniium Digital Storage Oscilloscopes with bandwidths of 13 GHz or higher. The DisplayPort Electrical Performance Compliance Test Application:

- Lets you select individual or multiple tests to run.
- Lets you identify the device being tested and its configuration.
- Shows you how to make oscilloscope connections to the device under test.
- Automatically checks for proper oscilloscope configuration.
- Automatically sets up the oscilloscope for each test.
- Provides detailed information for each test that has been run and lets you specify the thresholds at which marginal or critical warnings appear.
- Creates a printable HTML report of the tests that have been run.

NOTE

The tests performed by the DisplayPort Electrical Performance Compliance Test Application are intended to provide a quick check of the electrical health of the DUT. This testing is not a replacement for an exhaustive test validation plan.

You may refer to the following specification documents for compliance testing measurements. For more information, see the VESA web site at www.vesa.org.

Test Specification	Reference Documents
DisplayPort 1.3 (1.3)	VESA DisplayPort (DP) Standard Version 1.3, September 17, 2014
DisplayPort 1.2 (1.2b)	VESA DisplayPort Standard Version 1, Revision 2a, May 23, 2012 VESA DisplayPort PHY Compliance Test Specification Version 1.2b, November 26, 2012
Mobility DisplayPort 1.0 (MyDP)	VESA Mobility DisplayPort (MyDP) Standard Version 1, May 21, 2012 VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, April 26, 2013
SlimPort (MyDP HBR25)	SlimPort Compliance Test Specification Version 1, February 28, 2014

Required Equipment and Software

In order to run the DisplayPort automated tests, you need the following equipment and software:

- Infiniium 90000A Series/90000X Series/90000Q Series/V-Series/Z-Series Digital Storage Oscilloscopes with a bandwidth of 13GHz or higher.
- The minimum version of Infiniium Oscilloscope Software (see the U7232D DisplayPort Compliance Test Application Release Notes).
- U7232D DisplayPort Electrical Performance Compliance Test Application.
- Keyboard, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- Mouse, qty = 1, (provided with the Keysight Infiniium oscilloscope).
- U7232D DisplayPort Electrical Performance Compliance Test Application license.
- N5461B Serial Data Equalization software license (for DisplayPort 1.3 Test Specification only).
- N5465A InfiniiSim Waveform Transformation Toolset license (for DisplayPort 1.3 Test Specification only).

In order to run the automated tests on DisplayPort DUTs, you need the following fixtures and accessories:

- DisplayPort Test Point Adapter:

For DUT Type	Required Fixtures/Accessories (Recommended)	Quantity	Recommended Oscilloscope
Source	For DisplayPort Type-C Connector ▪ N7015A Type-C High-Speed Test Fixture For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P*	1 (each)	Infiniium Series
Sink or Cable	For DisplayPort Connector ▪ Wilder technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Receptacle (mDP-TPA-R)** For MyDP Connector ▪ Wilder Technologies (MYDP-TPA-R*)		

* All Wilder Technologies Test Point Adapters require the Wilder Technologies DP-TPA-A Aux Control Board.

** All Luxshare ICT Test Point Adapters require the Luxshare ICT DP-TPA-A AUX Control Board.

- InfiniiMax Series Probe Amplifiers with minimum 12GHz bandwidth:

Required Fixtures/Accessories (Recommended)	Quantity	Recommended Oscilloscope
▪ 1169A 12GHz InfiniiMax II Series Probe Amplifier ▪ N2832A 13GHz InfiniiMax III+ Series Probe Amplifier ▪ N2800A 16GHz InfiniiMax III Series Probe Amplifier	4	Infiniium Series

- InfiniiMax Series Probe Head with minimum 12GHz bandwidth:

Test Type	Required Fixtures/Accessories (Recommended)	Quantity	Recommended Oscilloscope
Physical Layer Tests	▪ N5380A InfiniiMax II 12GHz Differential SMA Adapter ▪ N5444A InfiniiMax III 28GHz SMA Probe Head	4	Infiniium Series
AUX Channel Tests	▪ E2677A InfiniiMax 12GHz Differential Solder-In Probe Head ▪ E2678A/B InfiniiMax 12GHz Single-Ended/Differential Probe Head & Accessories	1	

- Other Equipment (required for Internal/Self Calibration of the Infiniium Oscilloscope):

Required Fixtures/Accessories (Recommended)	Quantity	Recommended Oscilloscope/Description
BNC to SMA (male) Converter	4	Infiniium 90000A Series
SMA (male) to SMA (male) Converter	4	Infiniium 90000X Series/90000Q Series/V-Series/Z-Series
E2655A/B/C Probe De-Skew and Performance Verification Kit	1	Infiniium Series
Calibration Cable	1	Infiniium Series
80 Ω Damping Resistors (01130-81506)	1	To be used with Socketed Differential Probe Head

- Automation Controllers (Optional):

Testing Type	Supported Fixtures/Accessories (Optional)	Quantity	Recommended Oscilloscope
For Source DUT Testing	Unigraf DPR-100 Compact Sized DisplayPort Reference Sink	1 (each)	Infiniium Series
For Sink DUT Testing	Unigraf DPT-200 Compact Sized DisplayPort Reference Source		

In This Book

This manual describes the tests that are performed by the DisplayPort Electrical Performance Compliance Test Application in more detail; it contains information from (and refers to) various DisplayPort specifications and it describes how the tests are performed.

- Chapter 1, “Installing the DisplayPort Electrical Performance Compliance Test Application” shows how to install and license the automated test application (if it was purchased separately).
- Chapter 2, “Preparing to Take Measurements” shows how to start the DisplayPort Electrical Performance Compliance Test Application and gives a brief overview of how it is used.
- Chapter 3, “DisplayPort 1.2 Source Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.2 source devices.
- Chapter 4, “DisplayPort 1.2 Sink Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.2 sink devices.
- Chapter 5, “DisplayPort 1.2 Cable Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.2 cable devices.
- Chapter 6, “DisplayPort 1.2 AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of DisplayPort 1.2 source and sink devices.
- Chapter 7, “DisplayPort 1.2 Inrush Tests” describes the normative and informative inrush tests for compliance verification of DisplayPort 1.2 source and sink devices as a power consumer.
- Chapter 8, “DisplayPort 1.2 Dual Mode Tests” describes the normative and informative Dual Mode physical layer tests for compliance verification of DisplayPort 1.2 source devices.
- Chapter 9, “DisplayPort 1.3 Source Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.3 source devices.
- Chapter 10, “DisplayPort 1.3 Sink Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.3 sink devices.
- Chapter 11, “DisplayPort 1.3 Cable Tests” describes the normative and informative tests for compliance verification of DisplayPort 1.3 cable devices.
- Chapter 12, “DisplayPort 1.3 AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of DisplayPort 1.3 source and sink devices.
- Chapter 13, “DisplayPort 1.3 Inrush Tests” describes the normative and informative inrush tests for compliance verification of DisplayPort 1.3 source and sink devices as a power consumer.
- Chapter 14, “DisplayPort 1.3 Dual Mode Tests” describes the normative and informative Dual Mode physical layer tests for compliance verification of DisplayPort 1.3 source devices.
- Chapter 15, “MyDP 1.0 Source Tests” describes the normative and informative tests for compliance verification of MyDP 1.0 source devices.
- Chapter 16, “MyDP 1.0 Sink Tests” describes the normative and informative tests for compliance verification of MyDP 1.0 sink devices.
- Chapter 17, “MyDP 1.0 Cable Tests” describes the normative and informative tests for compliance verification of MyDP 1.0 cable devices.
- Chapter 18, “MyDP 1.0 AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of MyDP 1.0 source and sink devices.
- Chapter 19, “MyDP 1.0 Inrush Tests” describes the normative and informative inrush tests for compliance verification of MyDP 1.0 source and sink devices as a power consumer.
- Chapter 20, “SlimPort Source Tests” describes the normative and informative tests for compliance verification of SlimPort source devices.
- Chapter 21, “SlimPort Sink Tests” describes the normative and informative tests for compliance verification of SlimPort sink devices.
- Chapter 22, “SlimPort Cable Tests” describes the normative and informative tests for compliance verification of SlimPort cable devices.

- Chapter 23, “SlimPort AUX Channel Tests” describes the normative and informative AUX channel physical layer tests for compliance verification of SlimPort source and sink devices.
- Chapter 24, “SlimPort Inrush Tests” describes the normative and informative inrush tests for compliance verification of SlimPort source and sink devices as a power consumer.
- Chapter 25, “Calibrating the Infiniium Oscilloscope” describes how to calibrate the oscilloscope in preparation for running the DisplayPort automated tests.
- Chapter 26, “InfiniiMax Probing” describes the 1168A/1169A probe amplifier and probe head recommendations for DisplayPort testing.
- Appendix A, “DisplayPort AUX Channel Cookbook for Tx Automated Test” provides a guide on how to implement the test automation features architected in the *DisplayPort Specification 1.1a* using a sink emulator such as the Keysight W2642 DPTC controller.

See Also

- The DisplayPort Electrical Performance Compliance Test Application's Online Help, which describes:
  - Starting the DisplayPort Compliance Test Application
  - Creating or Opening a Test Project
  - Compliance Limits
  - Setting Up the Precision Probe/Cable
  - Setting Up Switch Matrix
  - Setting Up the Test Environment
  - Selecting Tests
  - Configuring Tests
  - Connecting the Oscilloscope to the DUT
  - Running Tests
  - Automating the Application
  - Viewing Results
  - Viewing/Exporting/Printing the Report
  - Understanding the Report
  - Saving Test Projects
  - User Defined Add-Ins
  - Controlling the Application via a Remote PC
  - Using a Second Monitor

- DisplayPort References:

Test Specification	Reference Documents
DisplayPort 1.3 (1.3)	VESA DisplayPort (DP) Standard Version 1.3, September 17, 2014
DisplayPort 1.2 (1.2b)	VESA DisplayPort Standard Version 1, Revision 2a, May 23, 2012 VESA DisplayPort PHY Compliance Test Specification Version 1.2b, November 26, 2012
Mobility DisplayPort (MyDP 1.0)	VESA Mobility DisplayPort (MyDP) Standard Version 1, May 21, 2012 VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, April 8, 2013
SlimPort (MyDP HBR25)	SlimPort Compliance Test Specification Version 1, February 28, 2014

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23 SlimPort AUX Channel Tests

1 Installing the DisplayPort Electrical Performance Compliance Test Application

If you purchased the U7232D DisplayPort Electrical Performance Compliance Test Application, you need to install the software and license key.

Installing the Software

1 Make sure you have the minimum version of Infiniium oscilloscope software (see the U7232D test application release notes) by choosing **Help>About Infiniium...** from the main menu.

2 To obtain the DisplayPort Electrical Performance Compliance Test Application, go to Keysight website: http://www.keysight.com/find/scope-apps-sw.

Figure 1 Keysight website for software Downloads

3 Search the list on this web page for the link to the U7232D DisplayPort Electrical Performance Compliance Test Application. Click the appropriate link and follow the instructions to download and install the application.

Installing the License Key

1 Request a license code from Keysight by following the instructions on the Entitlement Certificate.
You will need the oscilloscope's "Option ID Number", which you can find in the **Help>About Infiniium...** dialog box.
2 After you receive your license code from Keysight, choose **Utilities>Install Legacy Licenses....**
3 In the Install Option License dialog, enter your license code and click **Install License**.
4 Click **OK** in the dialog that tells you to restart the Infiniium oscilloscope application software to complete the license installation.
5 Click **Close** to close the Install Option License dialog.
6 Choose **File>Exit.**
7 Restart the Infiniium oscilloscope application to complete the license installation.

2 Preparing to Take Measurements

Before running the DisplayPort automated tests, you must acquire the appropriate test fixtures, and you should calibrate the oscilloscope and probe. After the oscilloscope and probe have been calibrated, you are ready to start the DisplayPort Electrical Performance Compliance Test Application and perform the measurements.

Calibrating the Oscilloscope

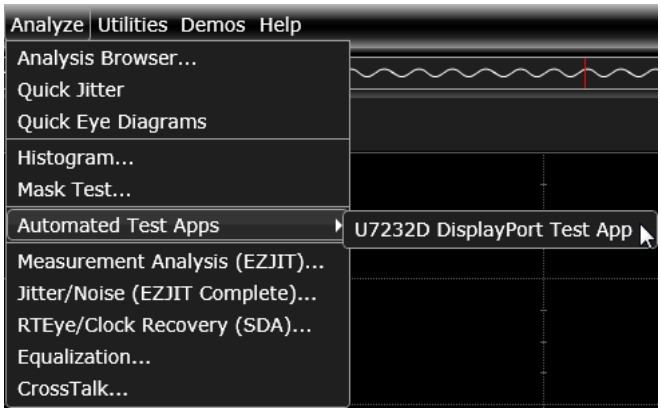
If you haven't already calibrated the oscilloscope and probe, see Chapter 25, "Calibrating the Infiniium Oscilloscope.

NOTE If the ambient temperature changes more than 5 degrees Celsius from the calibration temperature, internal calibration should be performed again. The delta between the calibration temperature and the present operating temperature is shown in the **Utilities>Calibration** menu.

NOTE If you switch cables between channels or other oscilloscopes, it is necessary to perform cable and probe calibration again. Keysight recommends that, once calibration is performed, you label the cables with the channel on which they were calibrated.

Starting the DisplayPort Electrical Performance Compliance Test Application

1 From the Infiniium oscilloscope's main menu, choose **Analyze>Automated Test Apps>U7232D DisplayPort Test App**.



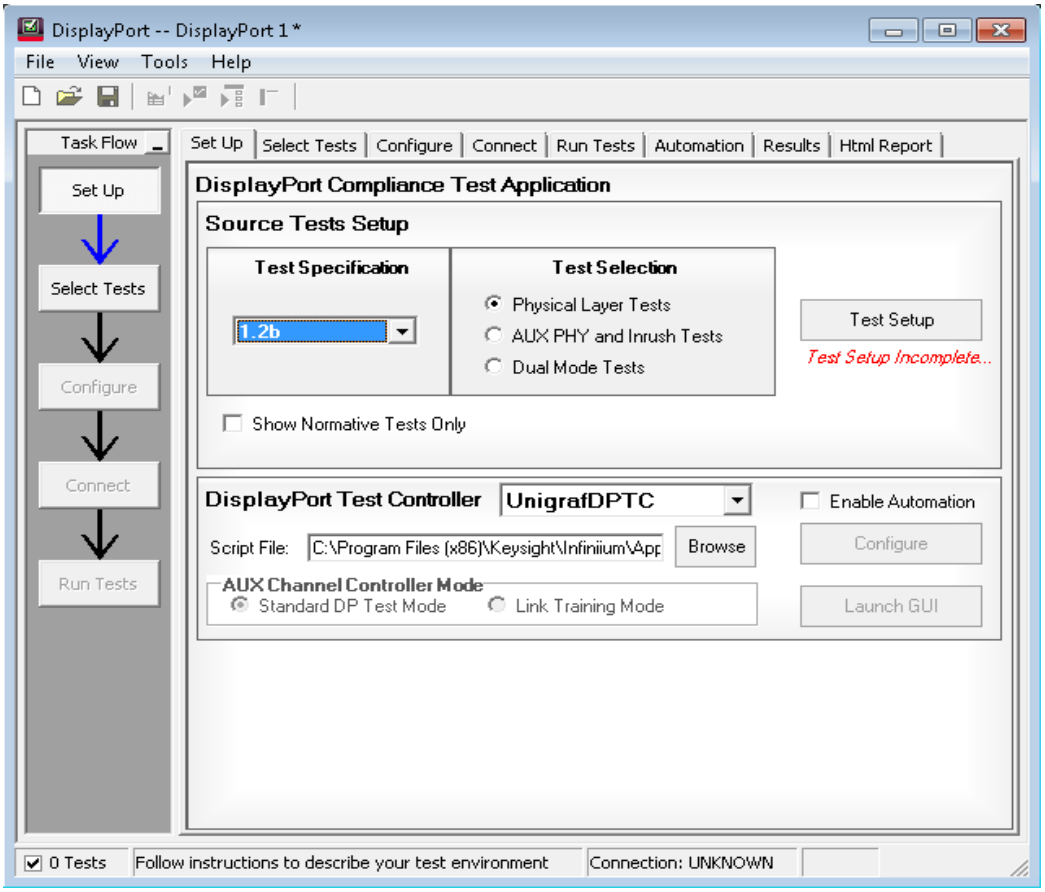


Figure 2 The DisplayPort Electrical Performance Compliance Test Application

NOTE

If DisplayPort Test does not appear in the Automated Test Apps menu, the DisplayPort Electrical Performance Compliance Test Application has not been installed (see Chapter 1, "Installing the DisplayPort Electrical Performance Compliance Test Application).

Figure 2 shows the DisplayPort Electrical Performance Compliance Test Application main window. The task flow pane, and the tabs in the main pane, show the steps you take in running the automated tests:

Tab	Description
Set Up	Lets you select your setup options. Allows you to setup by device type, test type, fixture type and connection type.
Select Tests	Lets you select the tests you want to run. The tests are organized hierarchically, so you can select all tests in a group. After tests are run, status indicators show which tests have passed, failed, or not been run, and there are indicators for the test groups.
Configure	Lets you enter information about the device being tested and configure test parameters (like memory depth). This information appears in the HTML report.
Connect	Shows you how to connect the oscilloscope to the device under test for the tests to be run.
Run Tests	Starts the automated tests. If the connections to the device under test need to be changed while multiple tests are running, the tests pause, show you how to change the connection, and wait for you to confirm that the connections have been changed before continuing.
Automation	Enables construction of automated script of commands that drive the functionality of the test application.
Results	Contains more detailed information about the tests that have been run. You can change the thresholds at which marginal or critical warnings appear.
HTML Report	Shows a compliance test report that can be printed.

Online Help Topics

For information on using the DisplayPort Electrical Performance Compliance Test Application, see the Online Help (which you can access by choosing **Help>Contents...** from the application's main menu).

The DisplayPort Electrical Performance Compliance Test Application's Online Help describes:

- Starting the DisplayPort Compliance Test Application
  - To view/minimize the task flow pane
  - To view/hide the toolbar
- Creating or Opening a Test Project
  - To set load preferences
- Compliance Limits
  - To Activate/Refresh Limit Set
  - To Create/Edit Limit Set
- Setting Up the Precision Probe/Cable
- Setting Up Switch Matrix
- Setting Up the Test Environment
  - Test Setup
  - DisplayPort Test Controller
- Selecting Tests
- Configuring Tests
- Connecting the Oscilloscope to the DUT
- Running Tests
  - To select the Store Mode
  - To run multiple times
  - To send email on pauses or stops
  - To pause or stop on events
  - To specify the event
  - To set the display preferences
  - To set the run preferences
- Automating the Application
- Viewing Results
  - To delete trials from the results
  - To show reference images and flash mask hits
  - To change margin thresholds
  - To change the test display order
  - To set trial display preferences
- Viewing/Exporting/Printing the Report
  - To export the report
  - To print the report
  - To set HTML Report preferences
- Understanding the Report
- Saving Test Projects
  - To set AutoRecovery preferences

- User Defined Add-Ins
  - To install an add-in
  - To remove an add-in
- Controlling the Application via a Remote PC
  - To check for the App Remote license
  - To identify the remote interface version
  - To enable the remote interface
  - To enable remote interface hints
- Using a Second Monitor

3 DisplayPort 1.2 Source Tests

This section provides the guidelines for source eye diagram differential tests using a Keysight 13 GHz or greater Infiniium oscilloscope, 1168A or 1169A probes, and the DisplayPort Electrical Performance Compliance Test Application.

Overview

This section describes the normative and informative main link physical layer tests for compliance verification of DisplayPort 1.2 source, sink and cable devices.

Test Point Definition for DisplayPort 1.2 (1.2b) Tests

Five different test points are identified for the physical layer measurement. See Figure 3

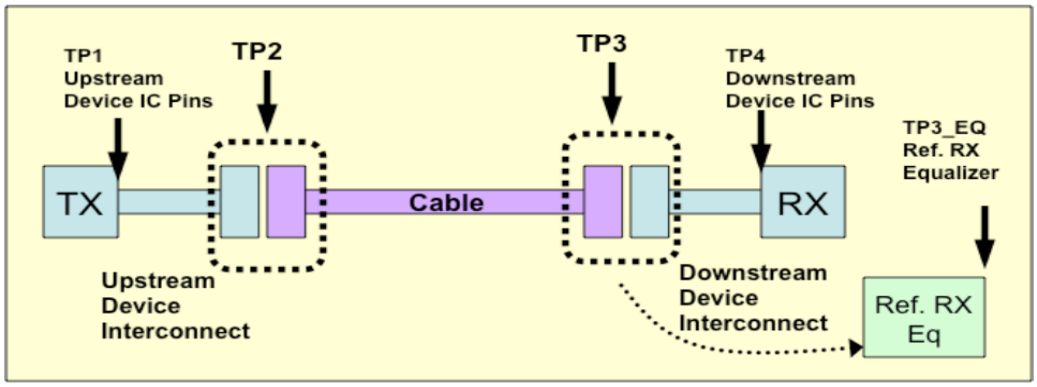


Figure 3 Test Points in a DisplayPort InterConnect System

Table 1 defines the Test Points used for various DisplayPort 1.2 Tests:

Table 1 Test Points for DisplayPort Tests

Test Point	Description
TP1	At the pins of the Transmitter Device
TP2	At the test interface on a test access fixture as close as possible to the DP mated connection to a Source device
TP3	At the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device
TP3_EQ	At TP3, when a defined cable model with equalizer is applied. There are two defined cable models: ▪ Worst Cable Model as defined in VESA DisplayPort 1.2a Standard, ▪ Zero length, zero loss cable. The equalizer is also defined in VESA DisplayPort 1.2a Standard
TP4	At the pins of a receiving device

Cable Models

The two cable models defined in VESA DisplayPort 1.2a Standard are:

1 Worst Case Cable Model—To achieve the TP3_EQ signal with the worst case cable model:

- Acquire the signal at TP2.
- Embed the TP2 signal with a “worst case” HBR cable model using an InfiniiSim Waveform Transformation Toolset software to emulate the insertion loss as defined in Figure 4-10 of the VESA DisplayPort 1.2a Standard.
  - For the DisplayPort Compliance Test Application, the “*CIC_rev0p6.s4p*” cable model transfer function is used.

- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

2 Zero Length Cable Model—To achieve the TP3_EQ signal with the zero length cable model:

- Acquire the signal at TP2.
- No cable model is embedded for the Zero Length cable model.
- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

Equalization

When equalization is required, use the CTLE (Continuous Time Linear Equalization) transfer function, as given in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

For main link, use the CTLE model with the following transfer function for HBR (2.7 Gbps):

The HBR Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2} \cdot \sqrt{\omega^2 + \omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.725 \times 10^9)$$
$$\omega_{p1} = 2\pi(1.35 \times 10^9)$$
$$\omega_{p2} = 2\pi(2.5 \times 10^9)$$

Figure 4 Transfer Function of the CTLE model for HBR

Table 2 CTLE Model for HBR

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.725 GHz	0.725 GHz
Pole 1 Frequency	1.35 GHz	1.35 GHz
Pole 2 Frequency	2.5 GHz	2.5 GHz

For main link, use the CTLE model with the following transfer function for HBR2 (5.4 Gbps):

The HBR2 Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 5 Transfer Function of the CTLE model for HBR2

Table 3 CTLE Model for HBR2

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.64 GHz	0.64 GHz
Pole 1 Frequency	2.7 GHz	2.7 GHz
Pole 2 Frequency	4.5 GHz	4.5 GHz
Pole 3 Frequency	13.5 GHz	13.5 GHz

Clock Recovery

When Clock Recovery is required, the clock recovery technique follows the definition of the receiver PLL as defined in Section 3.5.3.5 of the VESA DisplayPort 1.2a Standard. For main link, use the second-order clock recovery function with a closed loop tracking bandwidth and damping factor, with respect to the PRBS7 pattern, as shown in Table 4:

Table 4 Main Link Second-Order Clock Recovery Function

Bit Rate	Bandwidth	Damping Factor
HBR2 (5.4 Gbps)	10 MHz	1.00
HBR (2.7 Gbps)	10 MHz	1.51
RBR (1.62 Gbps)	5.4 MHz	1.51

Test Point Definition for DisplayPort 1.2 (1.2b) Source Tests

Test the Source DUT at Test Point 2 (TP2) as shown in Figure 6. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

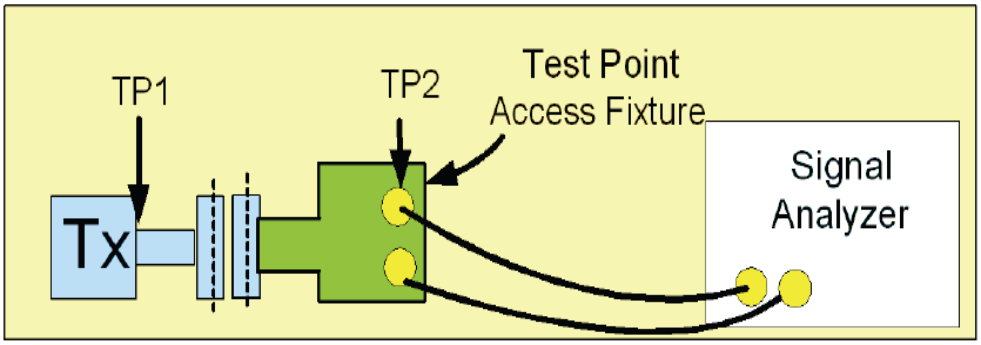


Figure 6 Test Point 2 Connection for DisplayPort 1.2 Source Tests

Table 5 defines the test point fixtures and instruments used for DisplayPort 1.2 (1.2b) Source Tests:

Table 5 Test Point Fixtures and Instruments for DisplayPort 1.2 Source Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 7)

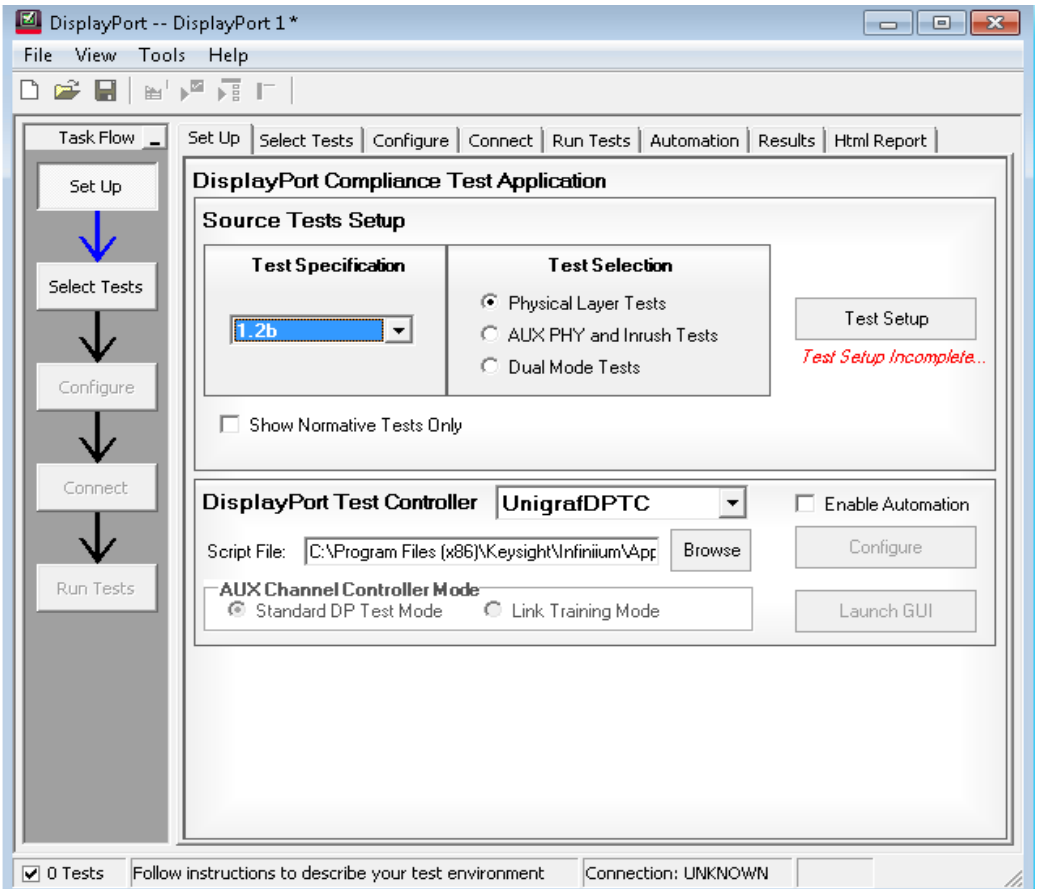


Figure 7 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.2b Standards, select **1.2b** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.2 Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

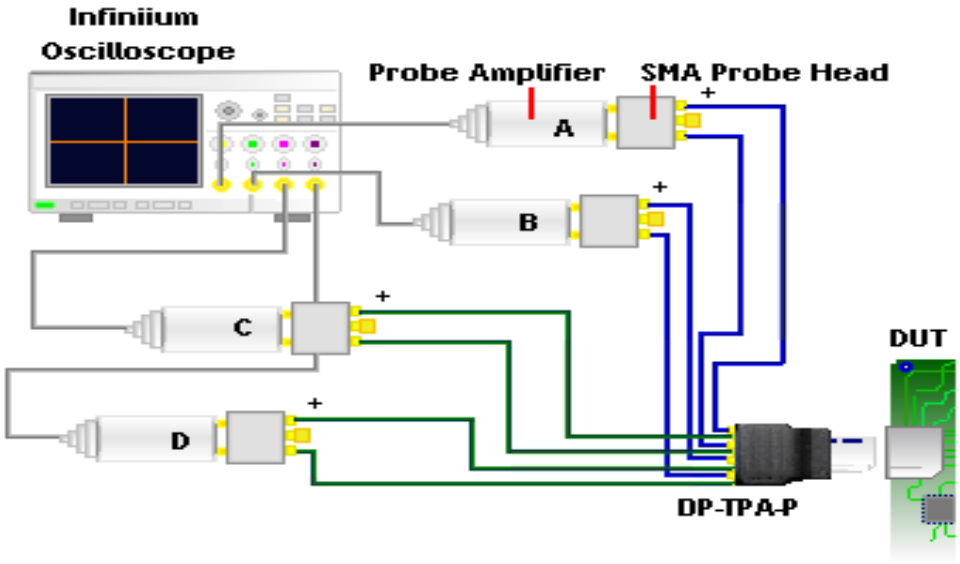


Figure 8 Sample connection diagram for DisplayPort 1.2 Source Tests

Source Eye Diagram Test

Test ID

1210001, 1210002, 1210003, 1210004 – Eye Diagram Test

Test Overview

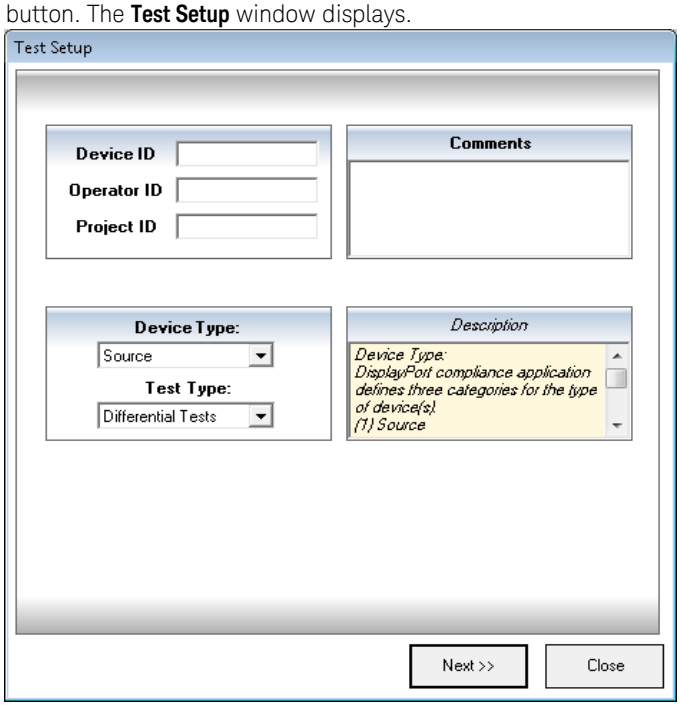
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
Spread Spectrum Clocking	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Swing	Level 2
Pre-Emphasis Level	Level 0
Post Cursor2 Level	Level 0
Lane Setting	All test lanes supported
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



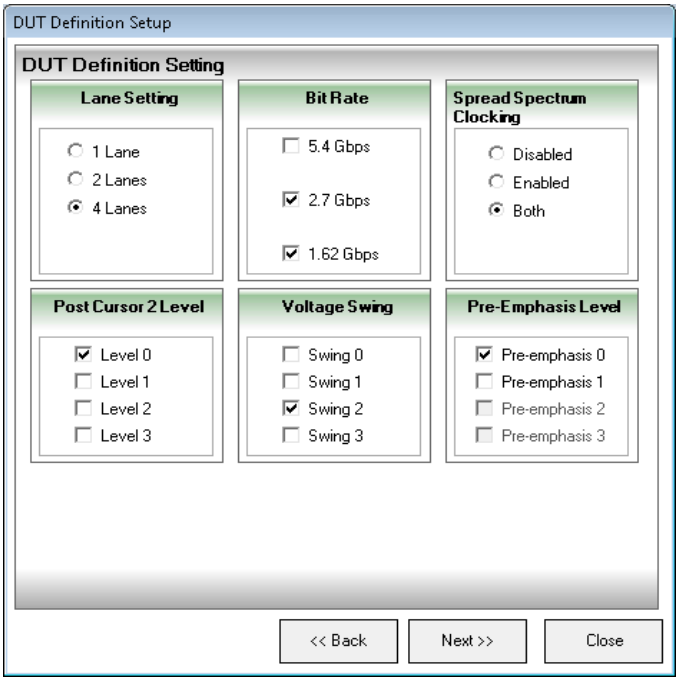
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

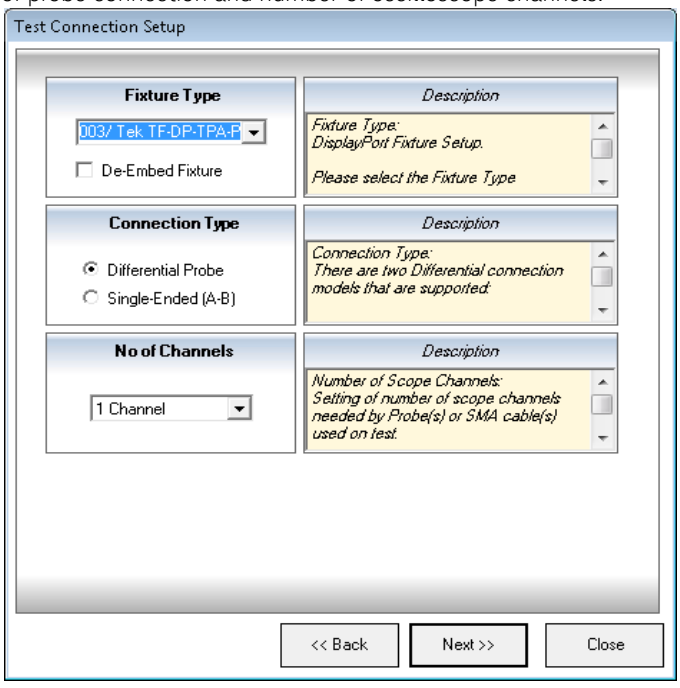
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

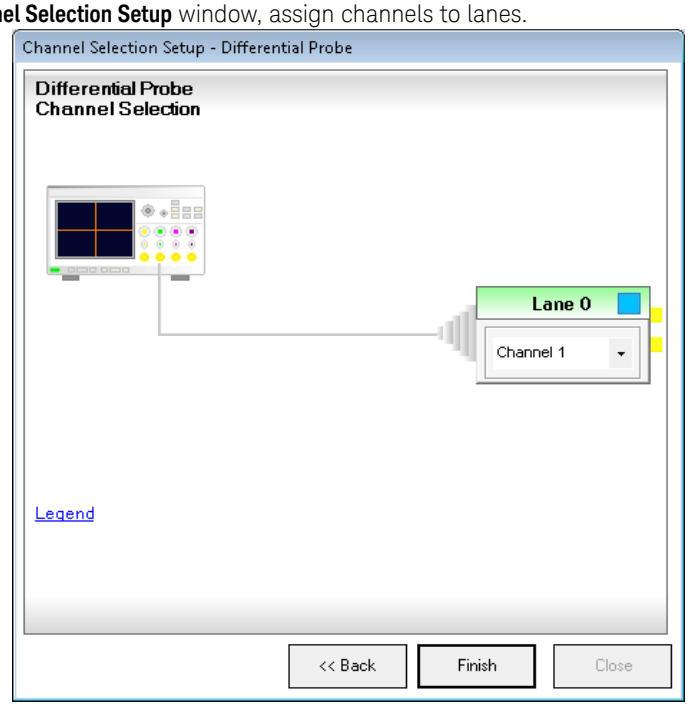
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

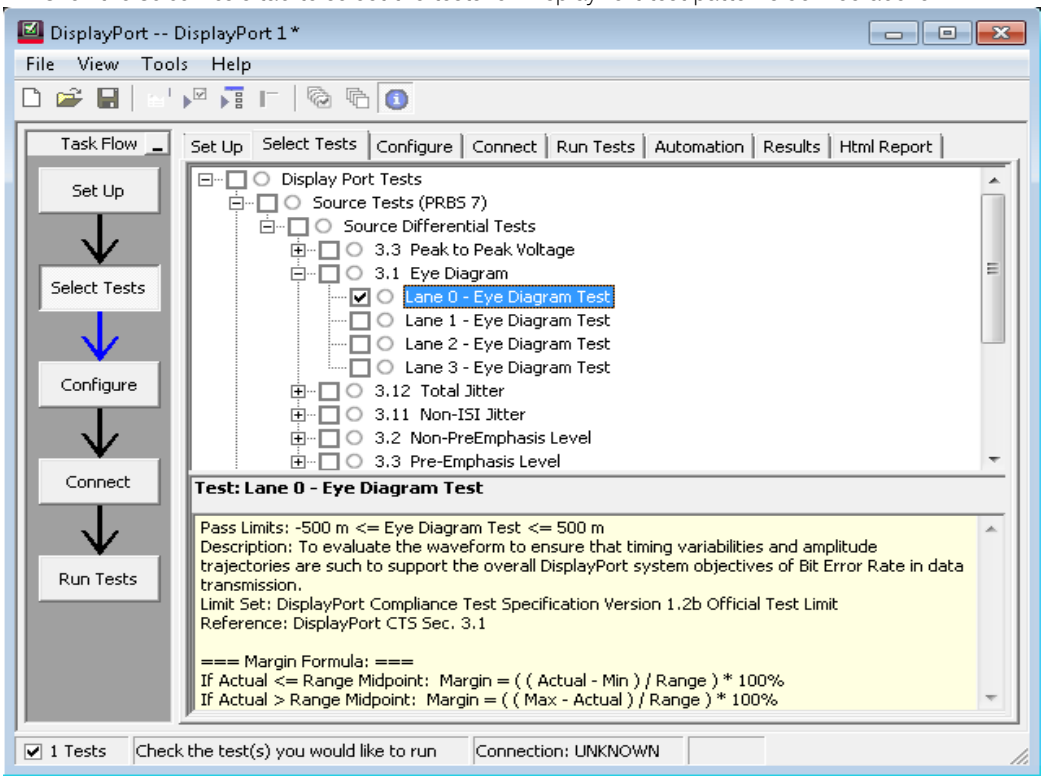


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.
11 Check for any signal trajectories that may have entered into the mask.
12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 6 shows the voltage and time coordinates for the mask used in the eye diagram.

Table 6 Eye Diagram Mask Coordinates for HBR and RBR

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	High (2.7 Gb/s)
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

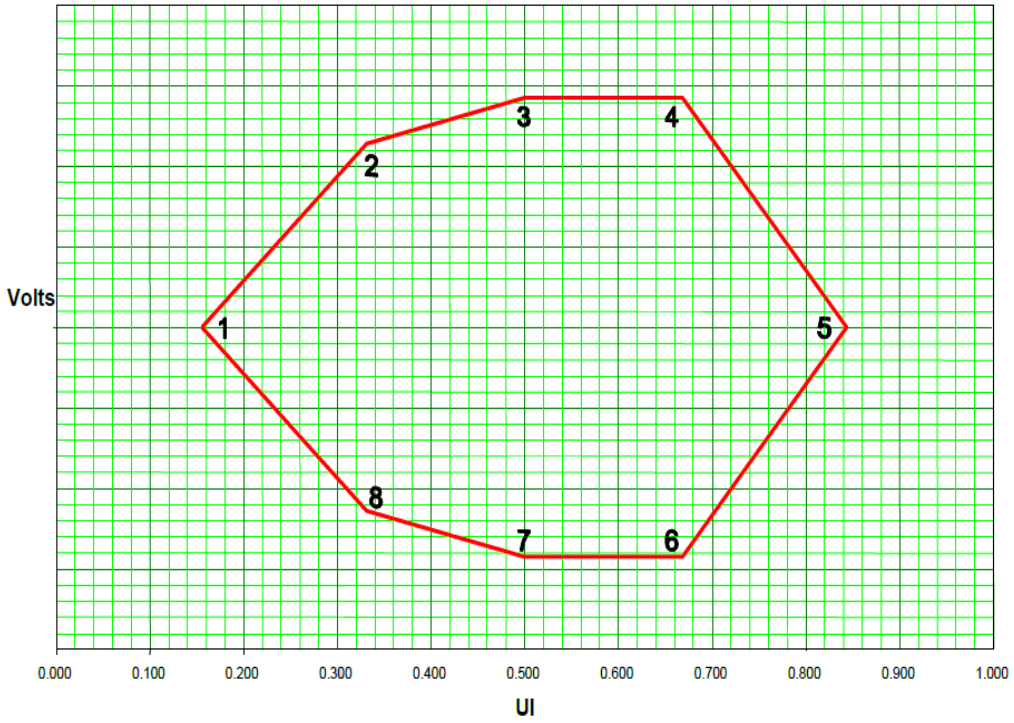


Figure 9 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-24 for RBR and Table 3-23 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

1220001, 1220002, 1220003, 1220004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

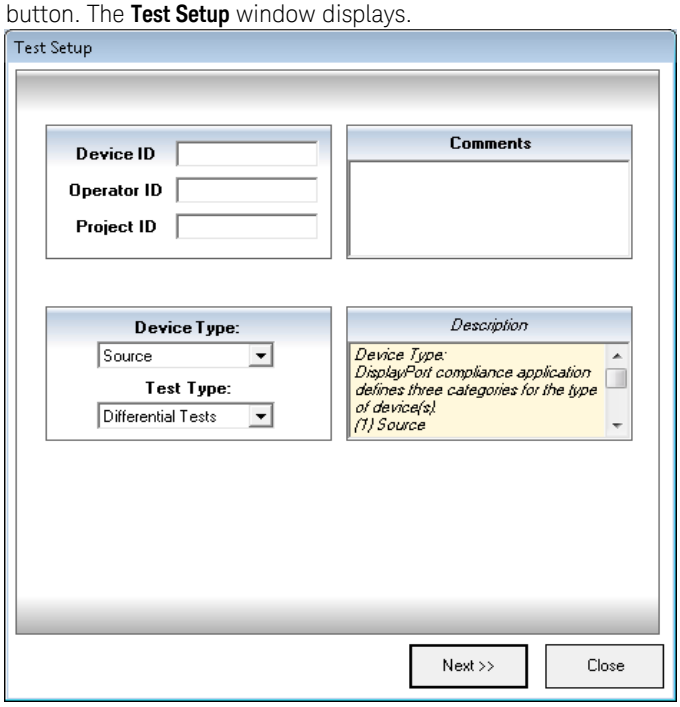
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



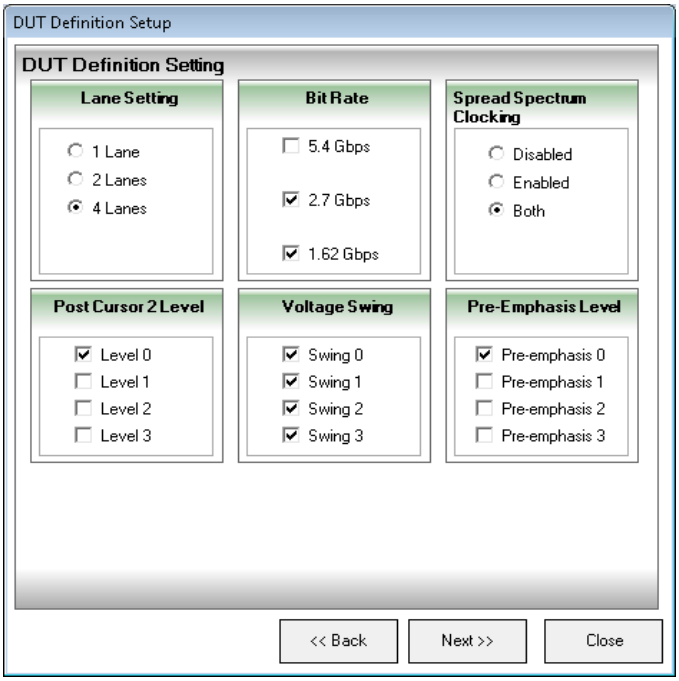
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

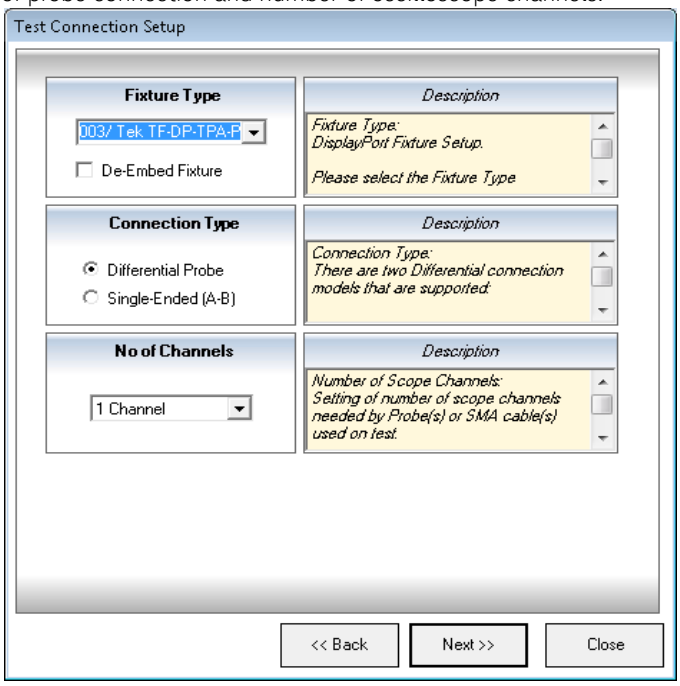
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

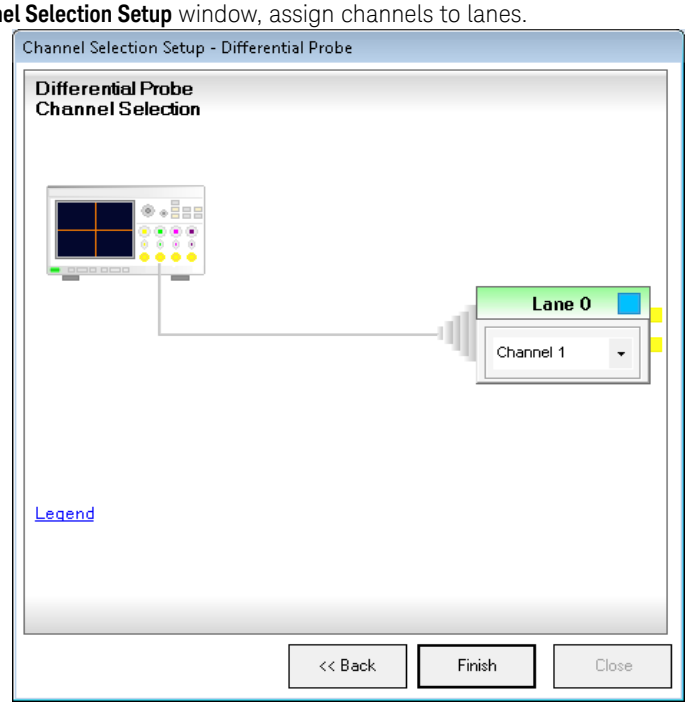
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

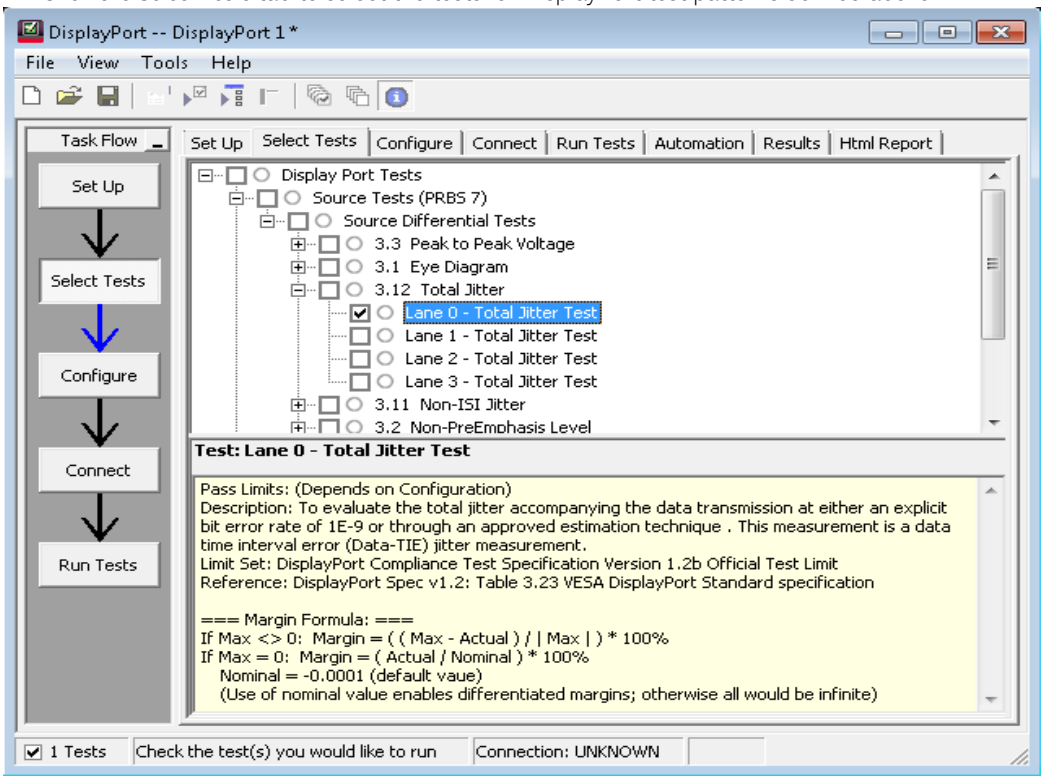


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 7 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non ISI Jitter Test

Test ID

1230001, 1230002, 1230003, 1230004 – Non ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

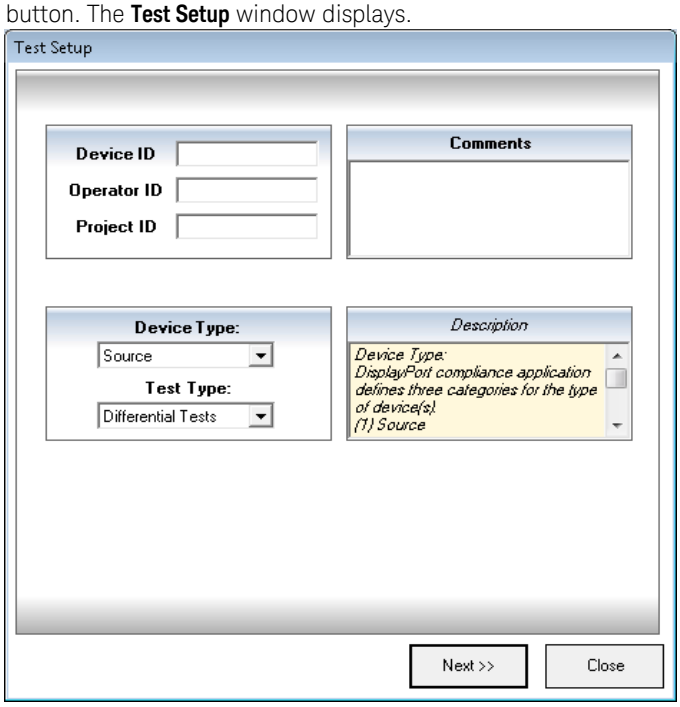
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



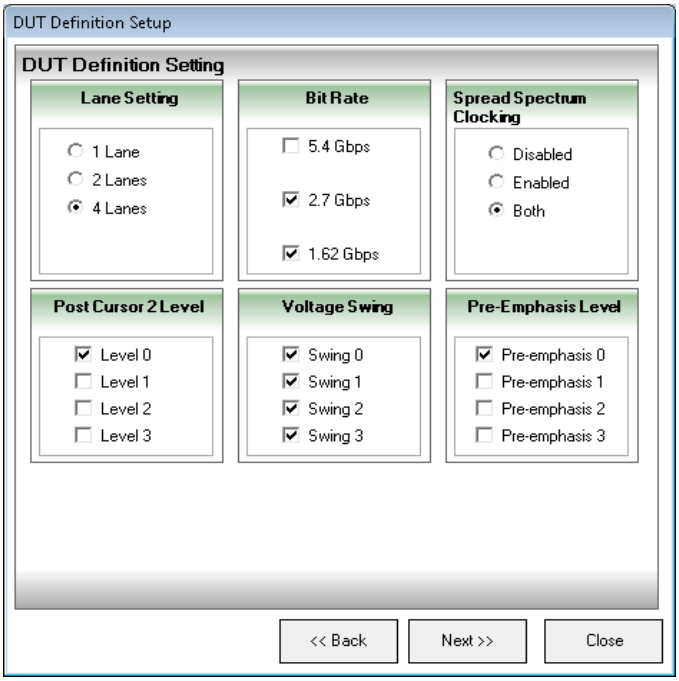
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

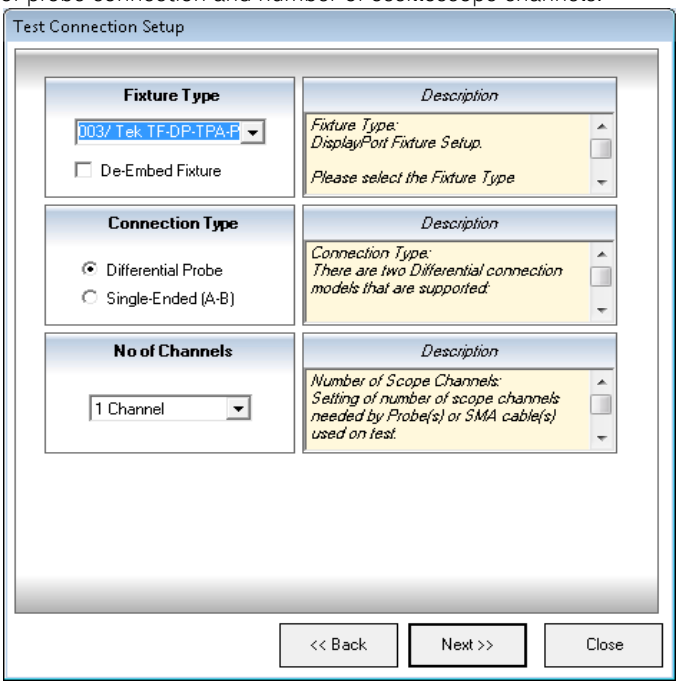
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

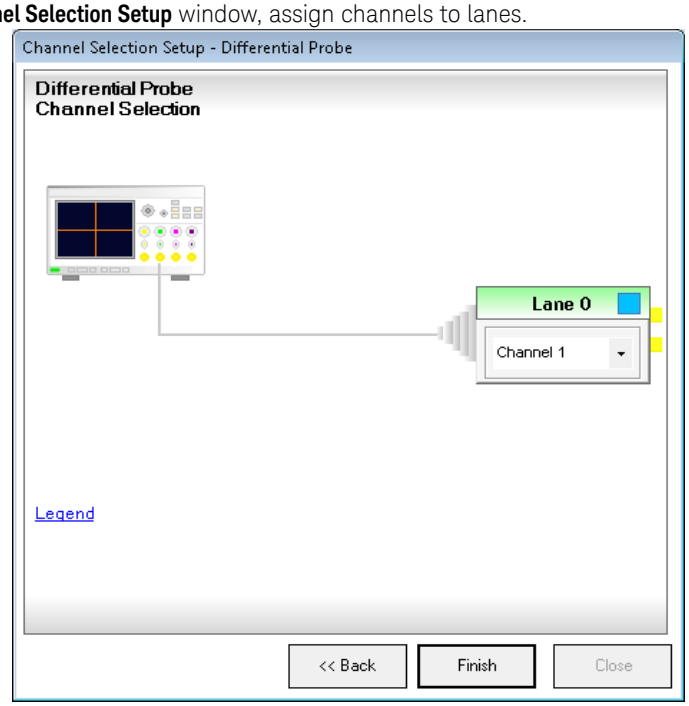
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

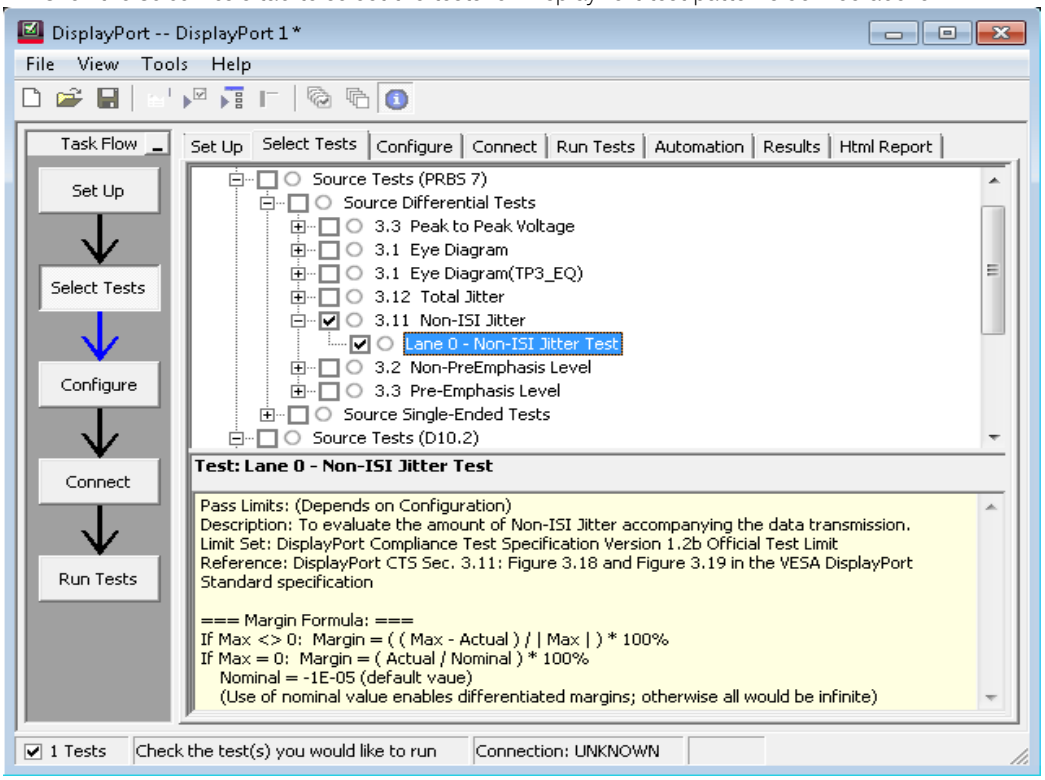


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = TJ - ISI$$

7 Report the measurement results.

PASS Condition

Table 8 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.210 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.11*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1261001, 1261002, 1261003, 1261004 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001, 1262002, 1262003, 1262004 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001, 1263002, 1263003, 1263004 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For HBR2:

- 1264101, 1264102, 1264103, 1264104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101, 1262102, 1262103, 1262104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101, 1263102, 1263103, 1263104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

Test Overview

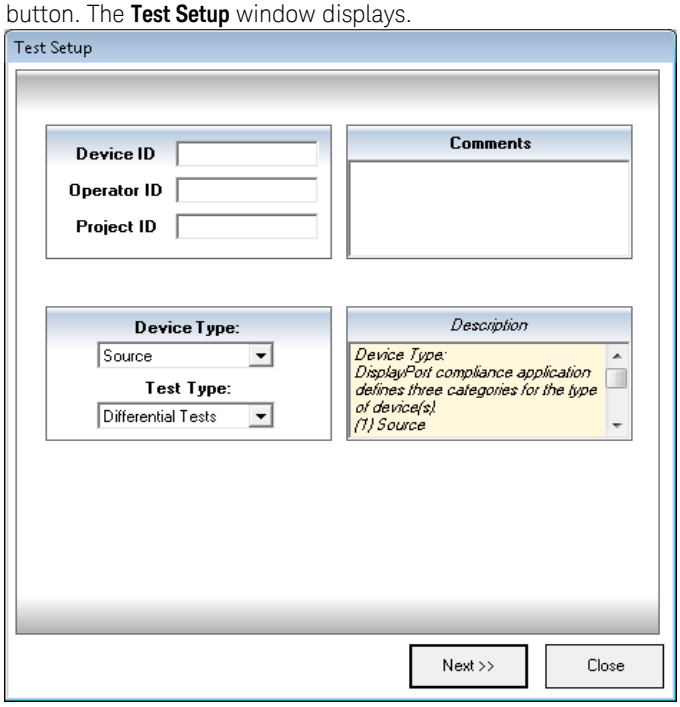
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



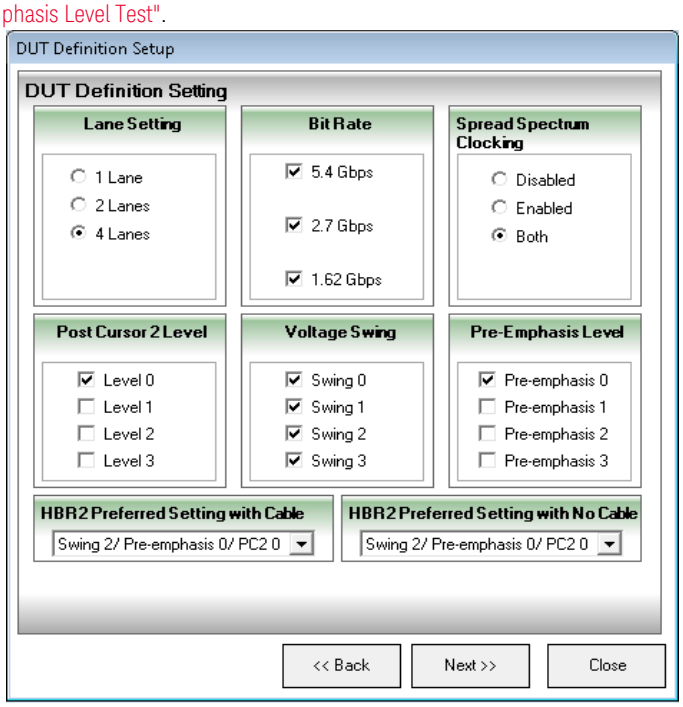
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

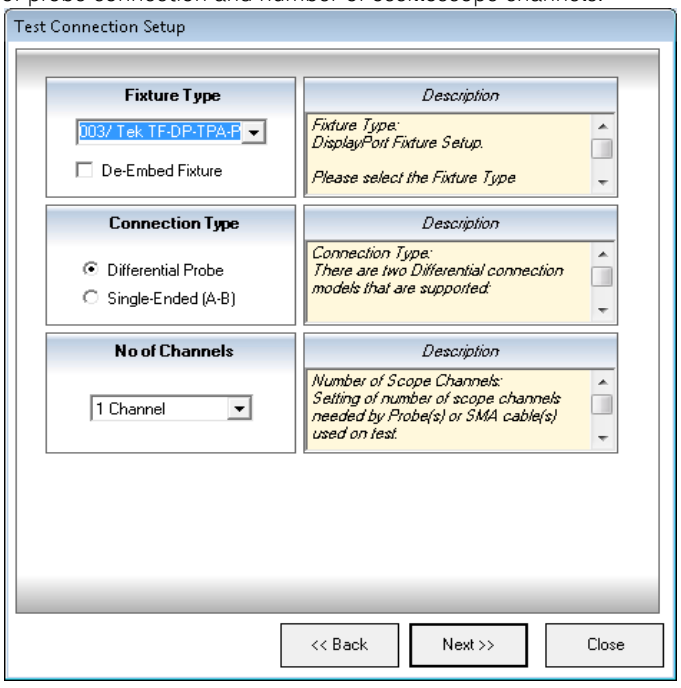
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

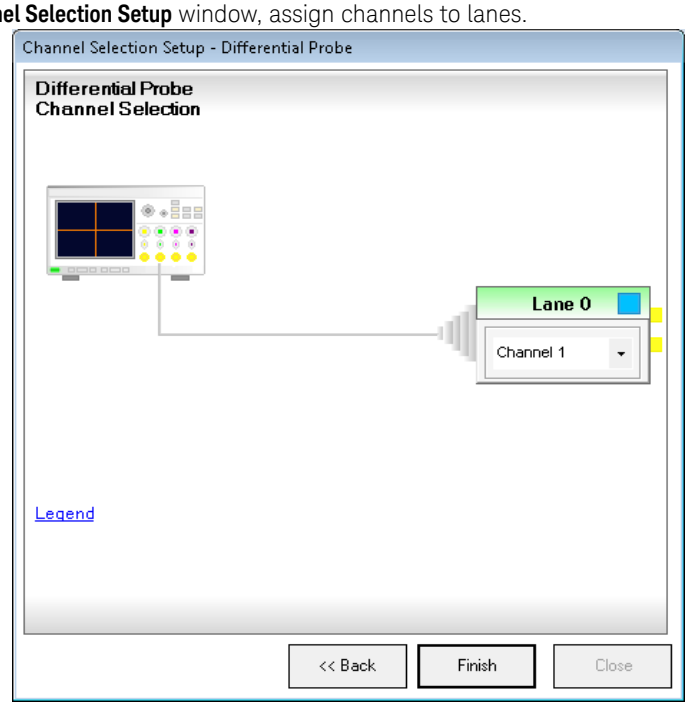
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non Pre-Emphasis Level Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

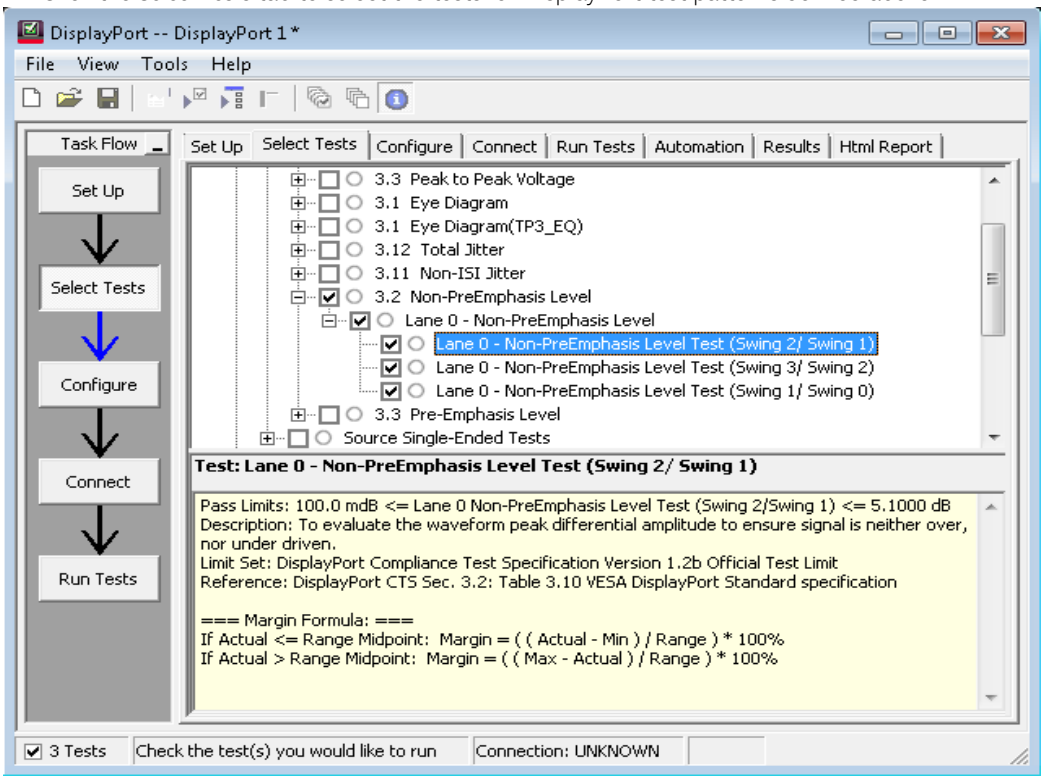


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

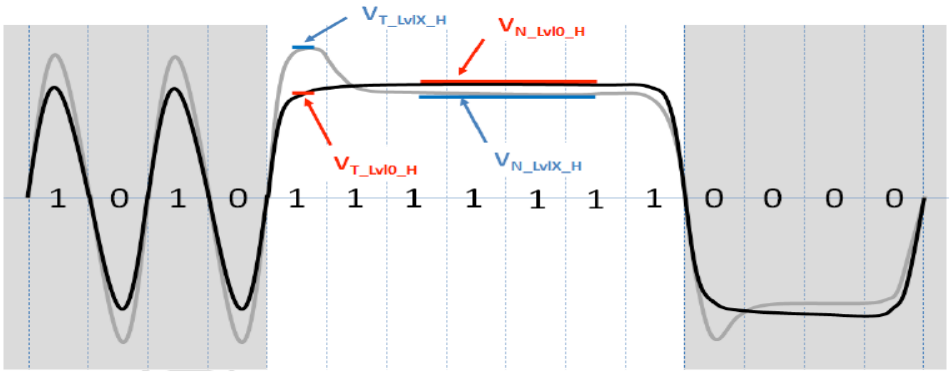


Figure 10 High Voltage measurement for RBR and HBR

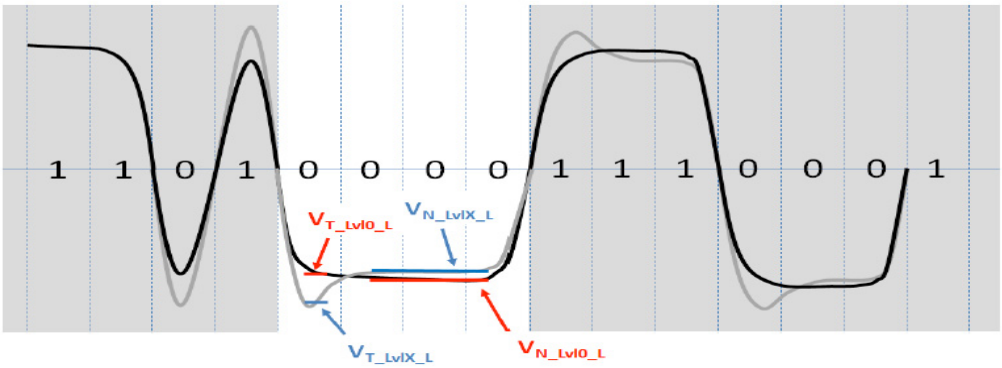


Figure 11 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in PLTPAT test pattern for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

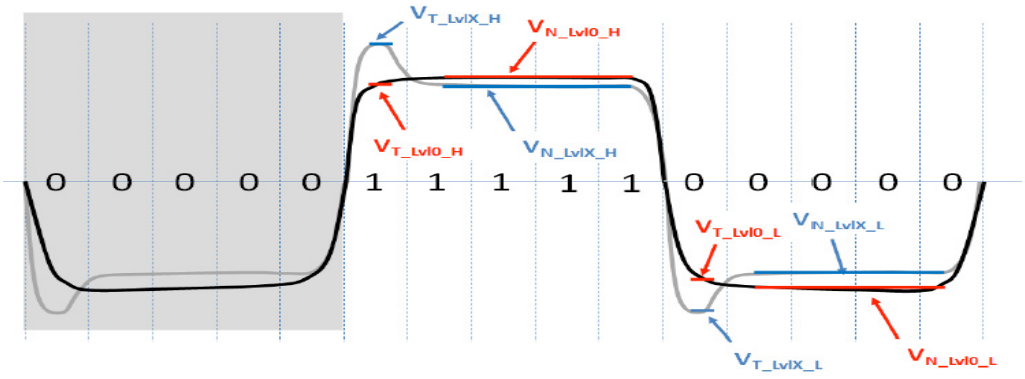


Figure 12 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * Log_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

Resultant = $20 * Log_{10}[Voltage_{Peak\text{-}Peak\_LevelA} / Voltage_{Peak\text{-}Peak\_LevelB}]$

Table 9 Compared Levels

Measurement#	$Voltage_{Peak\text{-}Peak\_LevelA}$	$Voltage_{Peak\text{-}Peak\_LevelB}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
HBR2		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
* if device optionally capable of Level 3		

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1 dB ≤ Resultant ≤ 4.4 dB

Table 10 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	
$V_{TX\text{-}OUTPUT\text{-}RATIO\_HBR2}$	Ratio of Output Voltage Level 2/Level 0	5.2	-	6.9	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	1.6	-	3.5	dB	
	Ratio of Output Voltage Level 3/Level 2	1	-	4.4	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1270001, 1270002, 1270003, 1270004 – Pre-Emphasis Level Test

For HBR2:

- 1270501, 1270502, 1270503, 1270504 – Pre-Emphasis Level Test

Test Overview

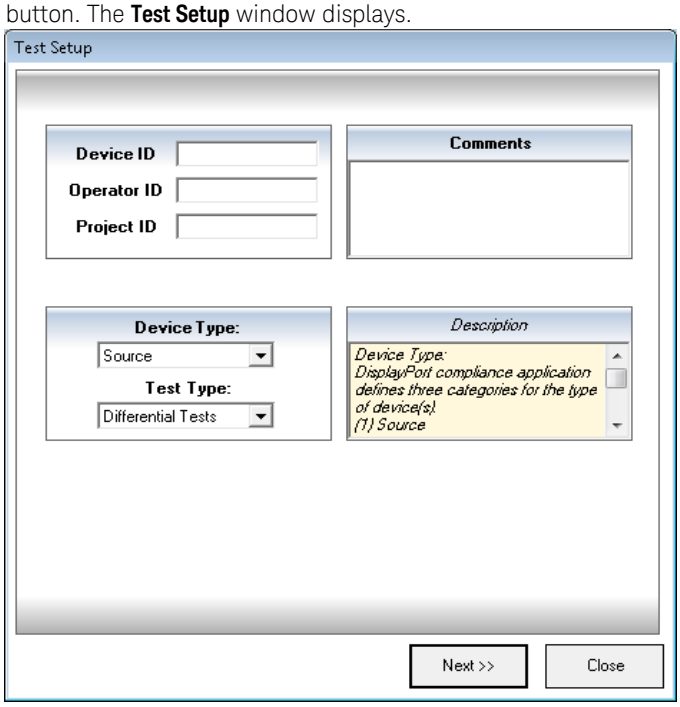
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



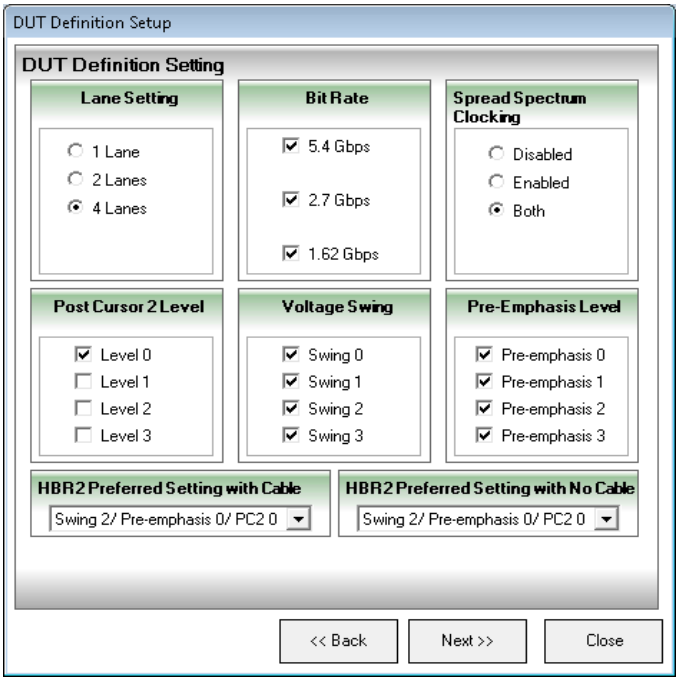
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

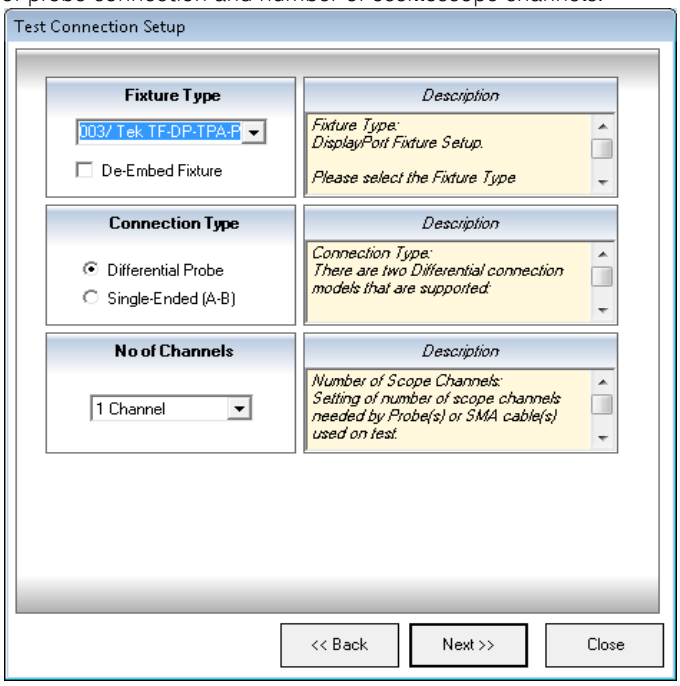
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

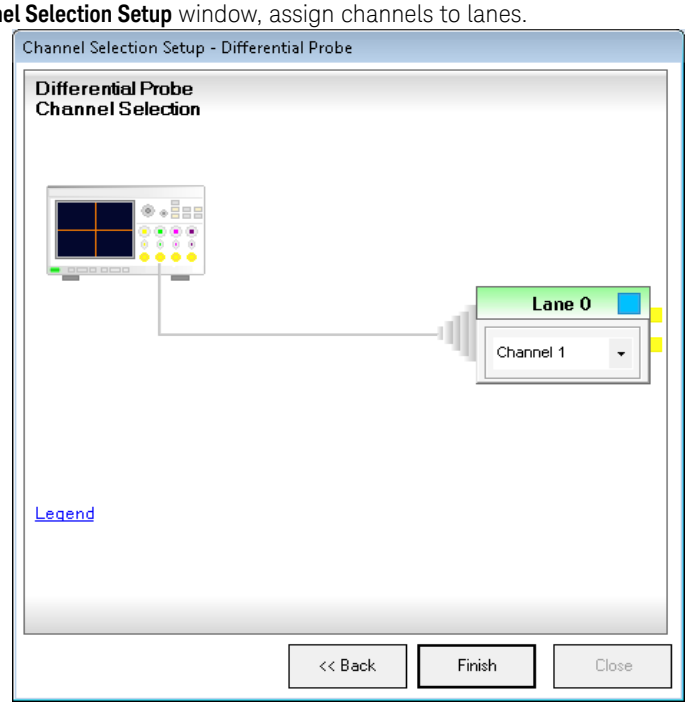
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Pre-Emphasis Level Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

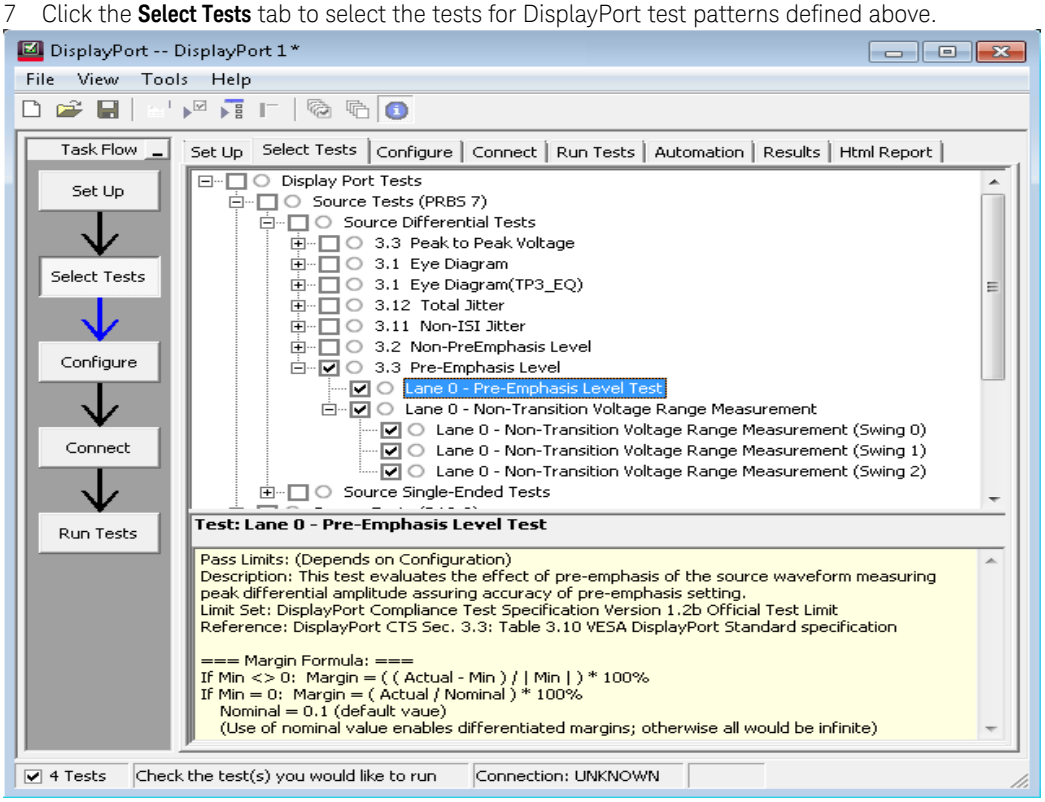


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

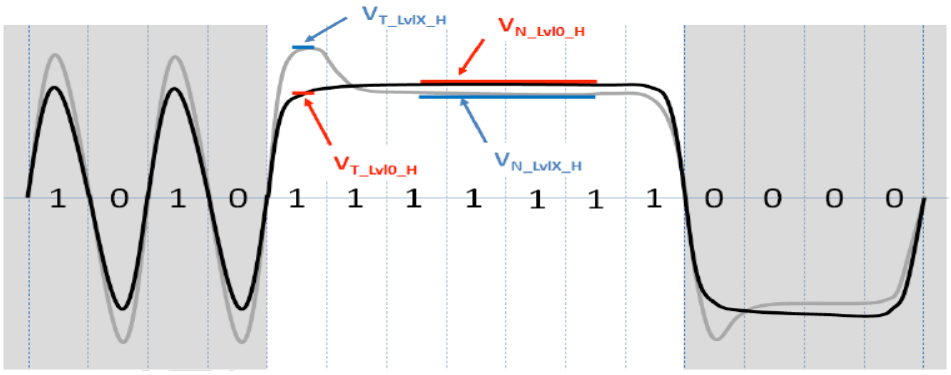


Figure 13 High Voltage measurement for RBR and HBR

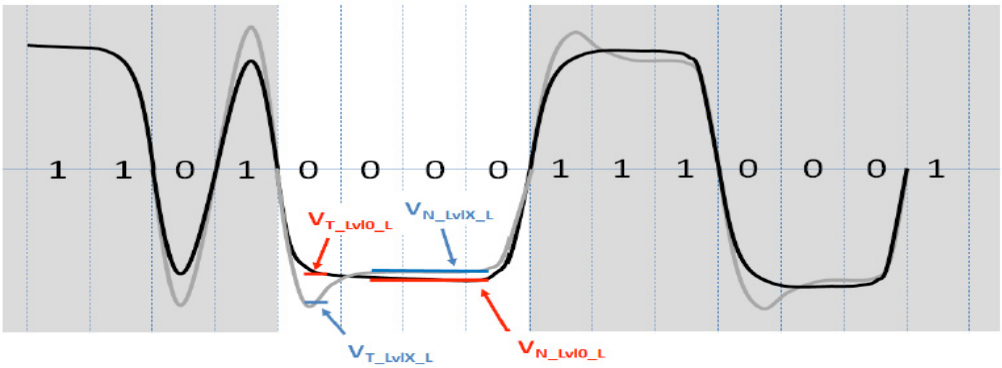


Figure 14 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PLTPAT for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

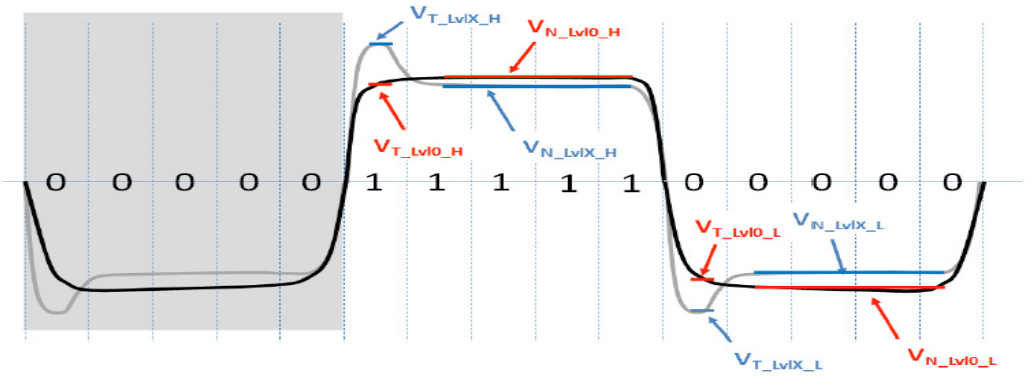


Figure 15 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log} [\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = $20 * \text{Log} [\text{Voltage}_{T\_Lvl1\_PP} / \text{Voltage}_{N\_Lvl1\_PP}] - 20 * \text{Log} [\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = $20 * \text{Log} [\text{Voltage}_{T\_Lvl2\_PP} / \text{Voltage}_{N\_Lvl2\_PP}] - 20 * \text{Log} [\text{Voltage}_{T\_Lvl1\_PP} / \text{Voltage}_{N\_Lvl1\_PP}]$ for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = $20 * \text{Log} [\text{Voltage}_{T\_Lvl3\_PP} / \text{Voltage}_{N\_Lvl3\_PP}] - 20 * \text{Log} [\text{Voltage}_{T\_Lvl2\_PP} / \text{Voltage}_{N\_Lvl2\_PP}]$ for Voltage Swing Level 0, if supported.

Table 11 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For RBR and HBR:

- 1272001, 1272002, 1272003, 1272004 – Non Transition Voltage Range Measurement (Swing 0)
- 1273001, 1273002, 1273003, 1273004 – Non Transition Voltage Range Measurement (Swing 1)
- 1274001, 1274002, 1274003, 1274004 – Non Transition Voltage Range Measurement (Swing 2)

For HBR2:

- 1272101, 1272102, 1272103, 1272104 – Non Transition Voltage Range Measurement (Swing 0)
- 1273101, 1273102, 1273103, 1273104 – Non Transition Voltage Range Measurement (Swing 1)
- 1274101, 1274102, 1274103, 1274104 – Non Transition Voltage Range Measurement (Swing 2)

Test Overview

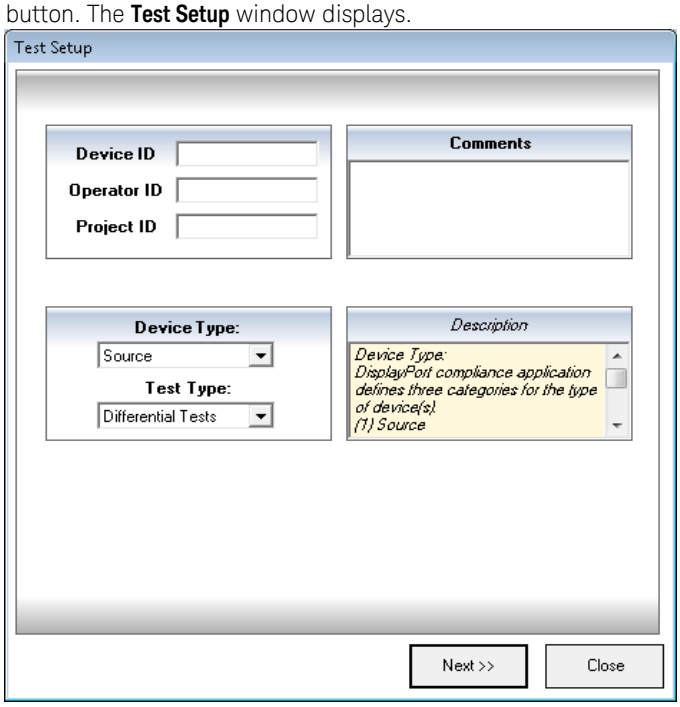
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



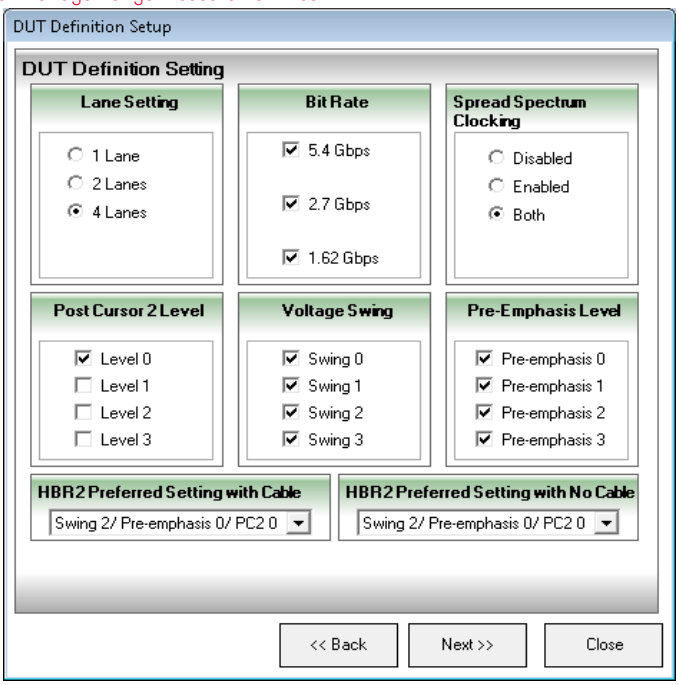
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

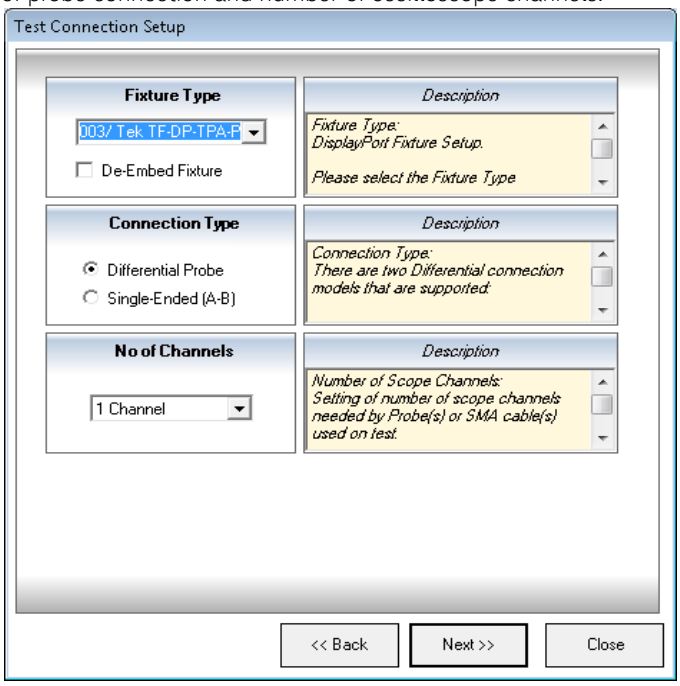
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

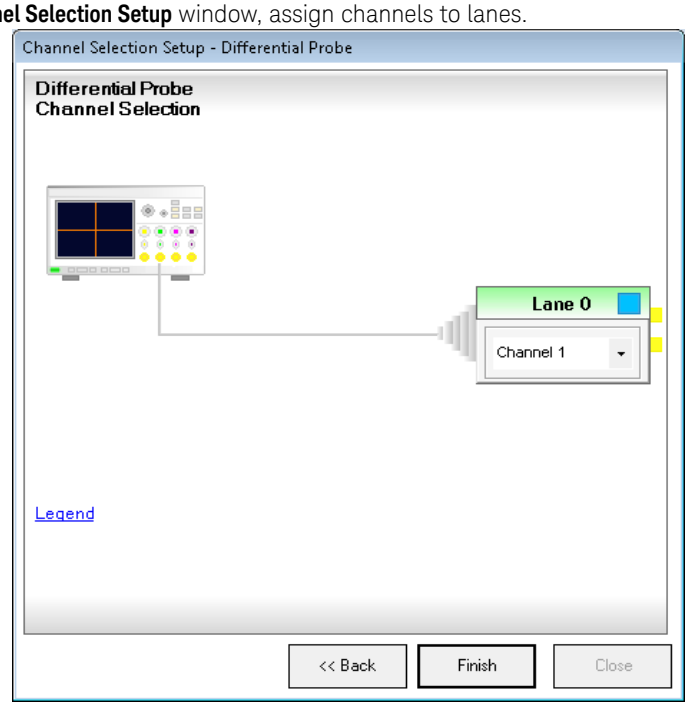
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non Transition Voltage Range Measurement Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

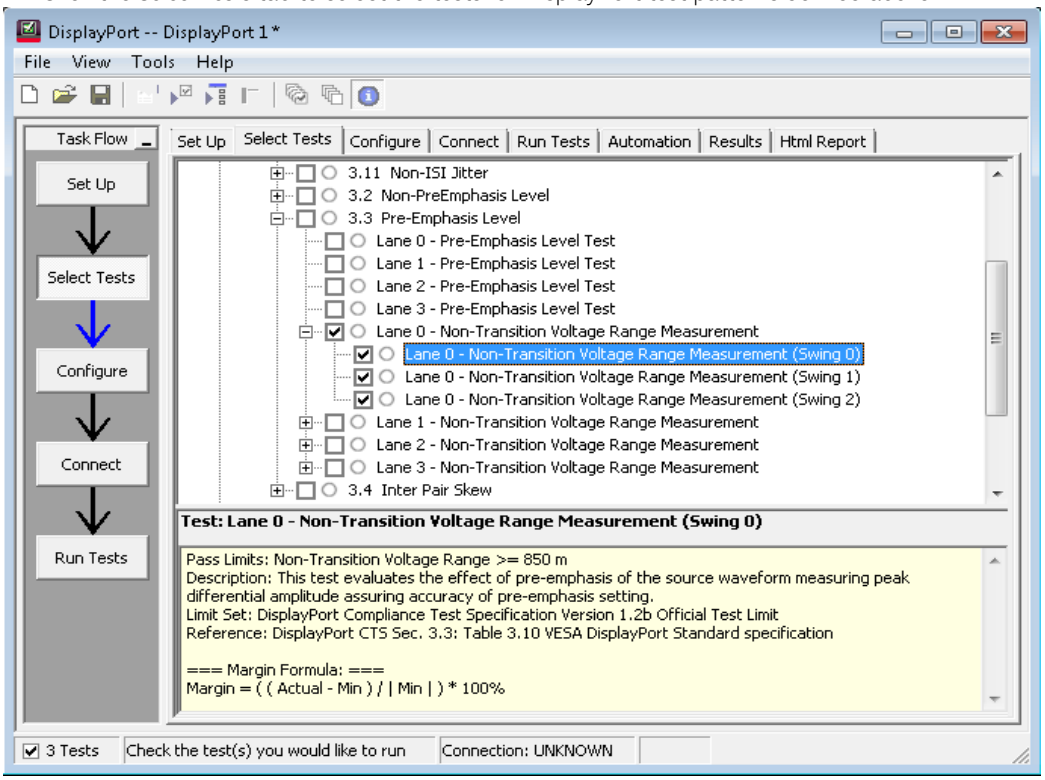


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

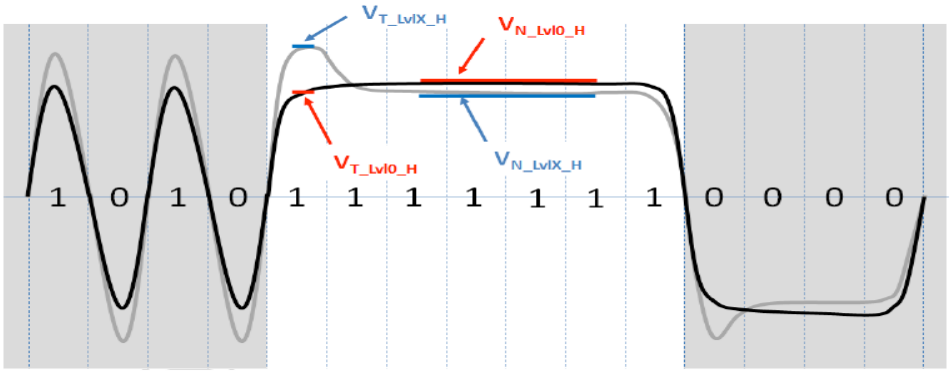


Figure 16 High Voltage measurement for RBR and HBR

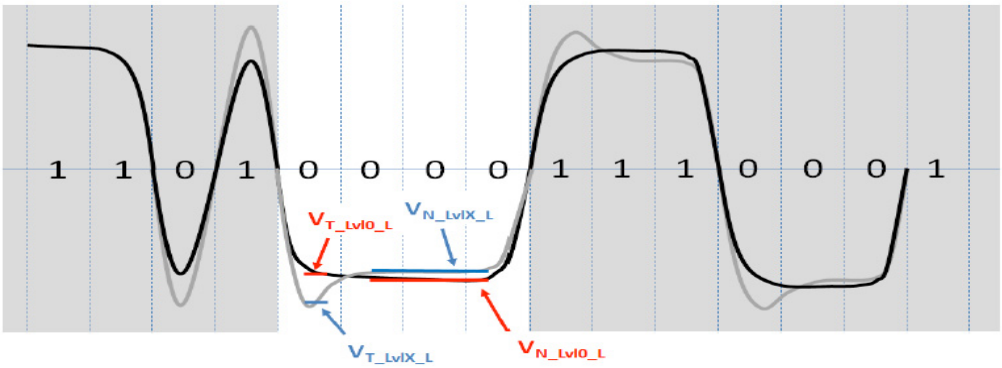


Figure 17 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PLTPAT for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

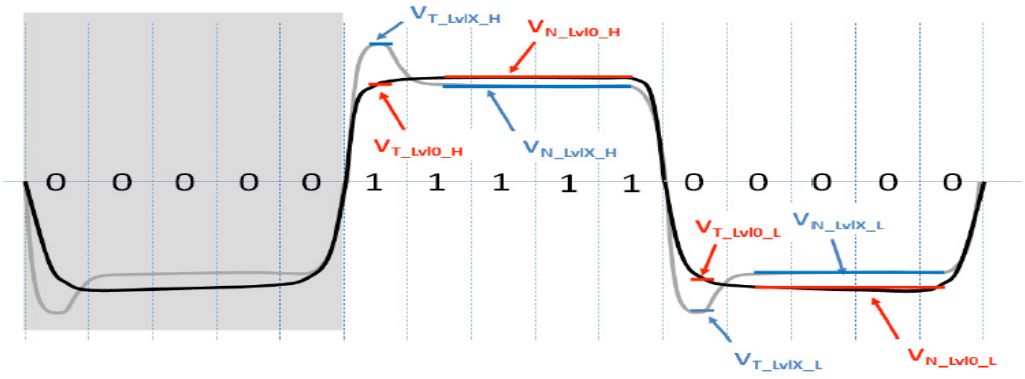


Figure 18 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant > 0.85 OR 20*log(Resultant) > -1.4dB

Table 12 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX\text{-}DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX\text{-}DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For RBR and HBR:

- 1266001, 1266002, 1266003, 1266004 – Peak to Peak Voltage Test

For HBR2:

- 1266101, 1266102, 1266103, 1266104 – Peak to Peak Voltage Test

Test Overview

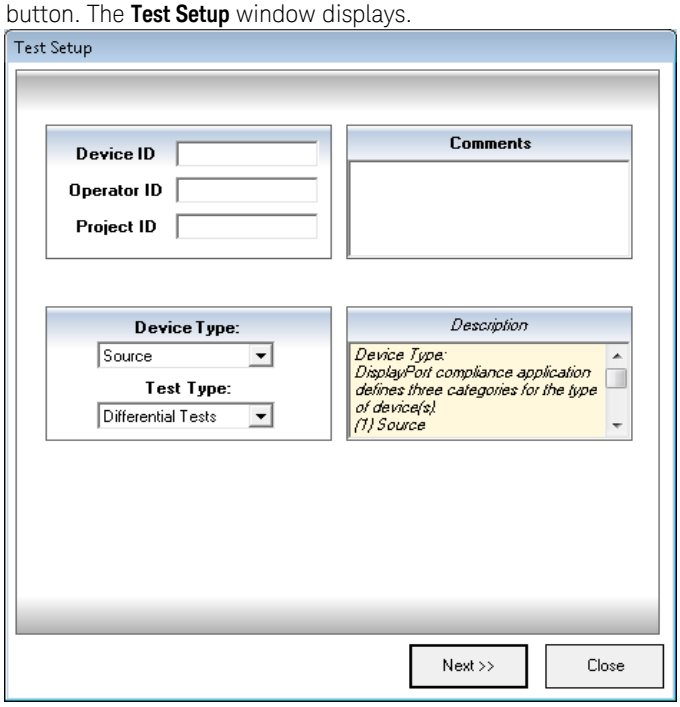
The objective of this test is to evaluate the maximum differential peak to peak voltage.

Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



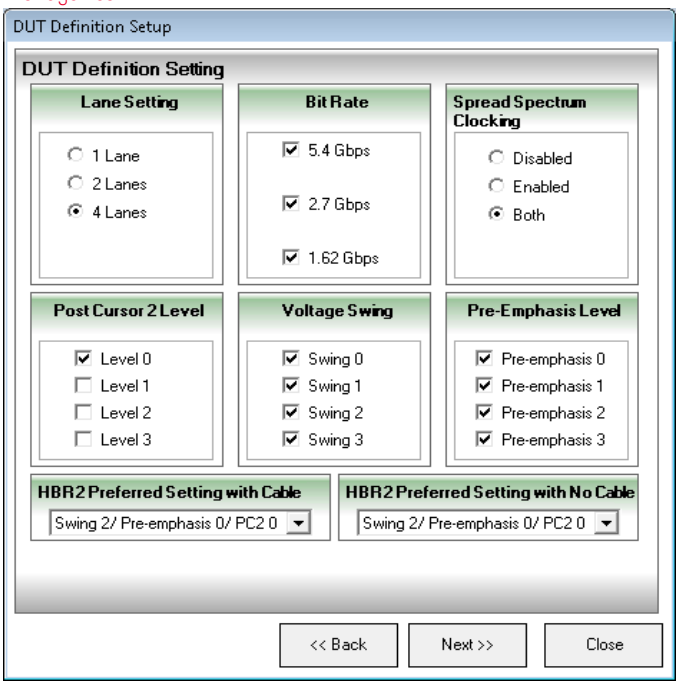
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

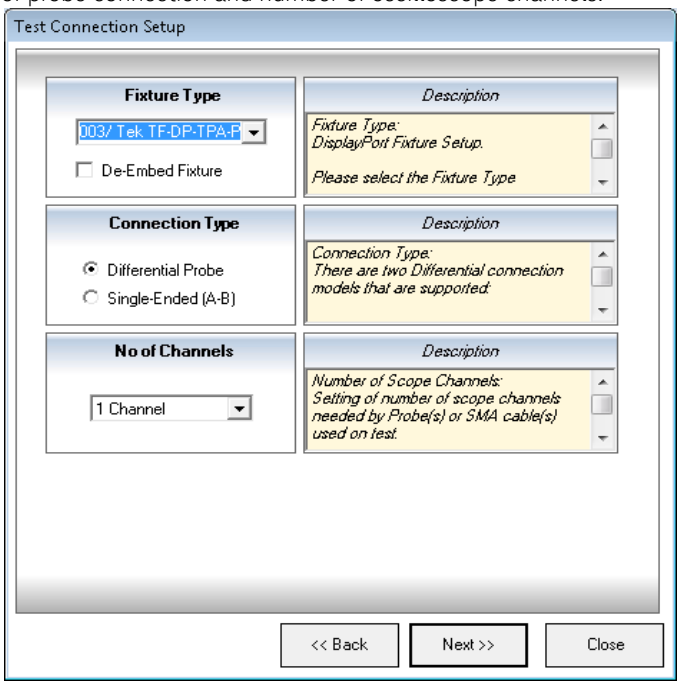
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

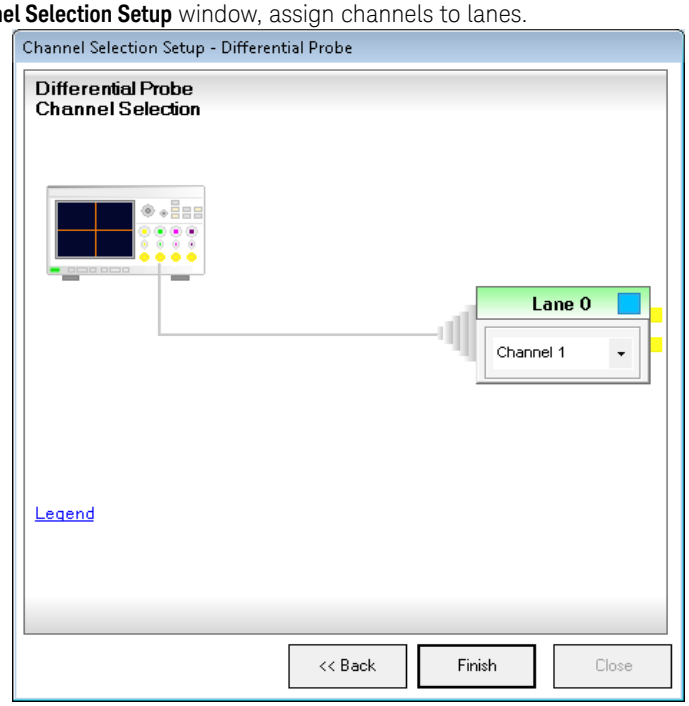
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Peak to Peak Voltage Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

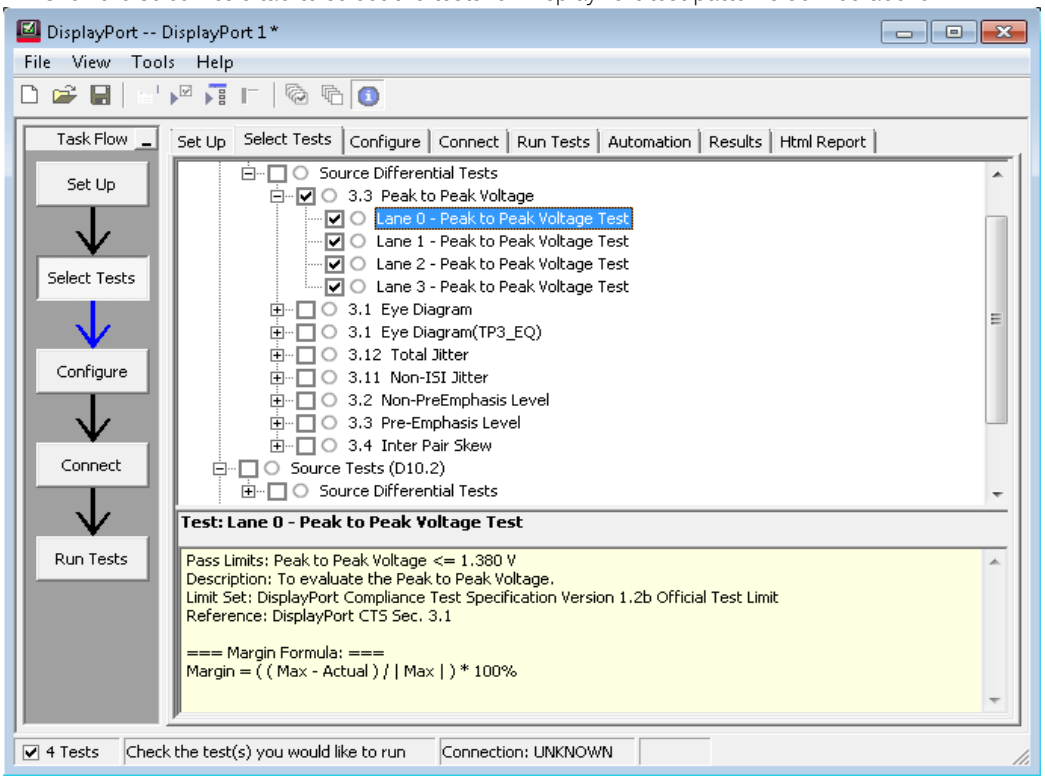


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

Peak to Peak Voltage = Maximum Voltage - Minimum Voltage

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V

Table 13 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Inter Pair Skew Test

Test ID

1290001 – Lane0/Lane1 Inter-Pair Skew Test

1290002 – Lane0/Lane2 Inter-Pair Skew Test

1290003 – Lane0/Lane3 Inter-Pair Skew Test

1290004 – Lane1/Lane2 Inter-Pair Skew Test

1290005 – Lane1/Lane3 Inter-Pair Skew Test

1290006 – Lane2/Lane3 Inter-Pair Skew Test

Test Overview

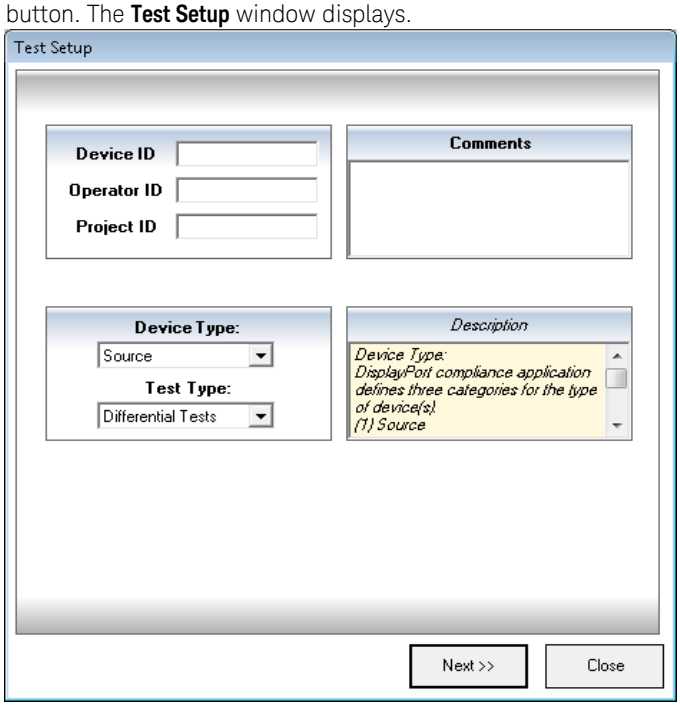
The objective of the test is to evaluate the skew or time delay between differential data lanes in the DisplayPort interface.

Test Conditions for Inter Pair Skew Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported For two lane operation: Lane 0 to Lane 1 For four lane operation: Lane 0 to Lane 1 Lane 0 to Lane 2 Lane 0 to Lane 3 Lane 1 to Lane 2 Lane 1 to Lane 3 Lane 2 to Lane 3
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



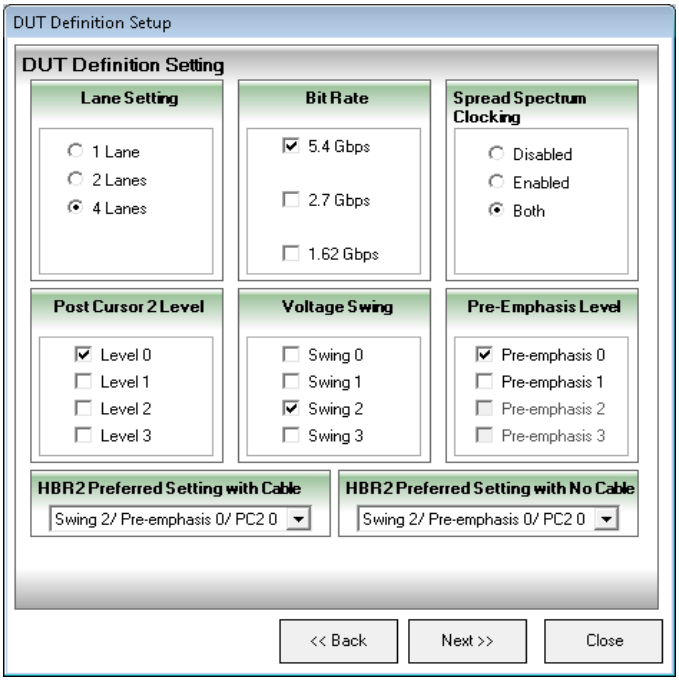
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

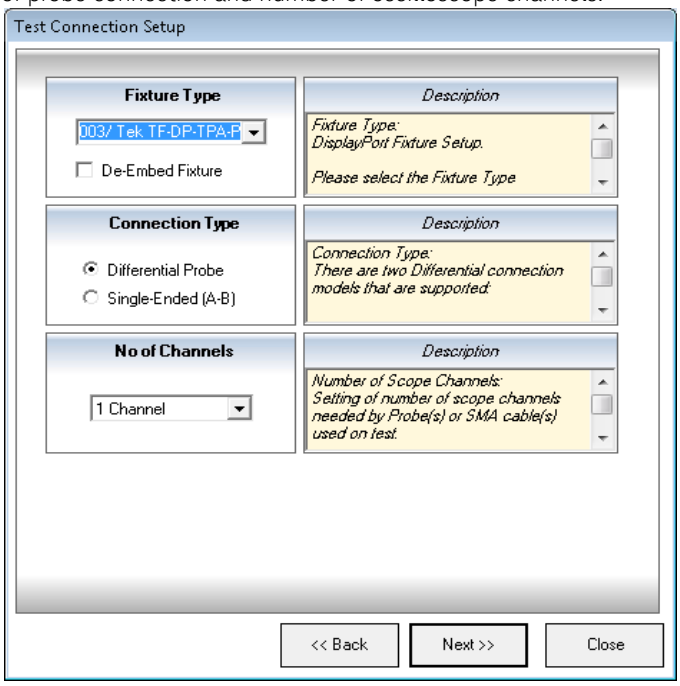
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

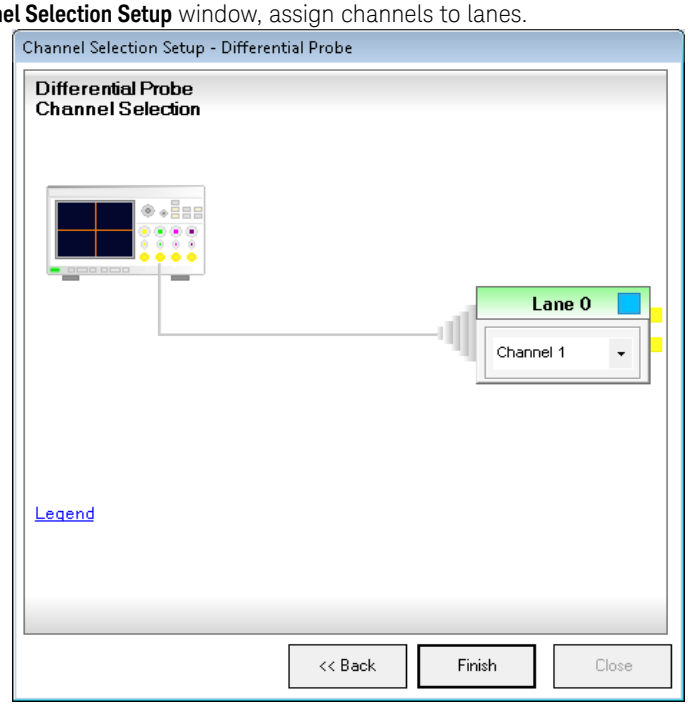
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Inter Pair Skew Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

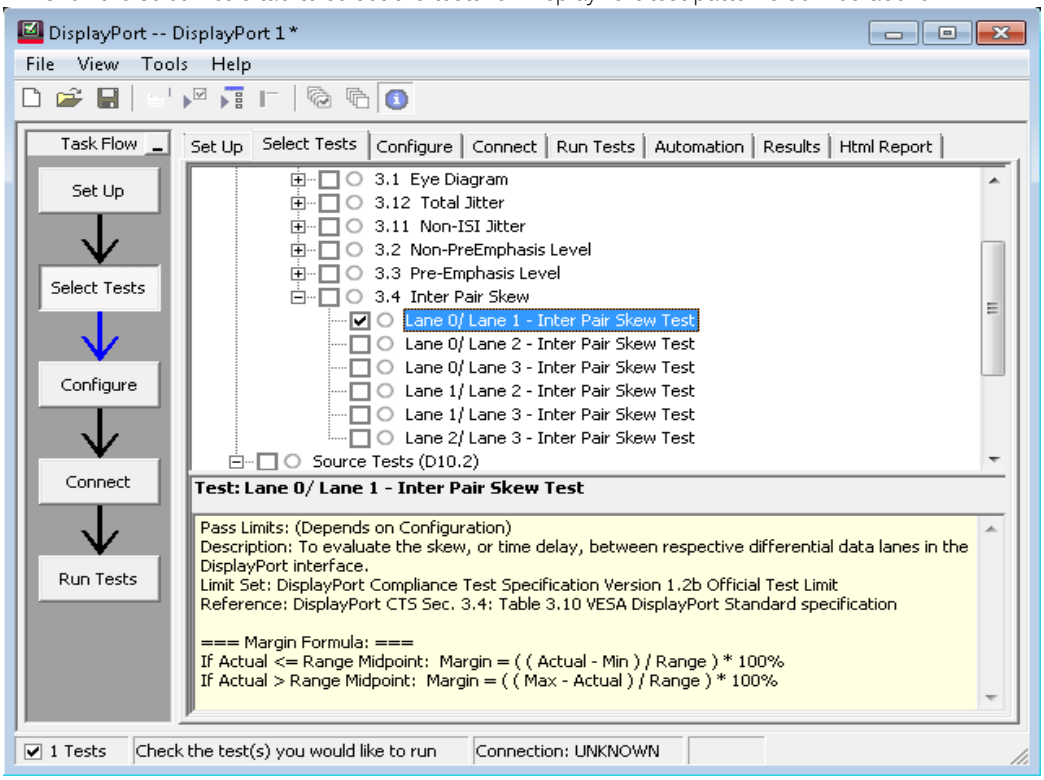


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given inter-pair skew measurement of Lane A to Lane B:
   a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   b Acquire and verify the input signal:
      i Verify the trigger and the amplitude of the Lane A input signal.
      ii Scale the vertical display of the Lane A input signal to optimum value.
      iii Measure V_{TOP} and V_{BASE} of the Lane A input signal.
      iv Verify the trigger and the amplitude of the Lane B input signal.
      v Scale the vertical display of the Lane B input signal to optimum value.
      vi Measure V_{TOP} and V_{BASE} of the Lane B input signal.
      vii Measure the data rate of the Lane A input signal.
      viii Measure the data rate of the Lane B input signal.
   c Set up the parameter of the measurement:
      i Enable measurement of all edges to obtain a statistical value of the measurement.
      ii Set up the measurement threshold.
   d Set up the parameter for the inter-pair skew measurement:
      i Set up two display grids such that each grid displays one test lane data signal.
      ii Set up the measurement threshold for each test lane data signal on the Transition Voltage = 0V.
      iii Decode the data signal for each test lane.
      iv Search the desired pattern from the decoded data signal.
      v Measure the time difference between the corresponding edges of both test lanes:

$$T_{Transition\_LaneA} - T_{Transition\_LaneB}$$

      vi Repeat the previous step until you measure 100 edges.
      vii VESA DisplayPort 1.2a Standard specifies 20 UI offset Lane 0 to Lane 1, Lane 1 to Lane 2 and Lane 2 to Lane 3. The resultant offset is cumulative.
      viii Calculate the inter-pair skew using the equation:

$$\text{Inter-Pair Skew} = \{1/\text{Number of Edges}\} \sum |T_{Transition\_LaneA} - T_{Transition\_LaneB}| - \text{Nominal Skew}$$

   where, Nominal Skew is the expected offset between tested lanes.
2 Report the measurement results.

PASS Condition

For RBR or HBR: -2UI $\leq$ Inter-Lane Skew Tolerance $\leq$ 2UI.

For HBR2: -(4UI + 500ps) $\leq$ Inter-Lane Skew Tolerance $\leq$ (4UI + 500ps).

Table 14 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$L_{TX-SKEW-INTER\_PAIR-HBR\_RBR}$	Lane-to-Lane Output Skew	-	-	2	UI	Applies to transmitters capable of 2- and 4-lane operation. Also, applies to all pairwise combinations of supported lanes.
$L_{TX-SKEW-INTER\_PAIR-HBR2}$	Lane-to-Lane Output Skew	-	-	4UI + 500ps		

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured inter-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

12193001 12193002 12193003 12193004 – Main Link Frequency Compliance

Test Overview

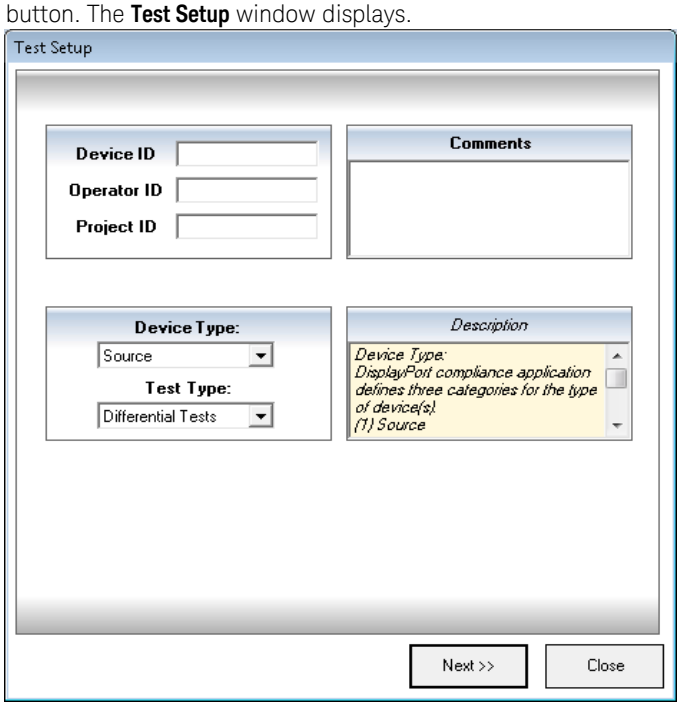
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.2a Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



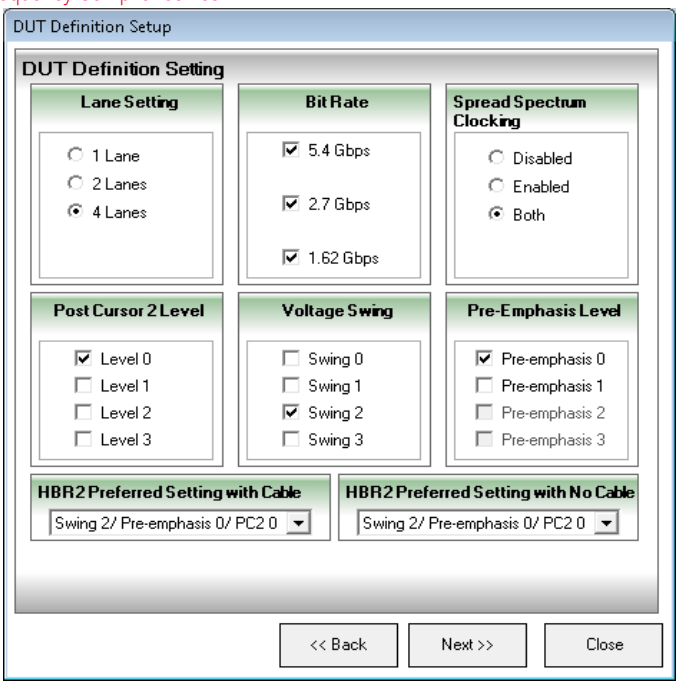
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

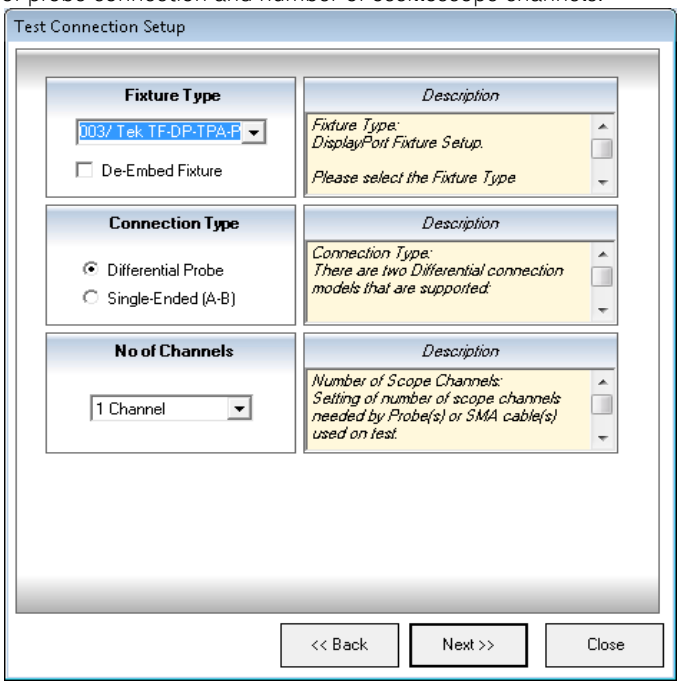
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

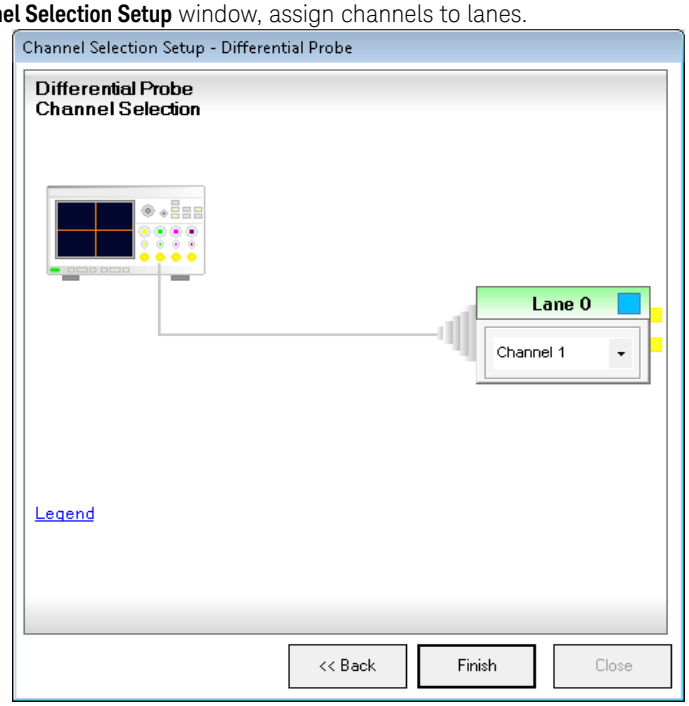
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Main Link Frequency Compliance Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

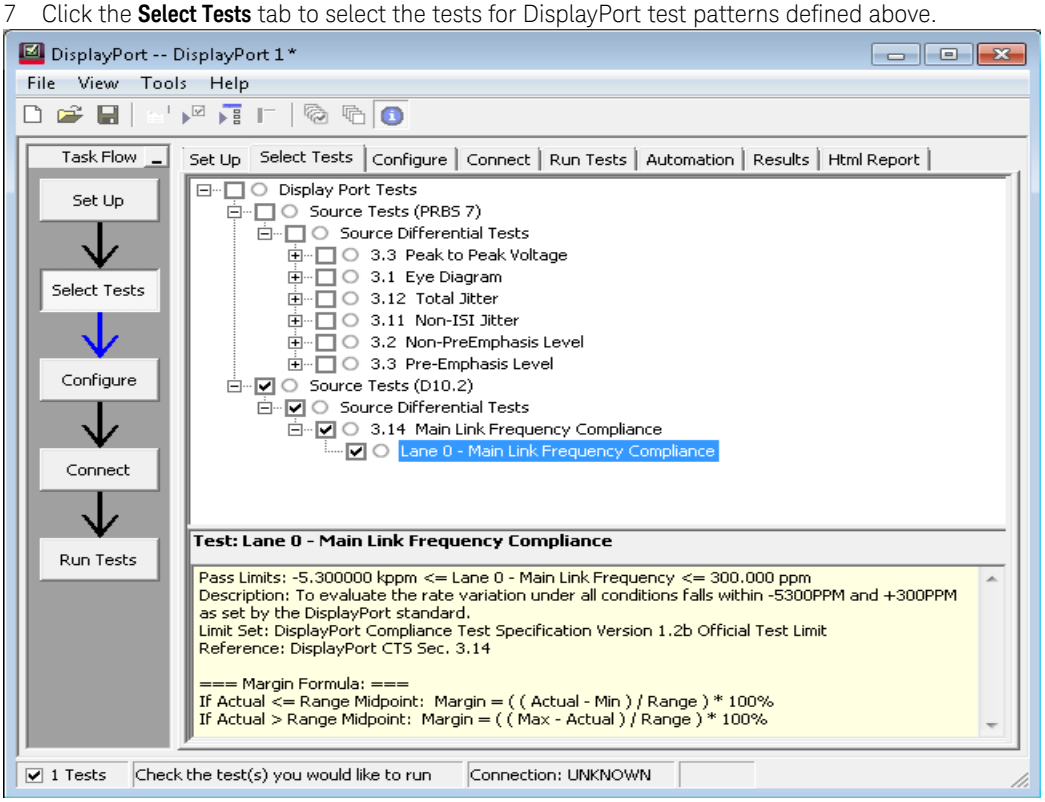


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.
5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.

9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:

a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.

b Acquire the signal with one complete SSC cycle.

c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

Maximum Data Rate = 1 / (Minimum Unit Interval)

d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

Minimum Data Rate = 1 / (Maximum Unit Interval)

e Repeat steps b, c and d until you acquire 10 SSC Cycles.

f Calculate the mean value for the maximum and minimum data rates.

10 Report the measurement results.

PASS Condition

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

Table 15 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.14*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

12170001 12170002 12170003 12170004 – SSC Modulation Frequency Test

Test Overview

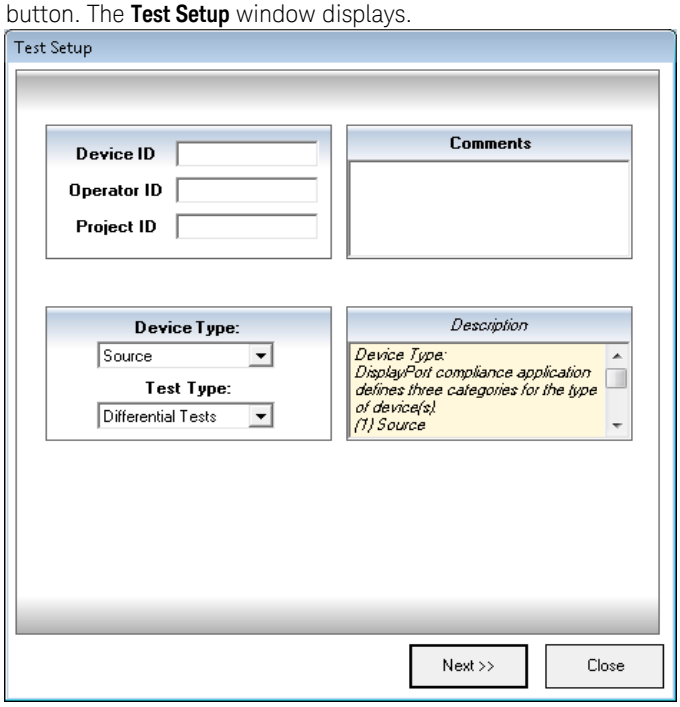
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



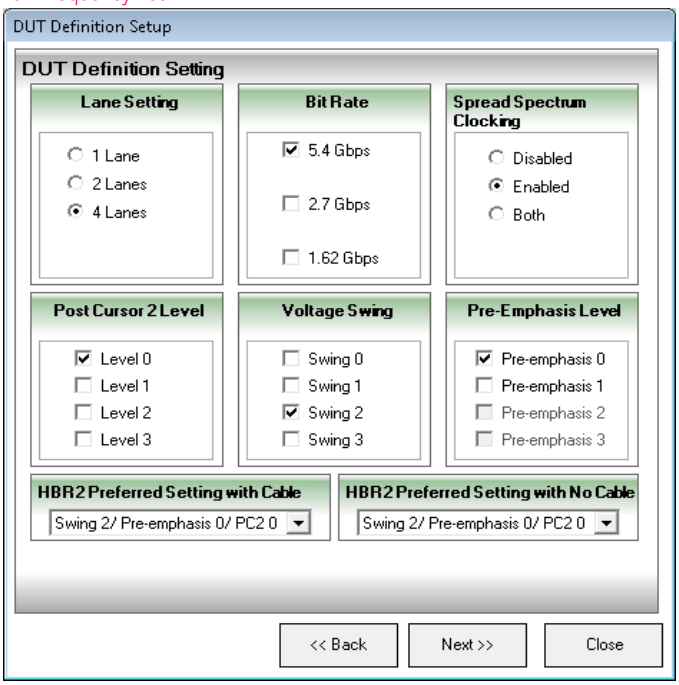
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

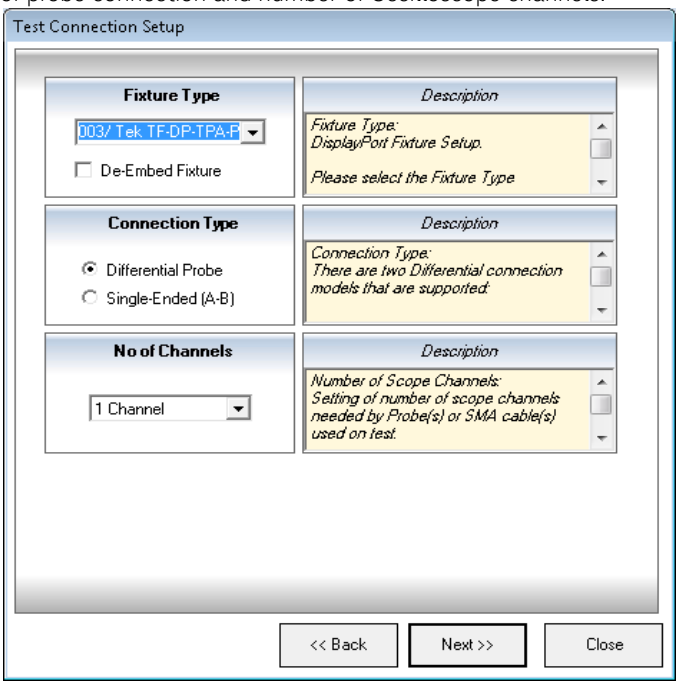
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

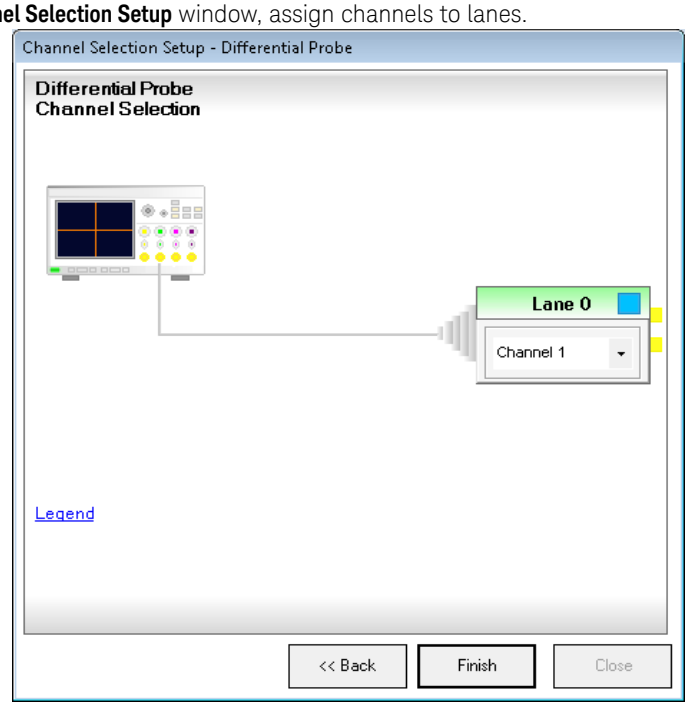
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Modulation Frequency Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

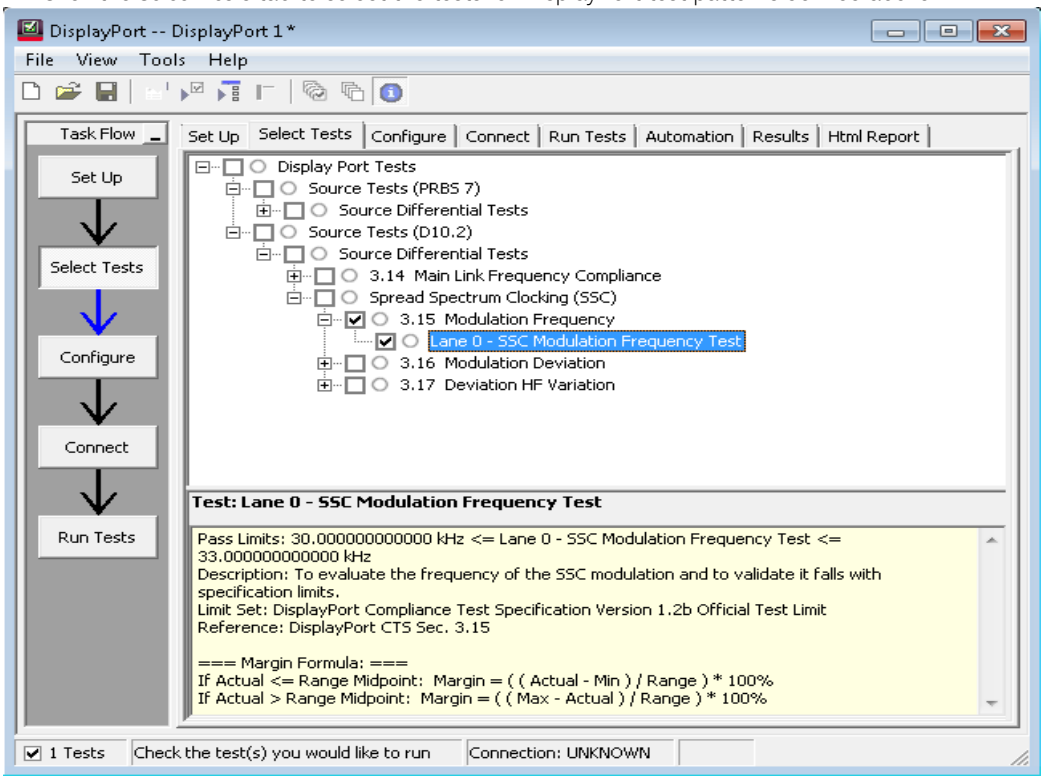


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
   g Acquire the signal for 10 SSC Cycles.
6 Get the mean value for the SSC Modulation frequency.
7 Report the measurement results.

PASS Condition

30kHz ≤ SSC Modulation Frequency (f_{SSC}) ≤ 33kHz

Table 16 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

12180001 12180002 12180003 12180004 – SSC Modulation Deviation Test

Test Overview

The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2^{nd} order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

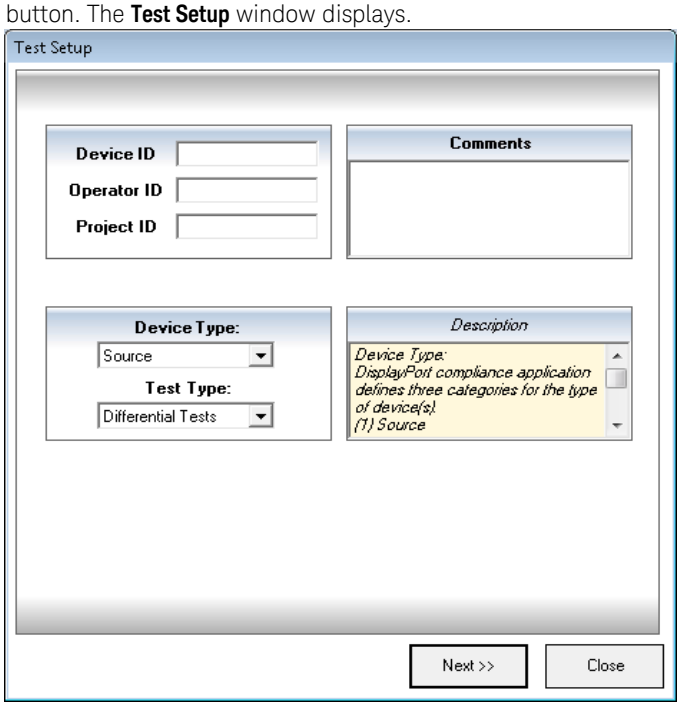
SSC Modulation Deviation = {[Average (Maximum Data Rate) - Average (Minimum Data Rate)] / Nominal Data Rate}*1e6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



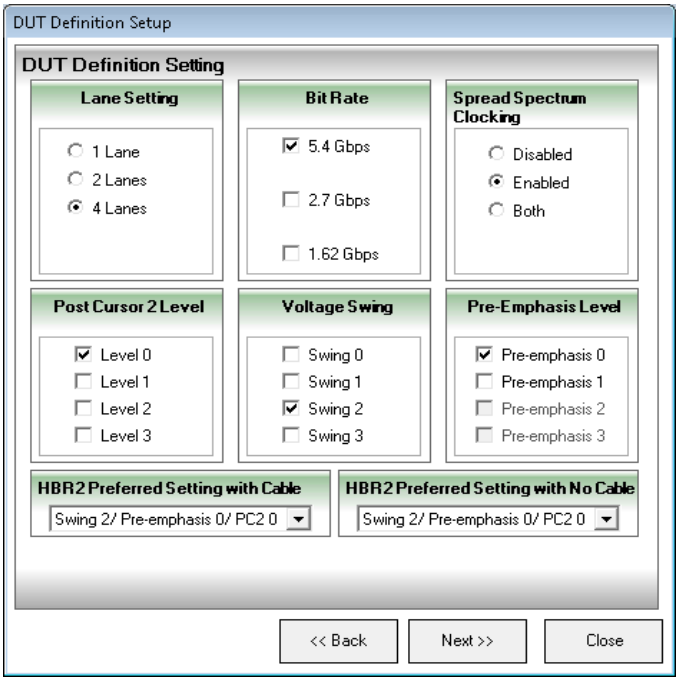
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

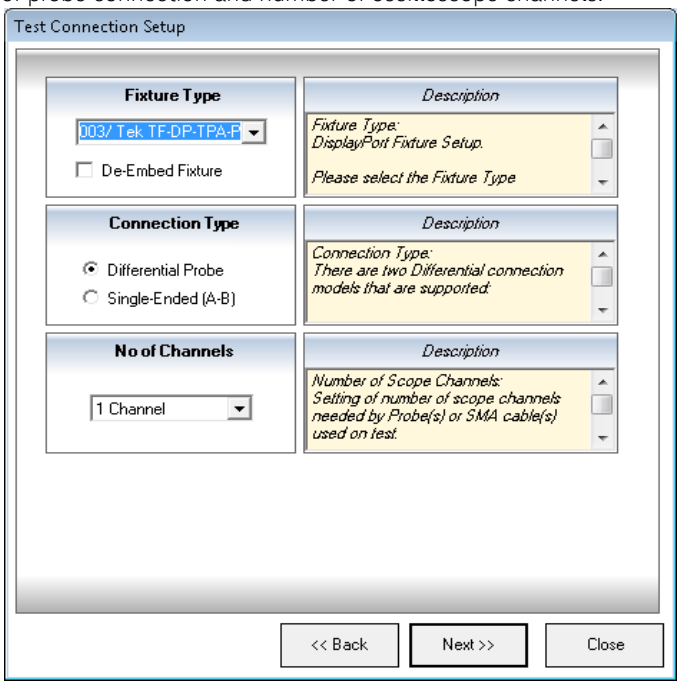
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

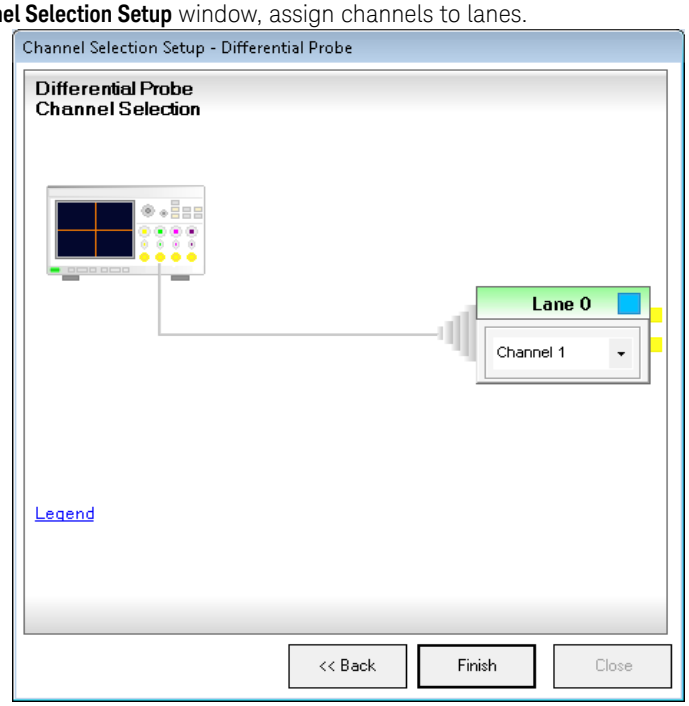
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Modulation Deviation Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

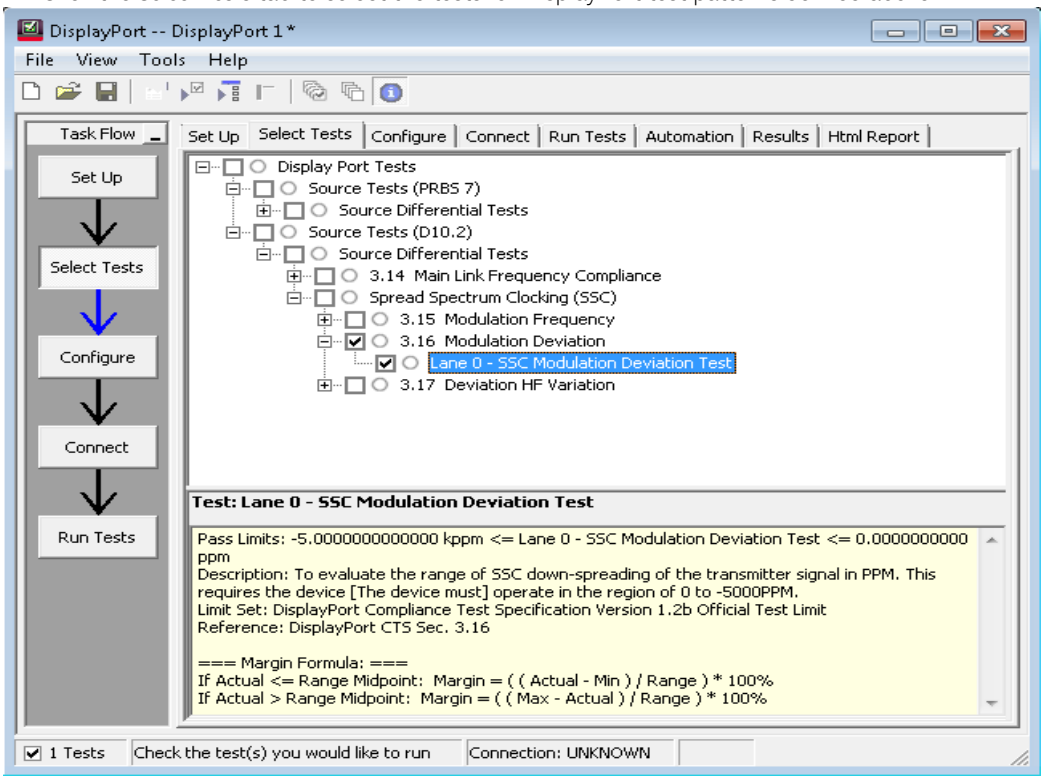


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.
5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.

9 Set up the parameters for SSC measurement.

a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.

b Acquire the signal with one complete SSC Cycle.

c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

Maximum Data Rate = 1/Minimum Unit Interval

d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

Minimum Data Rate = 1/Maximum Unit Interval

e Repeat steps b, c and d until you acquire 10 SSC Cycles.

f Calculate the mean value for the maximum and minimum data rate.

10 Calculate the SSC Modulation Deviation using the equation:

SSC Modulation Deviation = (Maximum Data Rate - Minimum Data Rate) / (Nominal Data Rate) * 1E6

11 Report the measurement results.

PASS Condition

-5000ppm ≤ SSC Modulation Deviation ($Resultant_{SSC\ Range}$) ≤ 0ppm

Table 17 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.16*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

12200001 12200002 12200003 12200004 – SSC Deviation HF Variation Test (Informative)

Test Overview

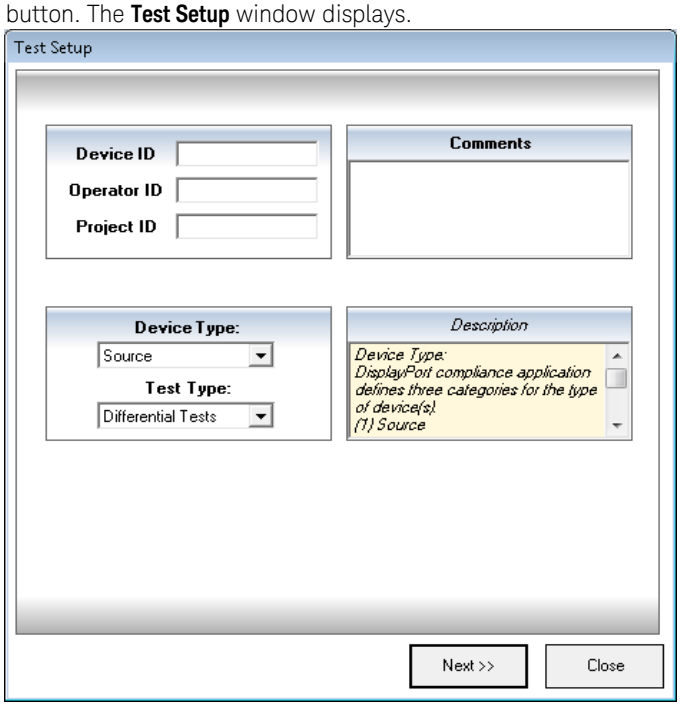
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



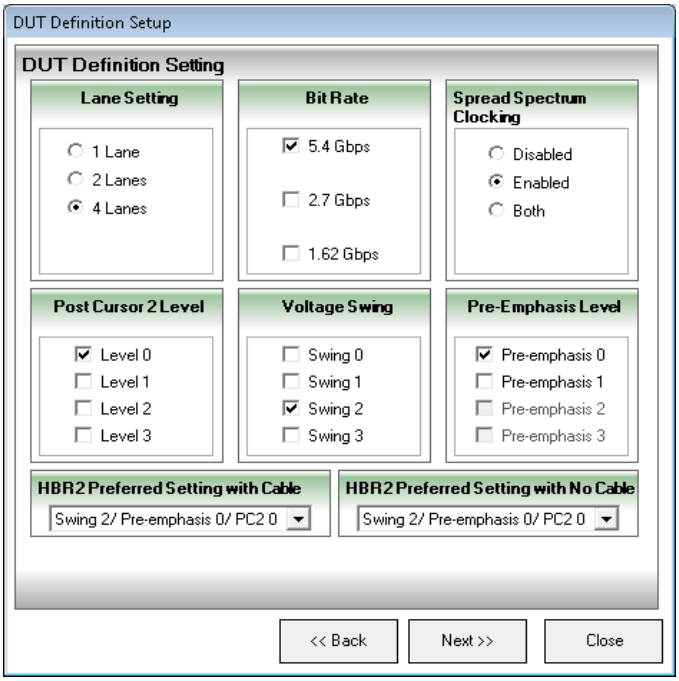
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

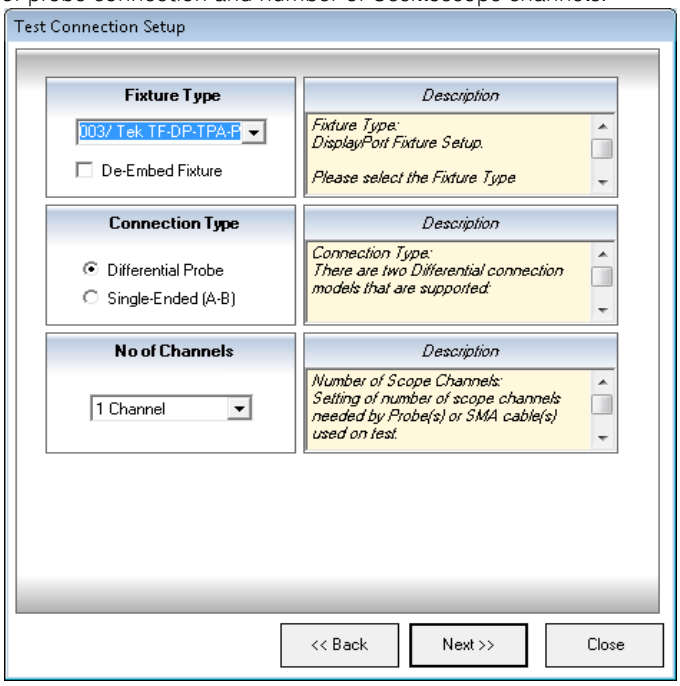
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

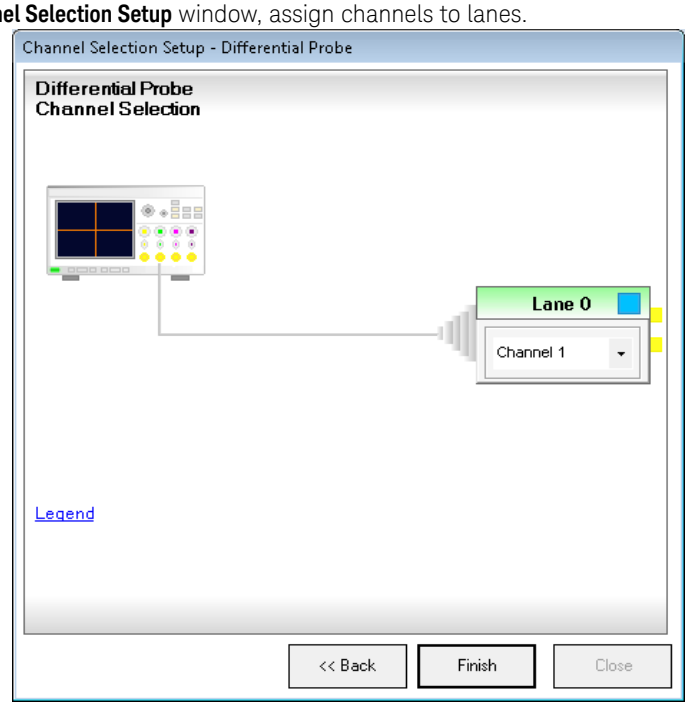
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Deviation HF Variation Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

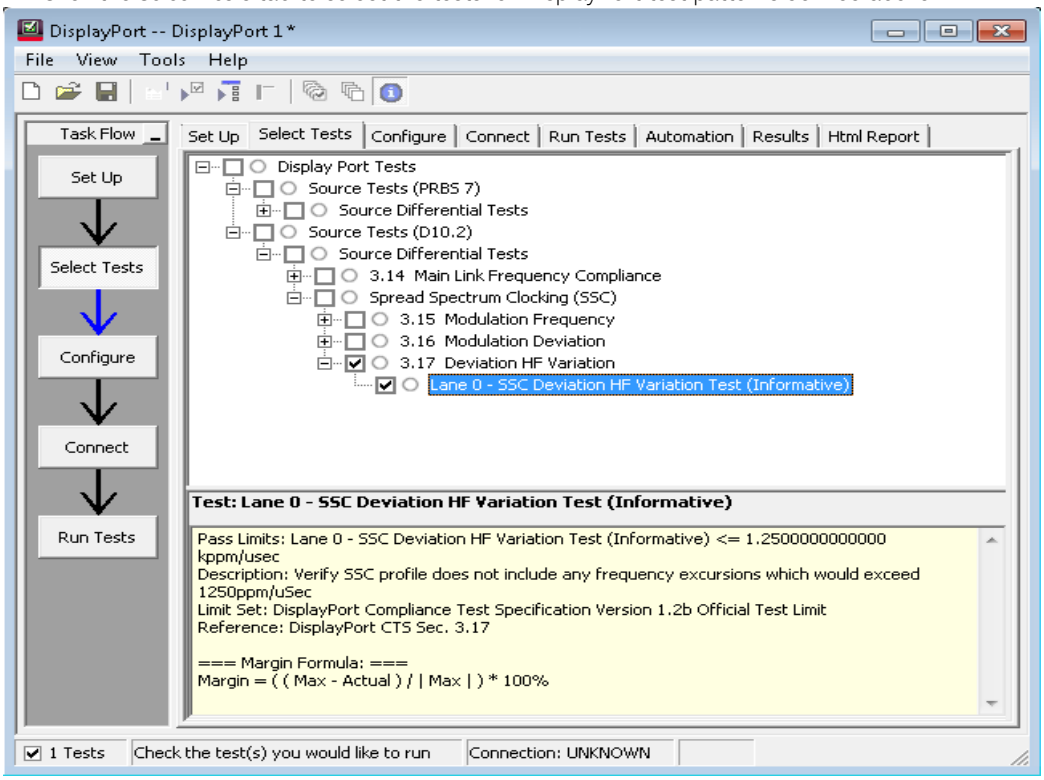


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
6 Set up the parameters for the SSC measurement.
   a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.
   b Acquire the signal with one complete SSC Cycles.
   c Read the FUNC2 filtered unit interval measurement trend.
   d Compute the slope using the “Sliding Window” with 1.00 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t\text{-}1.00\ \mu\text{sec})/1.00\ \mu\text{sec}$$

   e Repeat step b, c and d until you acquire 10 SSC Cycles.
   f Get the maximum value for the computed value of slope.
7 Report the measurement results.

PASS Condition

SSC_t dF/dt ≤ 1250ppm/µsec

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.17*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Post-Cursor 2 Verification Test (Informative)

Test ID

1279001 1279002 1279003 1279004 — Post Cursor 2 Verification Test - Level 1/Level 0 (Informative)

1279101 1279102 1279103 1279104 — Post Cursor 2 Verification Test - Level 2/Level 1 (Informative)

1279201 1279202 1279203 1279204 — Post Cursor 2 Verification Test - Level 3/Level 2 (Informative)

Test Overview

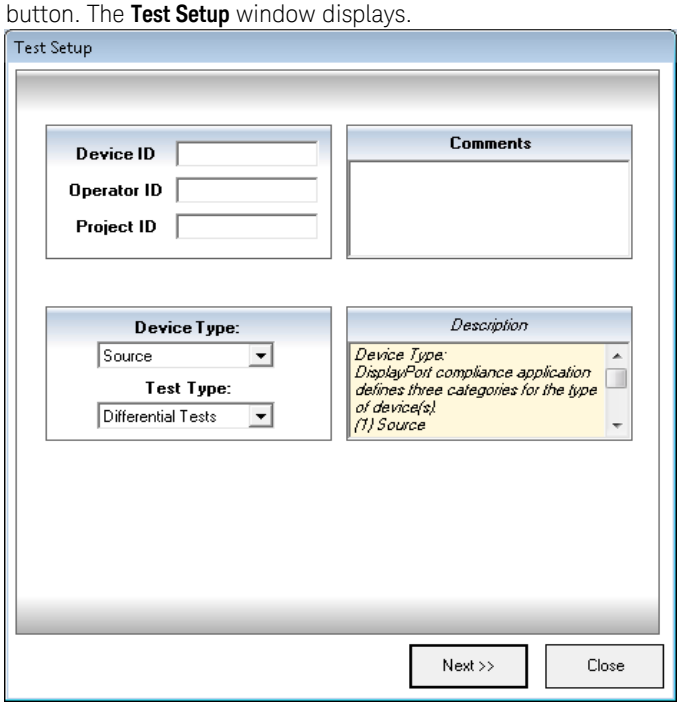
The objective of this test is to evaluate the effect of adding Post-Cursor 2 of the source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor 2 settings.

Test Conditions for Post Cursor 2 Verification Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	All Post-Cursor 2 levels supported
Test Lane	All test lanes are supported
Test Pattern	PCTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



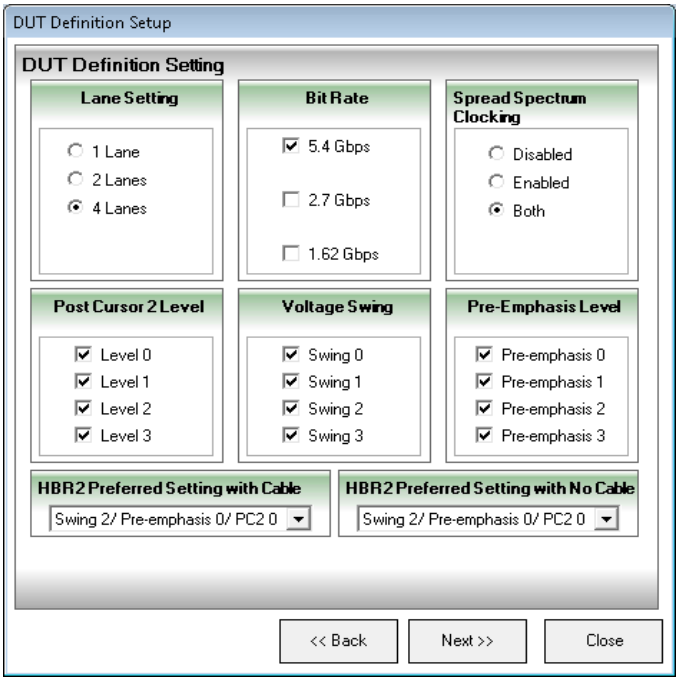
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

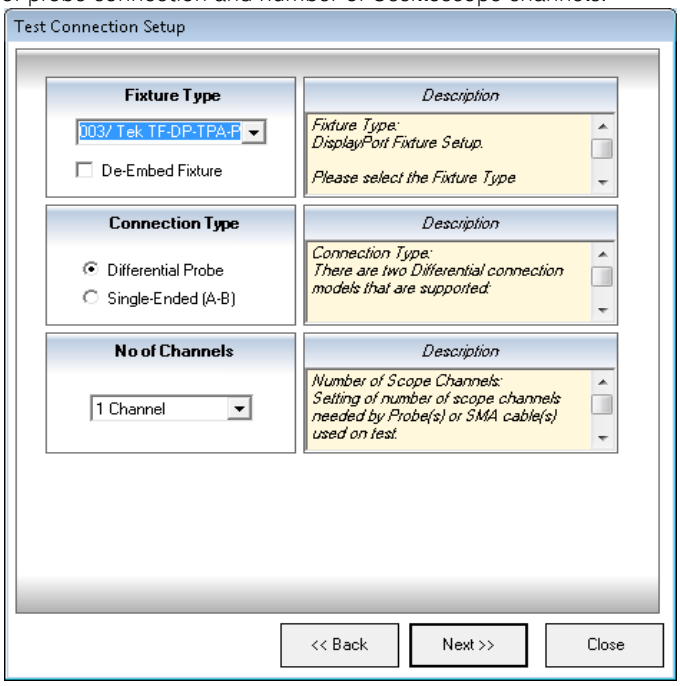
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

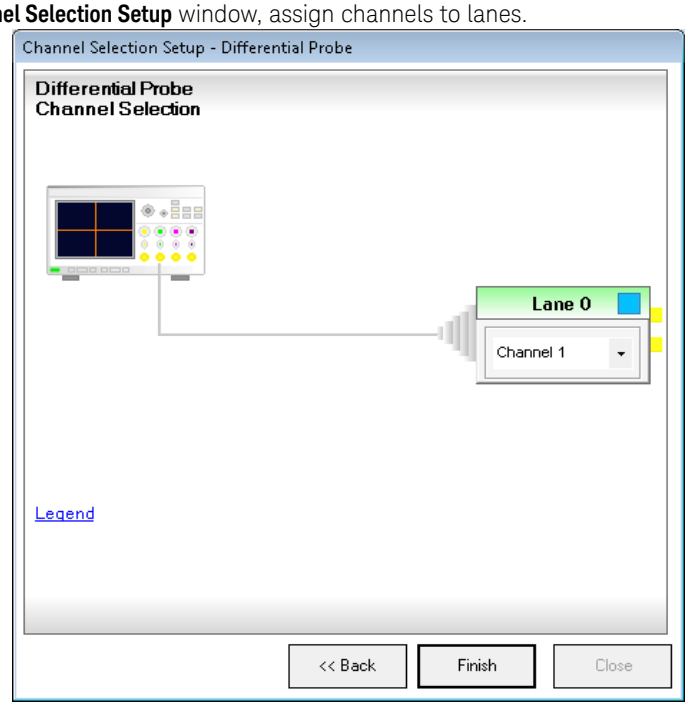
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Post Cursor 2 Verification Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

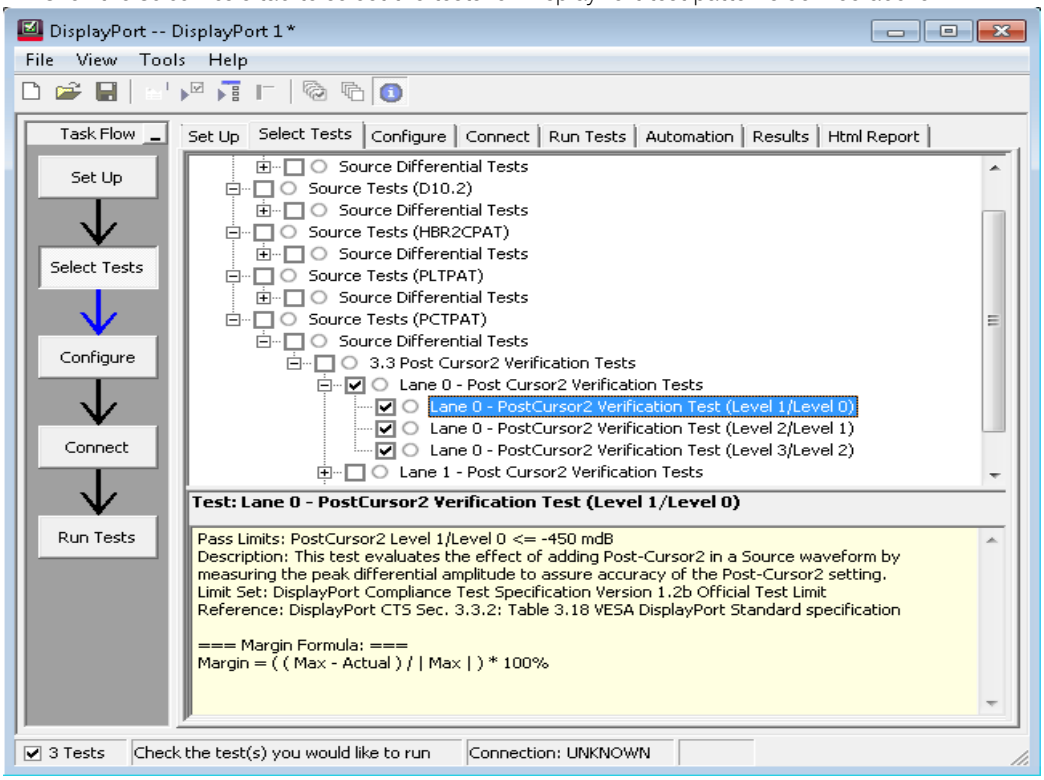


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level, Pre-Emphasis Level and Post-Cursor 2 Level X:
   a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   b Acquire and verify the input signal:
      i Verify the trigger and the amplitude of the input signal.
      ii Scale the vertical display of the input signal to optimum value.
      iii Measure V_{TOP} and V_{BASE} of the input signal.
      iv Measure the data rate of the input signal.
   c Set up the parameter of the measurement:
      i Enable measurement of all edges to obtain a statistical value of the measurement.
      ii Set up the measurement threshold.
      iii Set up the Clock Recovery as described in the section “Clock Recovery”.
   d Pattern fold the input signal based on the qualifying pattern 00101010 for the measurement of voltage $V_{T1010\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.
   e Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1010\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1010\_PC2\_LvlX\_L}$.
      i $V_{T1010\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1010 portion of the qualifying pattern.
      ii $V_{T1010\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1010 portion of the qualifying pattern.
   f Calculate the peak-to-peak voltage $V_{T1010\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1010\_PC2\_LvlX\_PP} = V_{T1010\_PC2\_LvlX\_H} - V_{T1010\_PC2\_LvlX\_L}$$

   g Pattern fold the input signal based on the qualifying pattern 00011001100 for the measurement of voltage $V_{T1100\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.
   h Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1100\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1100\_PC2\_LvlX\_L}$.
      i $V_{T1100\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1100 portion of the qualifying pattern.
      ii $V_{T1100\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1100 portion of the qualifying pattern.
   i Calculate the peak-to-peak voltage $V_{T1100\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1100\_PC2\_LvlX\_PP} = V_{T1100\_PC2\_LvlX\_H} - V_{T1100\_PC2\_LvlX\_L}$$

   j Calculate the Post-Cursor 2 ratio using the equation:

$$\text{Post-Cursor 2 Ratio}_{LvlX} = V_{T1100\_PC2\_LvlX\_PP} / V_{T1010\_PC2\_LvlX\_PP}$$

2 Compare the pre-emphasis delta of Post-Cursor 2 Level with the limits by repeating Step 1 with another Post-Cursor2 Level.
3 Calculate the pre-emphasis delta of Post-Cursor 2 Level using the equation:

$$\text{Post-Cursor 2 Delta (Level 1 vs Level 0)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl1} / \text{Post-Cursor 2 Ratio}_{Lvl0}]$$

$$\text{Post-Cursor 2 Delta (Level 2 vs Level 1)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl2} / \text{Post-Cursor 2 Ratio}_{Lvl1}]$$

$$\text{Post-Cursor 2 Delta (Level 3 vs Level 2)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl3} / \text{Post-Cursor 2 Ratio}_{Lvl2}]$$

4 Report the measurement results.

PASS Condition

Post Cursor 2 Verification Measurements

For Level 1 vs. Level 0 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl0\_to\_Lvl1} \leq -0.45$ dB

For Level 2 vs. Level 1 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl1\_to\_Lvl2} \leq -0.5$ dB

For Level 3 vs. Level 2 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl2\_to\_Lvl3} \leq -0.6$ dB

Table 18 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX-PREEMP\_POST2-DELTA}$	Delta of Pre-emphasis Post Cursor2 Level 1 vs. Level 0	-0.45	-	-	dB	Measured on 2nd T_{BIT} at Pre-emphasis Level 0
	Delta of Pre-emphasis Post Cursor2 Level 2 vs. Level 1	-0.5	-	-	dB	Support for Pre-emphasis Post Cursor2 is optional
	Delta of Pre-emphasis Post Cursor2 Level 3 vs. Level 2	-0.6	-	-	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2a, Section 3.3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis delta of Post-Cursor 2 for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Eye Diagram Test (TP3_EQ)

Test ID

For HBR:

- 1211001, 1211002, 1211003, 1211004 – Eye Diagram Test (TP3_EQ) - PRBS7
- 1211011, 1211012, 1211013, 1211014 – Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS7

For HBR2:

- 1215001, 1215002, 1215003, 1215004 – Eye Diagram Test (TP3_EQ) - HBR2CPAT
- 1215011, 1215012, 1215013, 1215014 – Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT

Test Overview

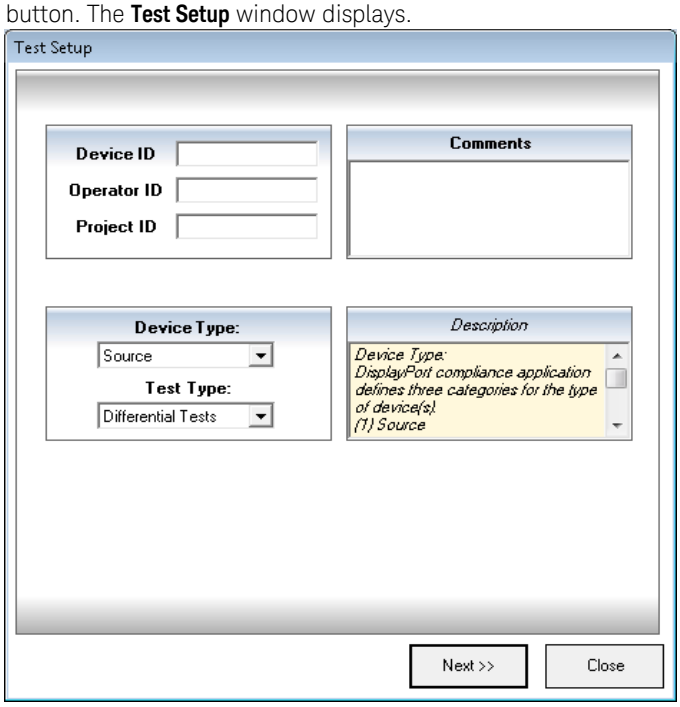
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	HBR – Level 2 HBR2 – Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	HBR–PRBS7 HBR2–HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



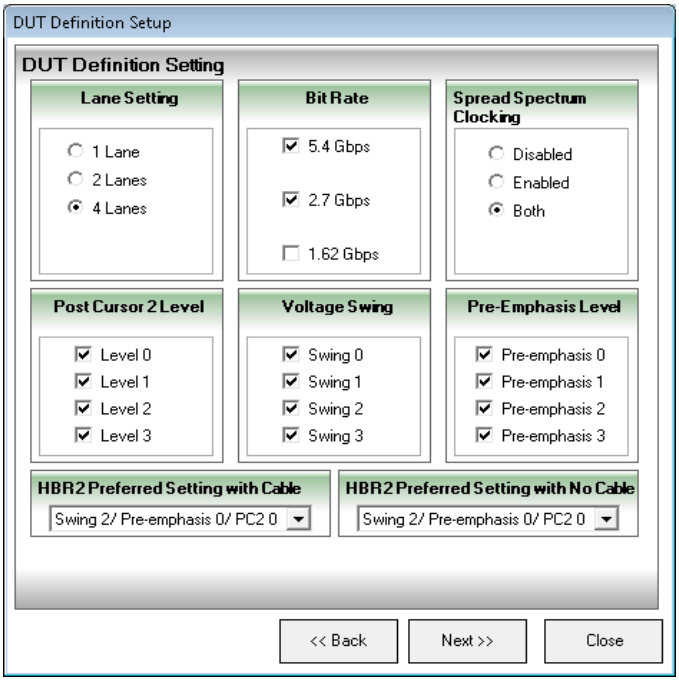
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

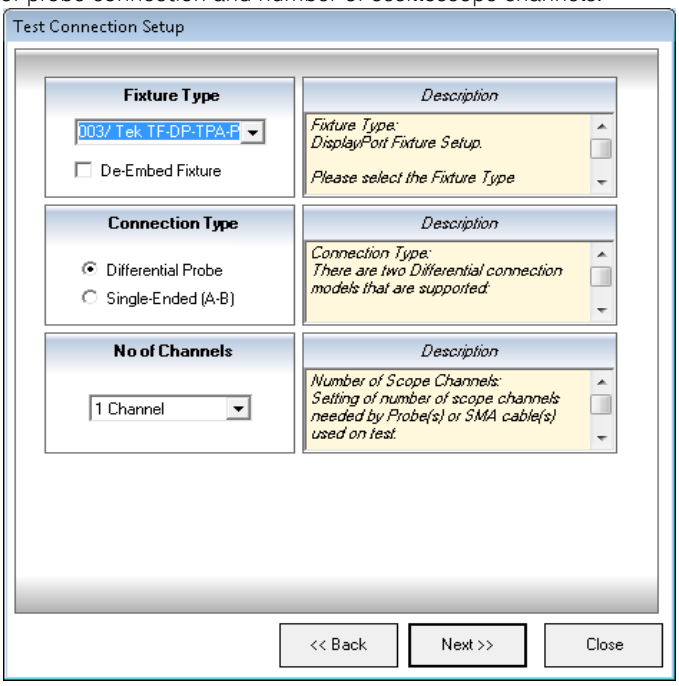
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

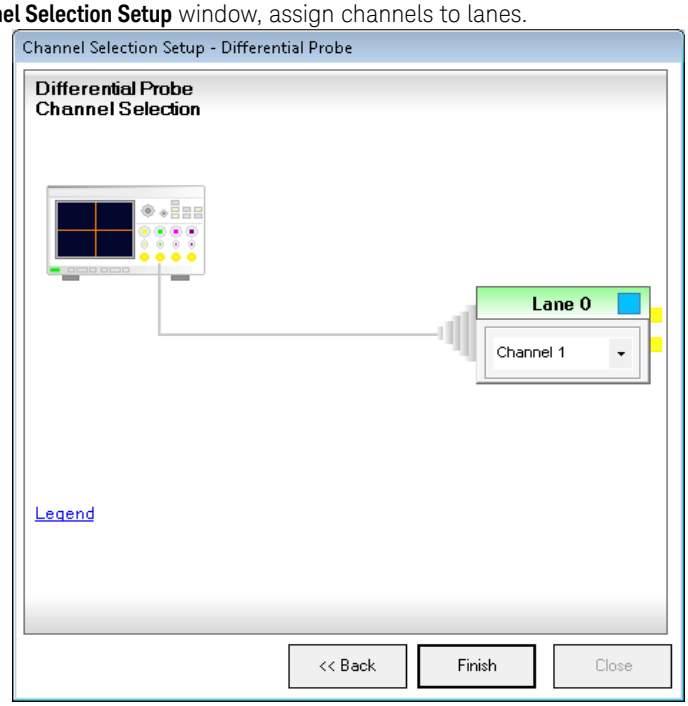
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

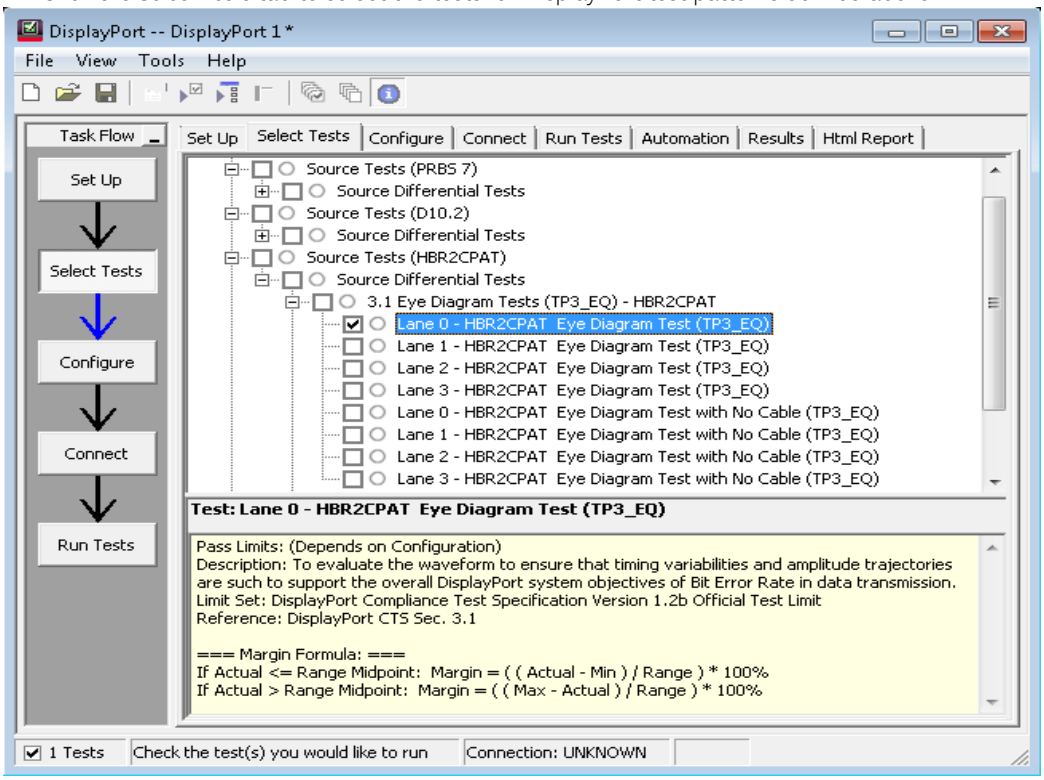


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure for HBR

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.

4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 1,000,000 edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If you select more than one lane (2 lanes or 4 lanes DUT configuration), the eye mask height and width is derate in the following manner, to include crosstalk as defined in DisplayPort 1.2b Compliance Test Specification:
      i Eye Mask Width Derate (Crosstalk) = 0.04 UI
      ii Eye Mask Height Derate (Crosstalk) = 0.014V
   b If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification (0.38 UI) + Eye Mask Width Derate (Crosstalk) + 2 * Eye Mask Width Derate (Random Jitter)

e Calculate the Eye Mask Height:

V_{HIGH} Eye Mask Height = {Eye Height Specification (0.09 UI) + Eye Mask Height Derate (Crosstalk)}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

V_{LOW} Eye Mask Height = -{Eye Height Specification (0.09 UI) + Eye Mask Height Derate (Crosstalk)}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 1,000,000 UI are folded.

13 Measure the eye height of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 19 and Table 20 show the voltage and time coordinates for the mask used for the eye diagram.

Table 19 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

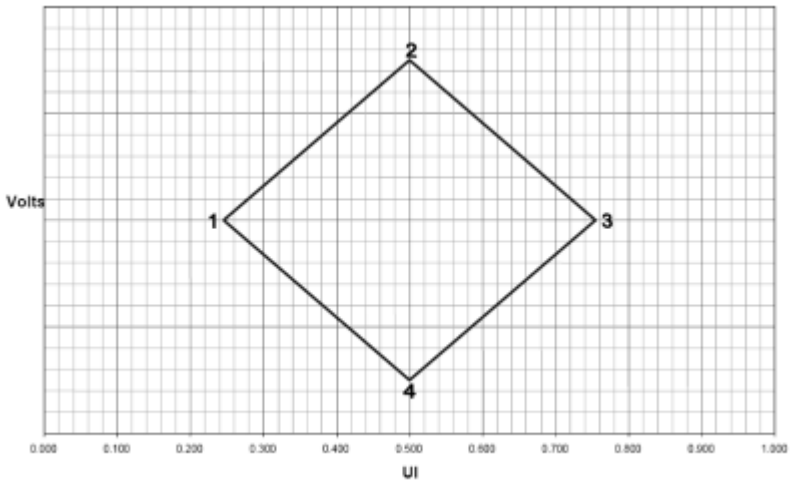


Figure 19 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 20 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045

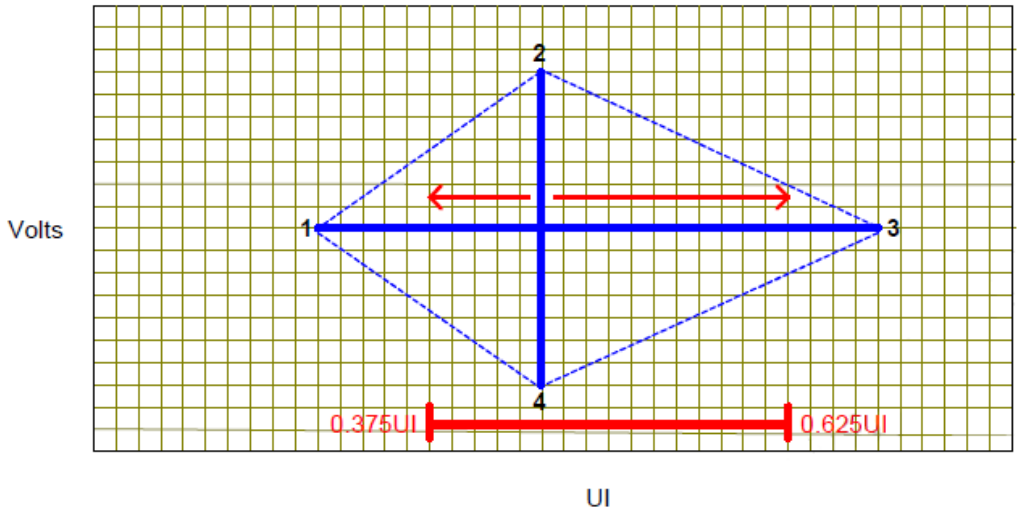


Figure 20 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test (TP3_EQ)

Test ID

For HBR2:

- 1222001, 1222002, 1222003, 1222004 – Total Jitter Test (TP3_EQ) - HBR2CPAT
- 1222011, 1222012, 1222013, 1222014 – Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1221001, 1221002, 1221003, 1221004 – Total Jitter Test (TP3_EQ) - D10.2
- 1221011, 1221012, 1221013, 1221014 – Total Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

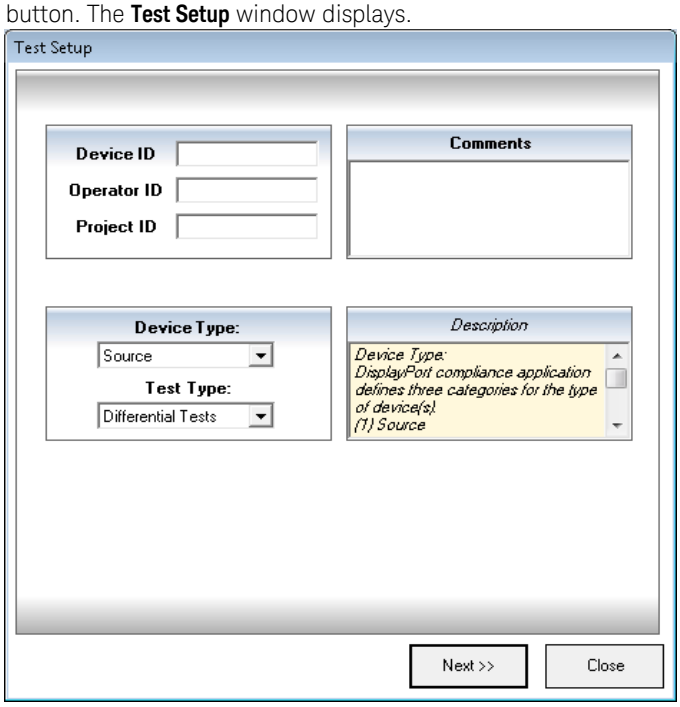
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



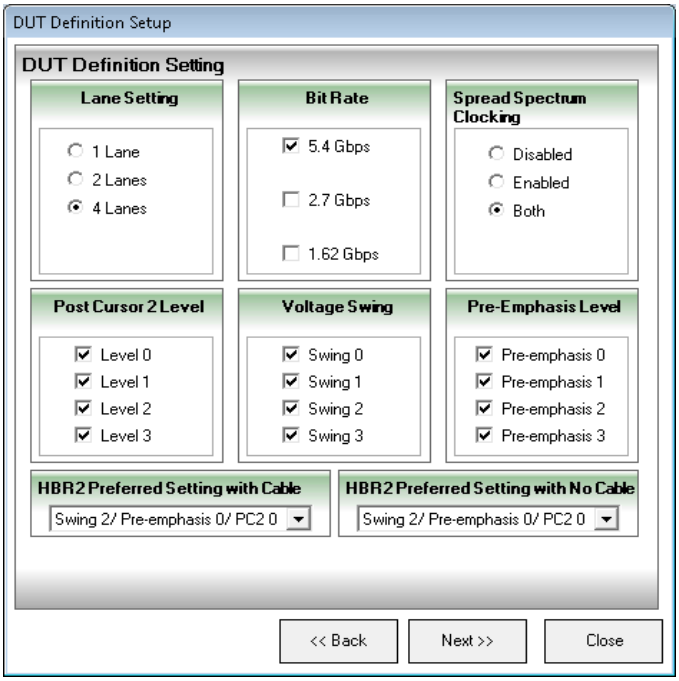
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

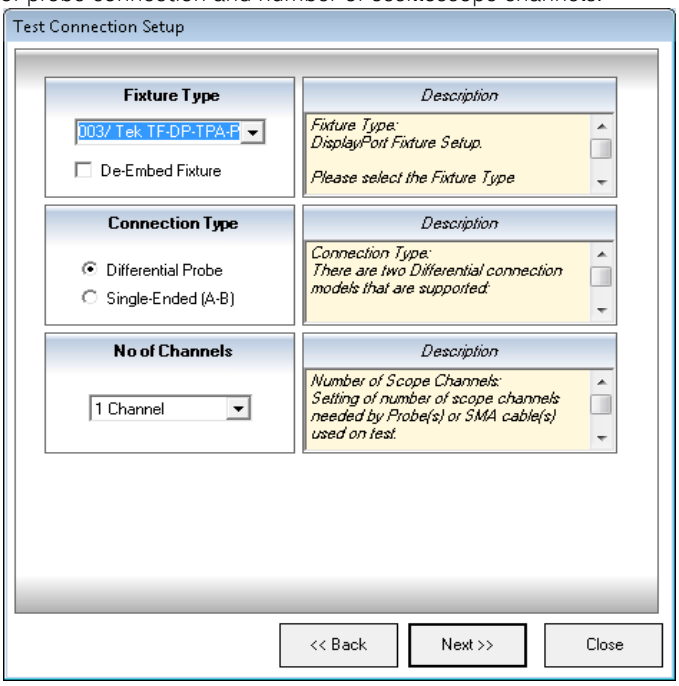
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

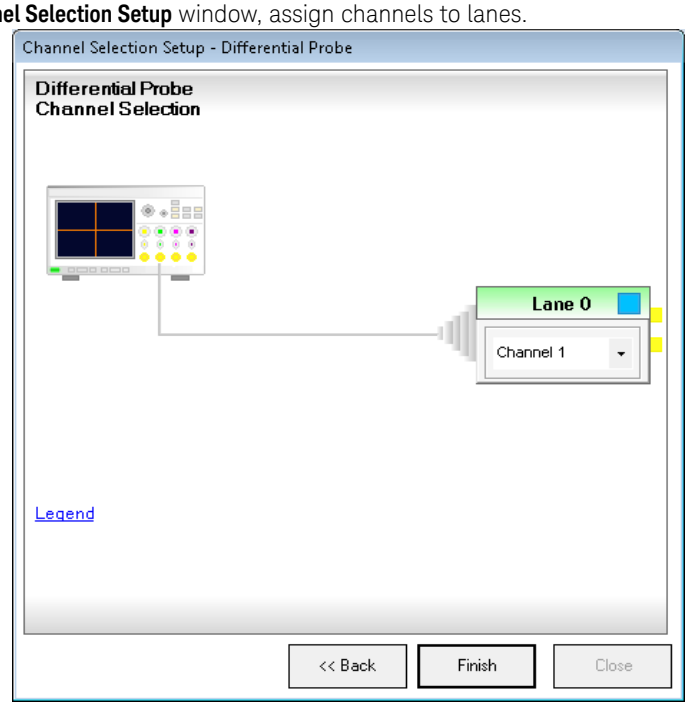
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

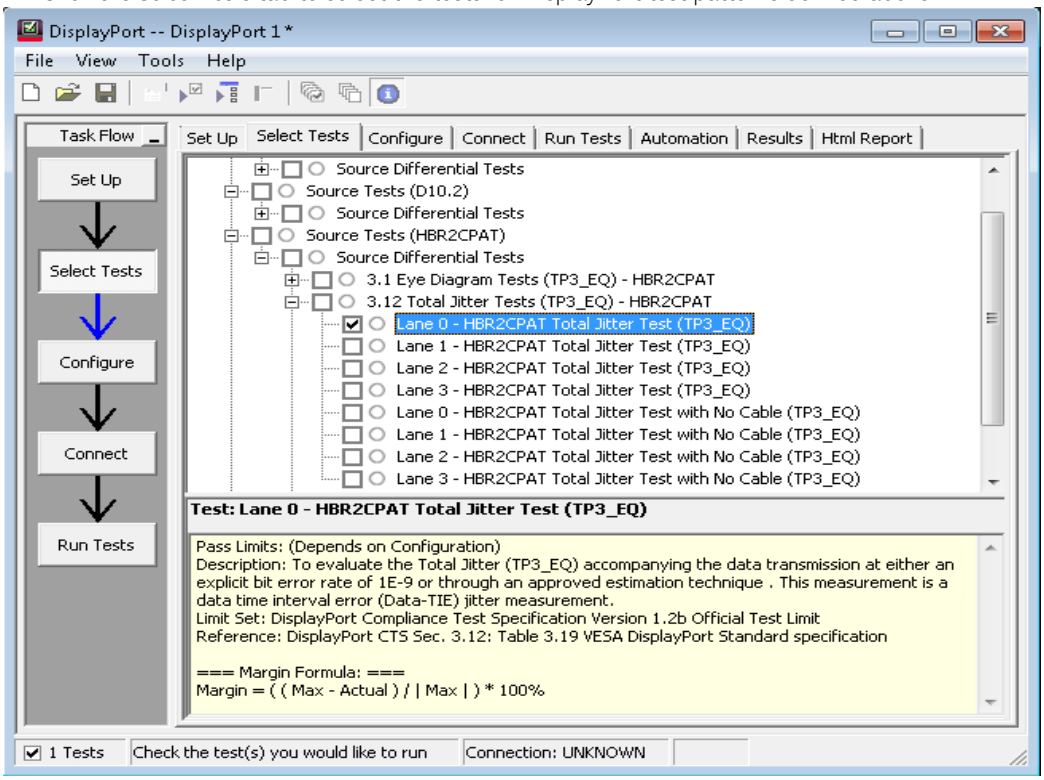


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 21 Total Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 22 Total Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.40 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Deterministic Jitter Test (TP3_EQ)

Test ID

- 1236001, 1236002, 1236003, 1236004 – Deterministic Jitter Test (TP3_EQ) - HBR2CPAT
- 1236011, 1236012, 1236013, 1236014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1235001, 1235002, 1235003, 1235004 – Deterministic Jitter Test (TP3_EQ) - D10.2
- 1235011, 1235012, 1235013, 1235014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

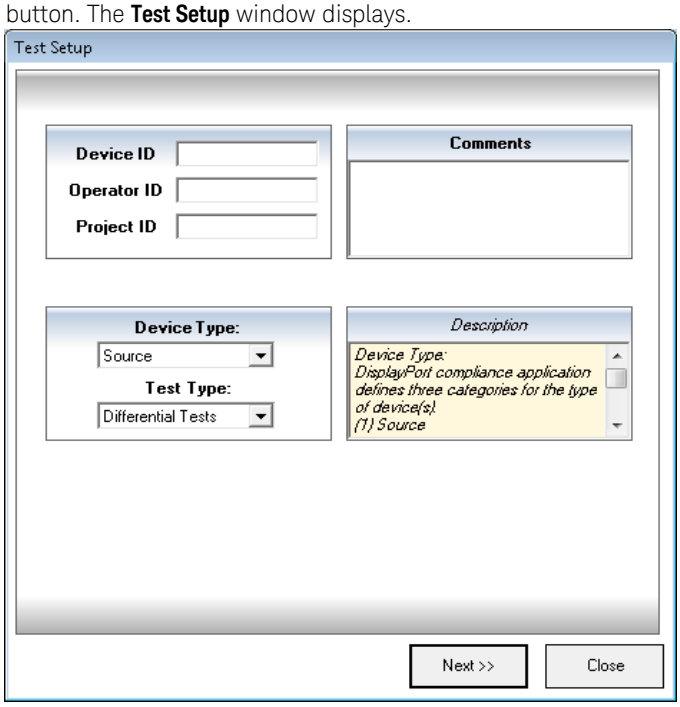
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



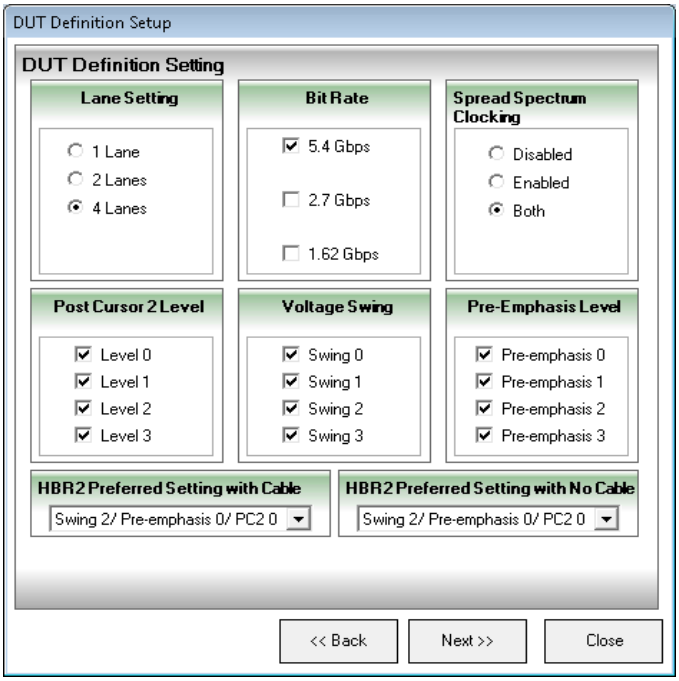
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

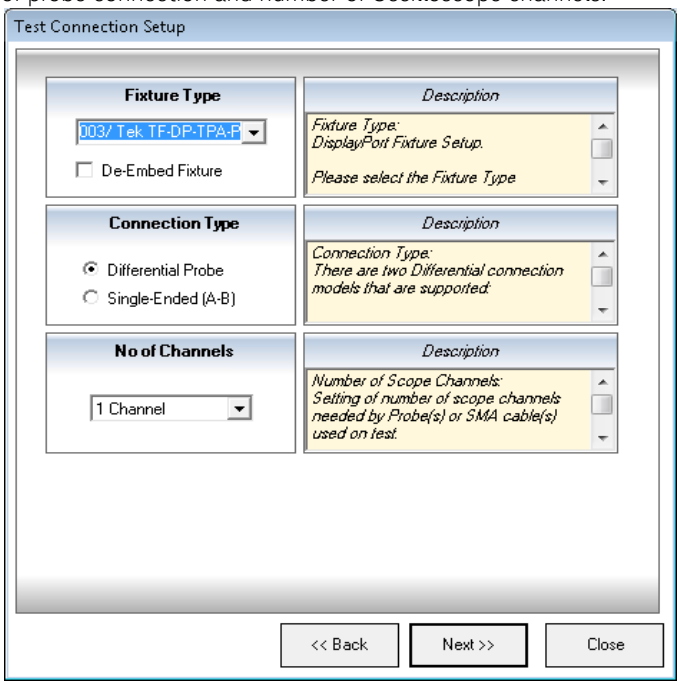
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

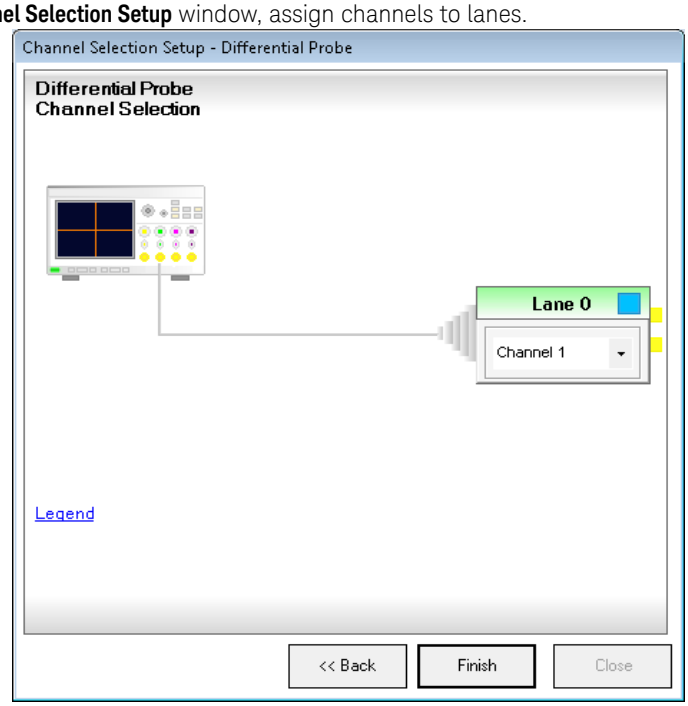
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Deterministic Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

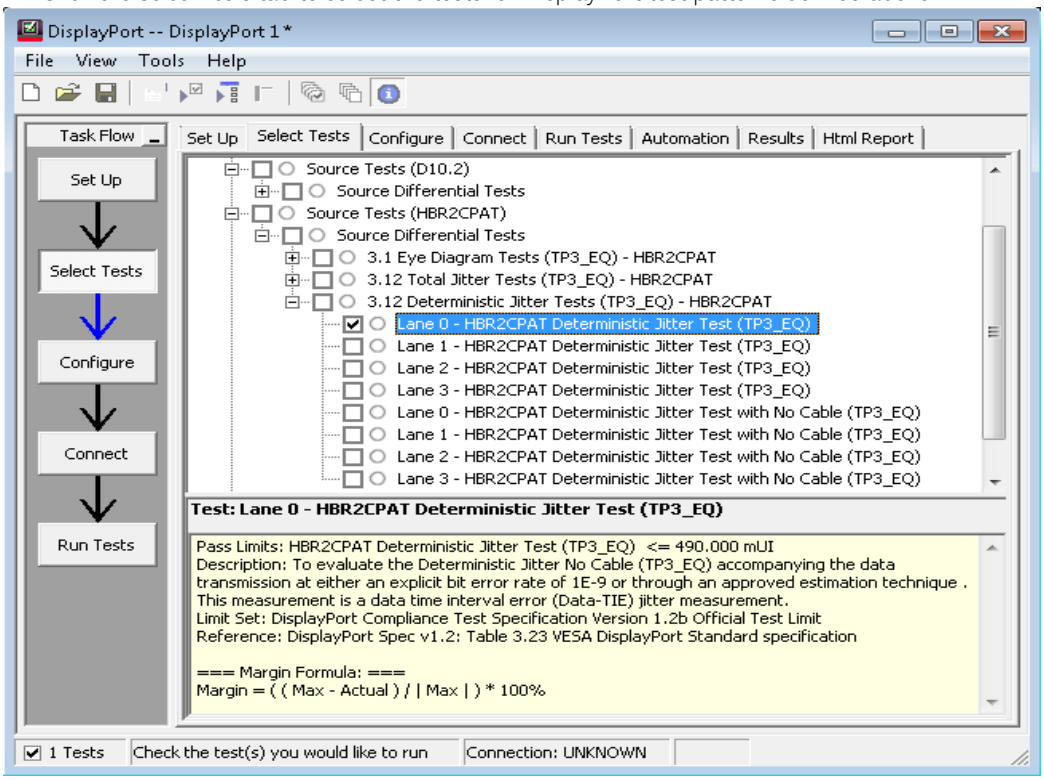


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 23 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 24 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.25 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Random Jitter Test (TP3_EQ)

Test ID

- 1238001, 1238002, 1238003, 1238004 — Random Jitter Test (TP3_EQ) - D10.2
- 1238011, 1238012, 1238013, 1238014 — Random Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

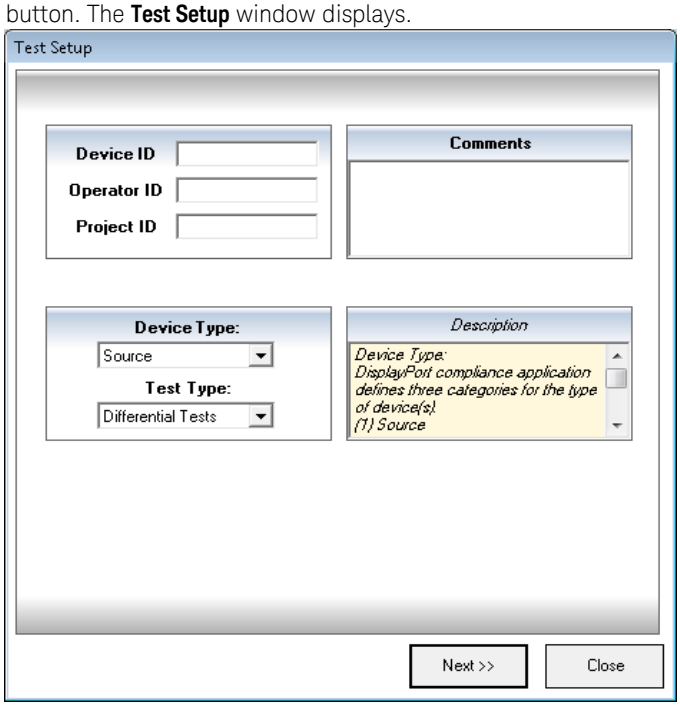
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes are supported
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



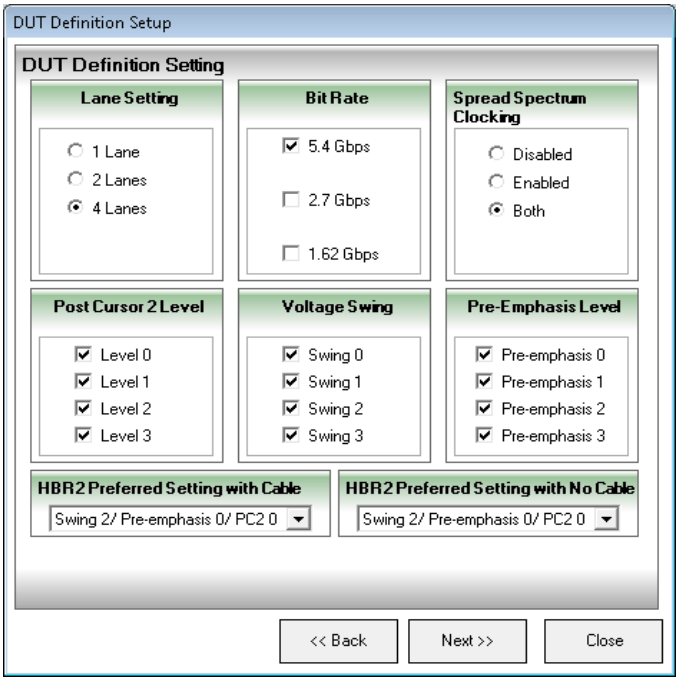
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

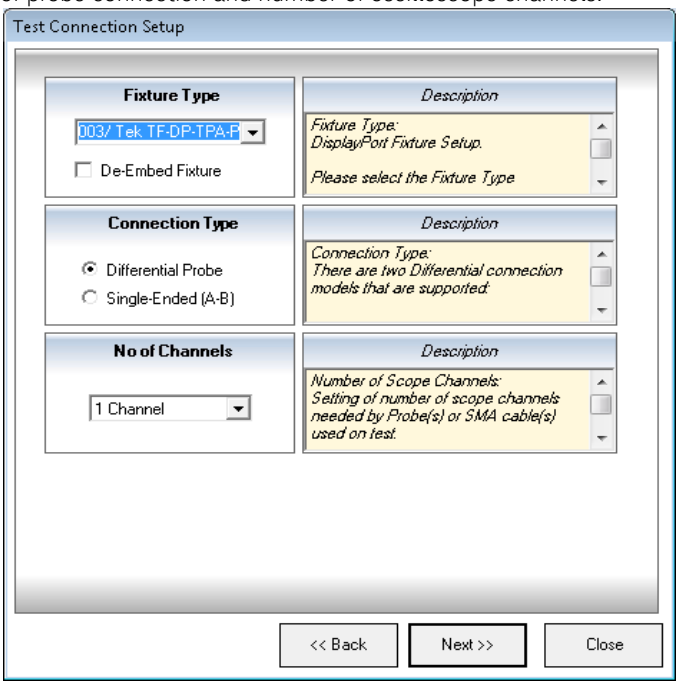
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

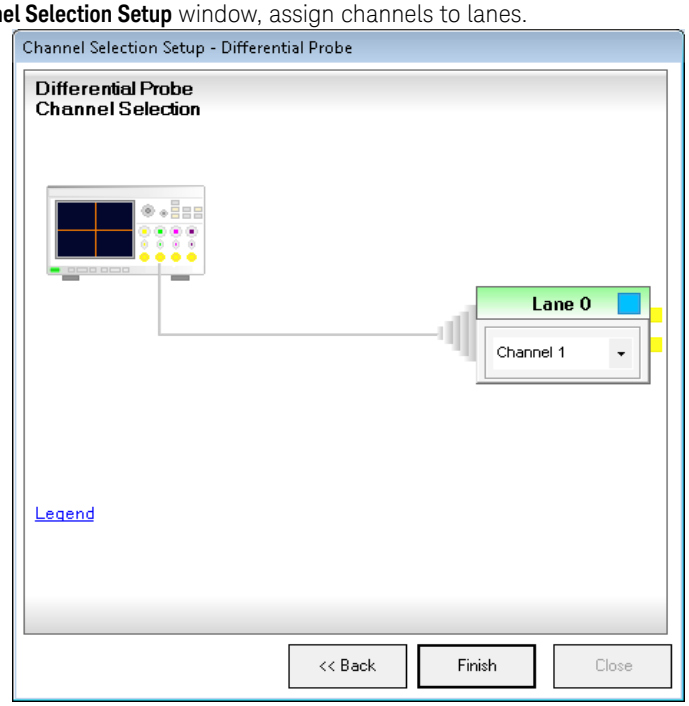
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Random Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

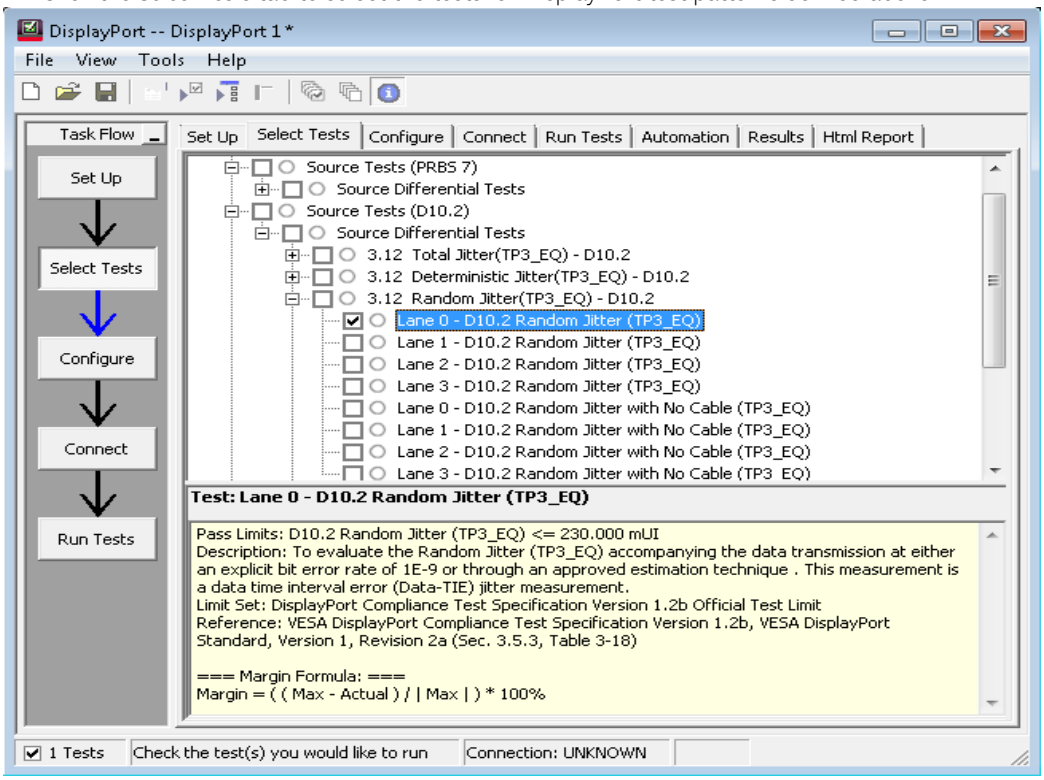


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 25 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.23 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative)

Test ID

12110001, 12110002, 12110003, 12110004 – AC Common Mode Test (Informative)

Test Overview

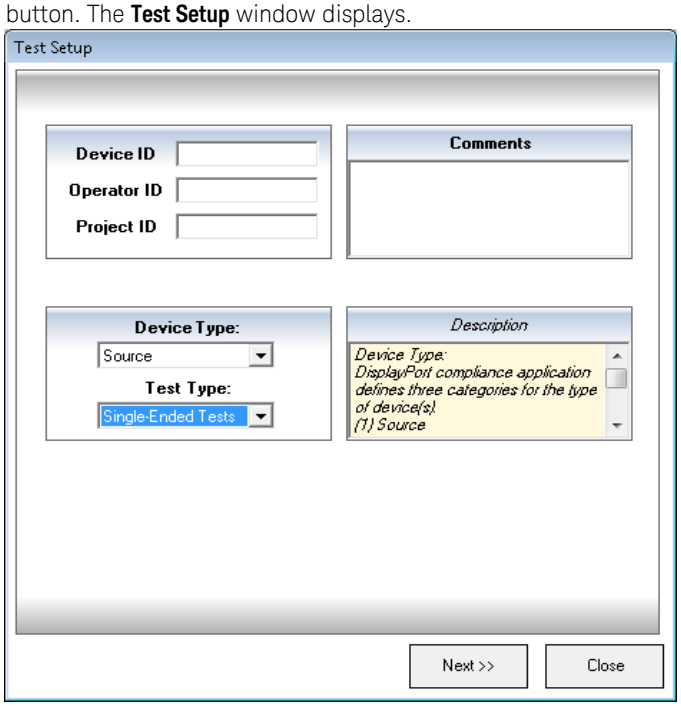
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis level supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



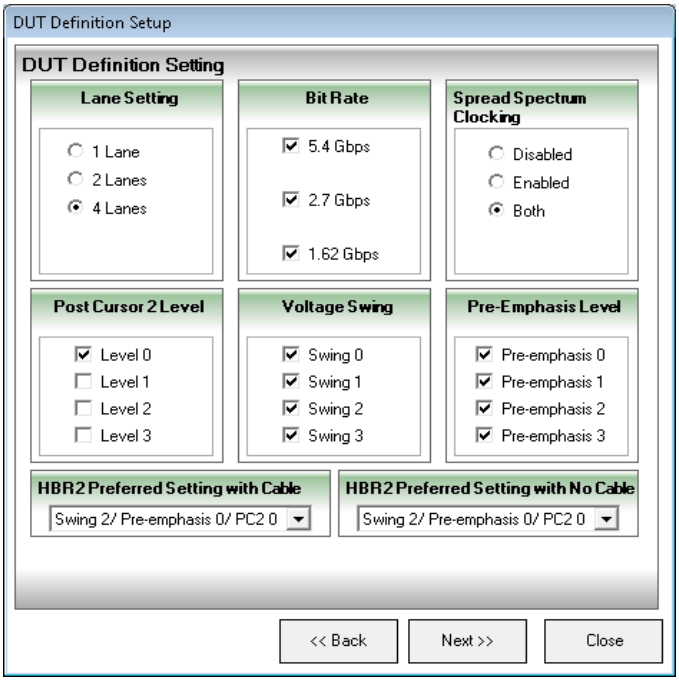
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

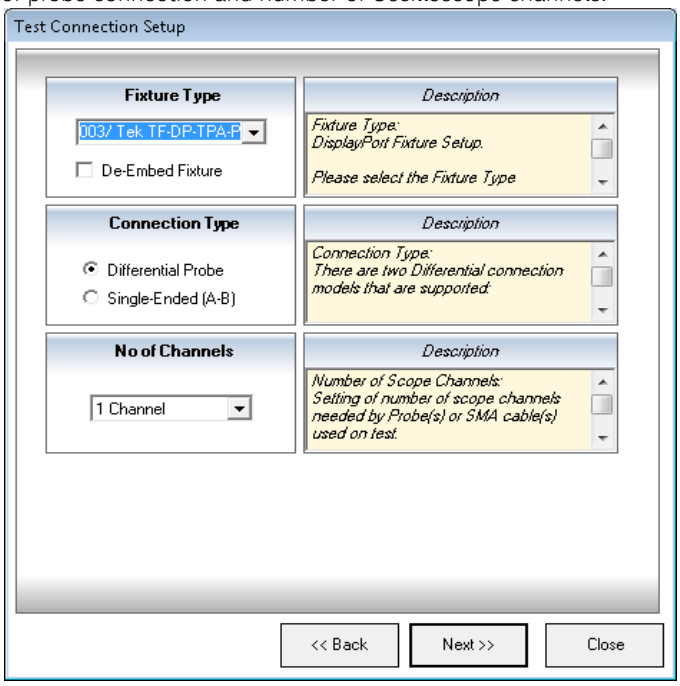
b Select **Device Type:** as **Source**, **Test Type:** as **Single-Ended Tests**.

c Click **Next**.

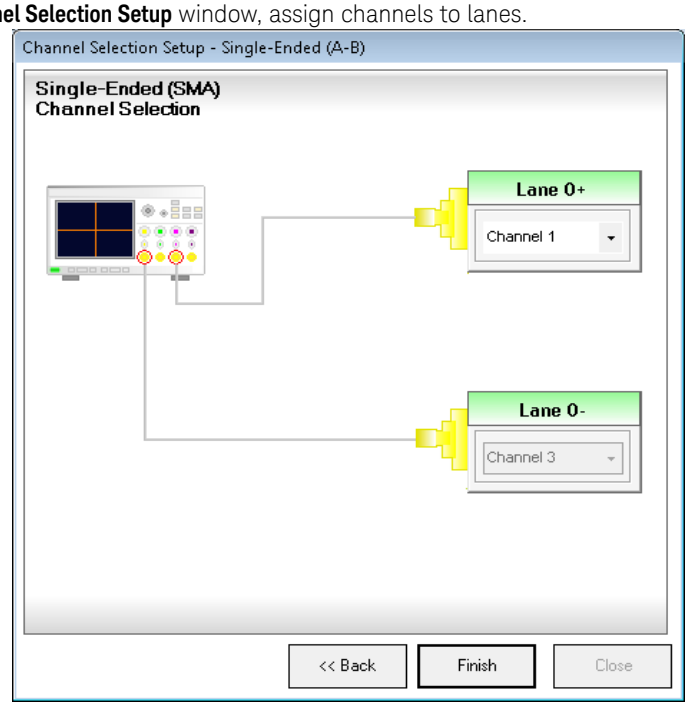
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for AC Common Mode Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

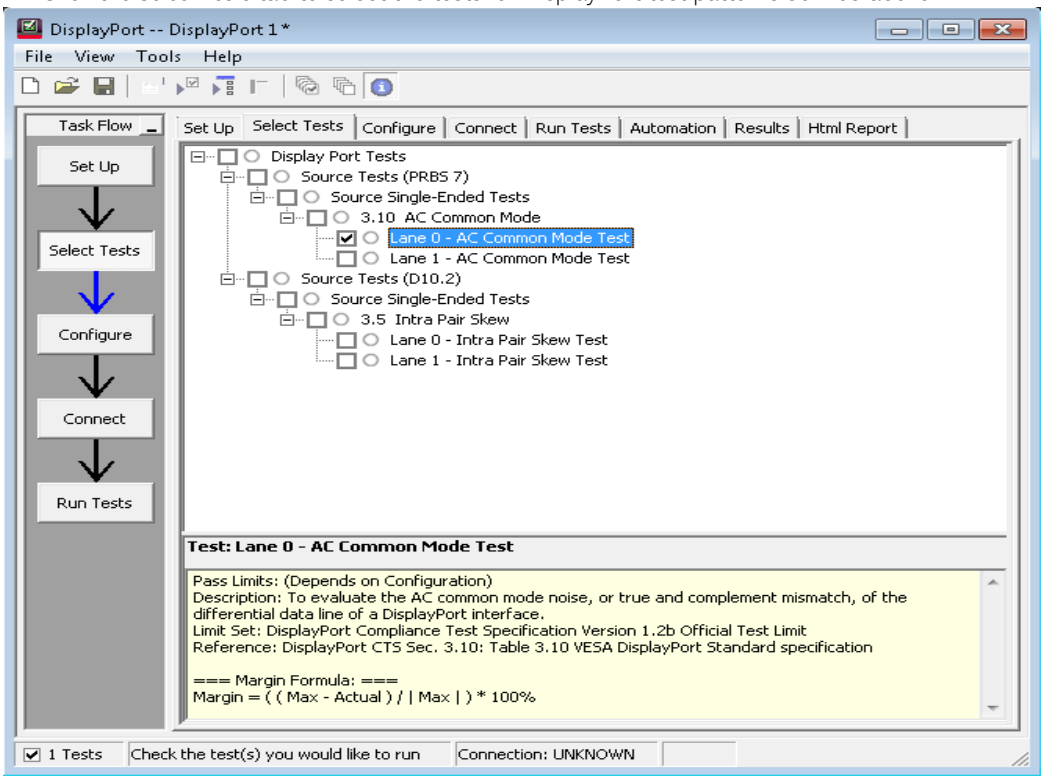


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled ["Filter" configuration variable set to "High Pass Filter", "Low Pass Filter" or "None" (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.
8 Get the mean for the V_{rms} measurement.
9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.10*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 9.2, Table 9-6*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

Source Intra-Pair Skew Test (Informative)

Test ID

12100001, 12100002, 12100003, 12100004 — Intra-Pair Skew Test (Informative)

Test Overview

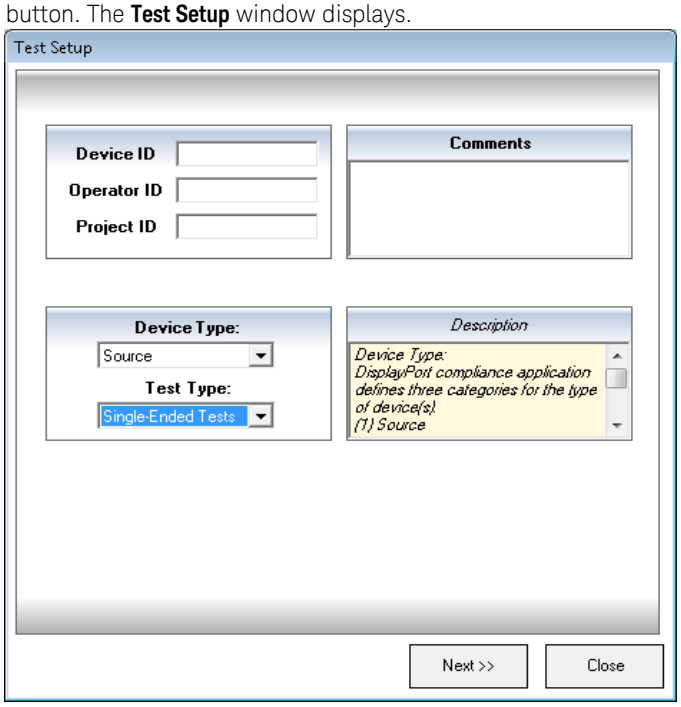
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported For one lane operation: Lane 0+ to Lane 0- For two lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- For four lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- Lane 2+ to Lane 2- Lane 3+ to Lane 3-
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



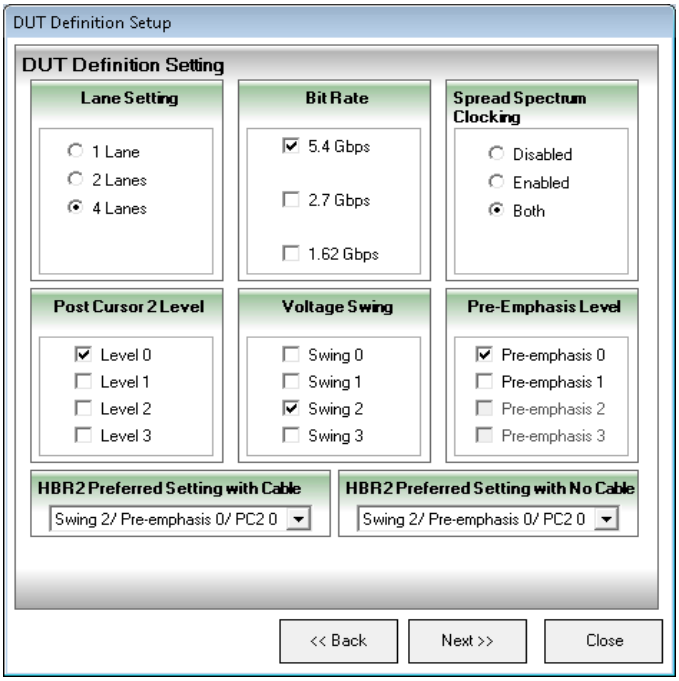
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

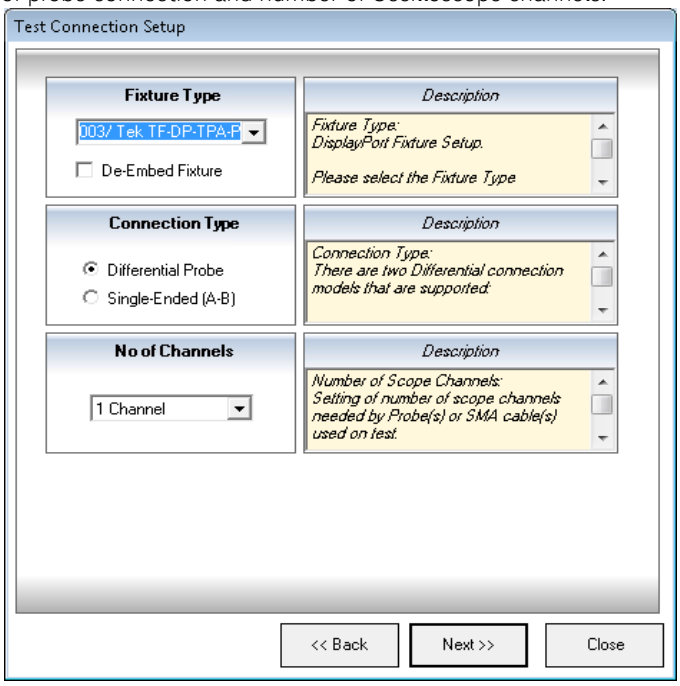
b Select **Device Type:** as **Source**, **Test Type:** as **Single-Ended Tests**.

c Click **Next**.

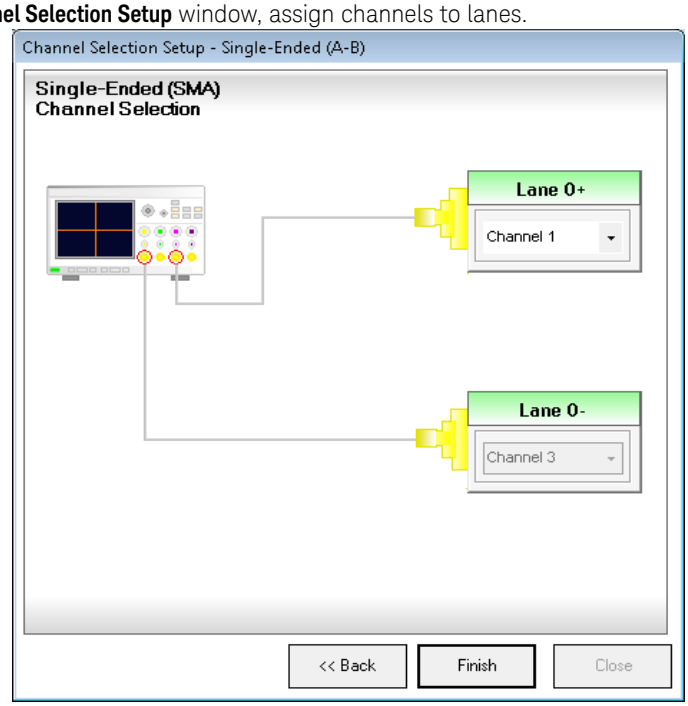
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Intra-Pair Skew Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

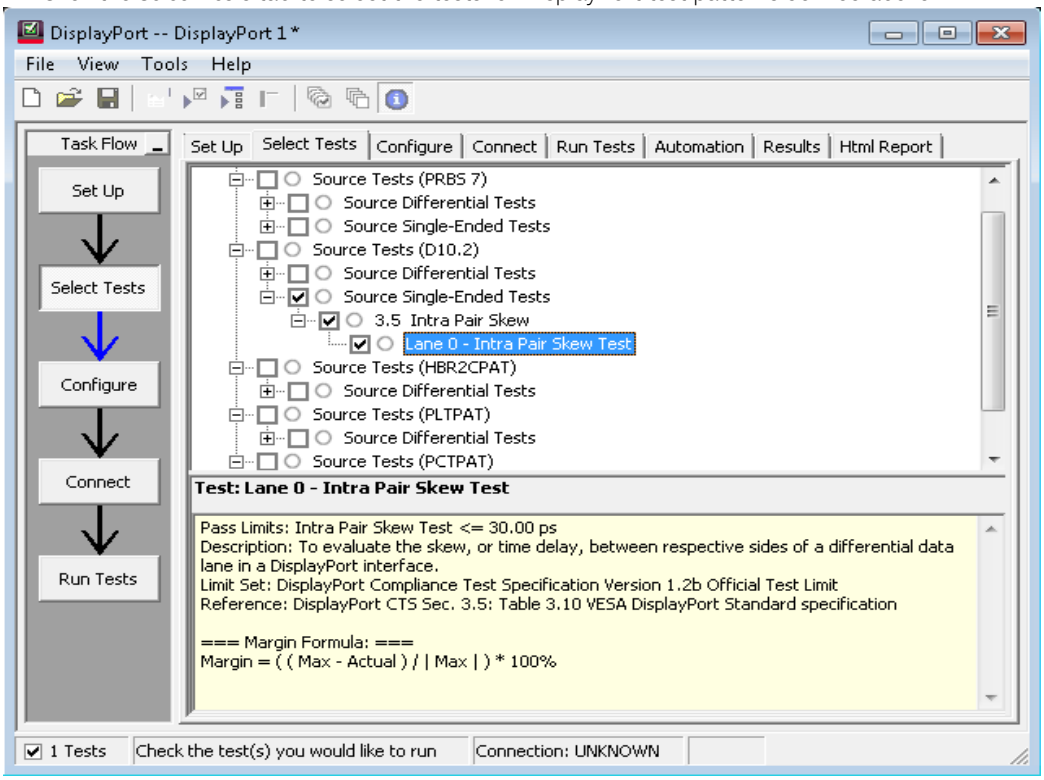


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Source Tests" on page 62 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find VHIGH by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find VLOW by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:
   a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.
   b Set up InfiniiScan to trigger on the desired pattern.
   c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

   d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

   e Acquire the signal until you measure 100 edges.
   f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra Pair Skew ≤ 30 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.5*

- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “Test References” section for this test.

4 DisplayPort 1.2 Sink Tests

Overview

Test Point Definition for DisplayPort 1.2 (1.2b) Sink Tests

NOTE Sink Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Sink DUT at Test Point 3(TP3) as shown in Figure 21. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

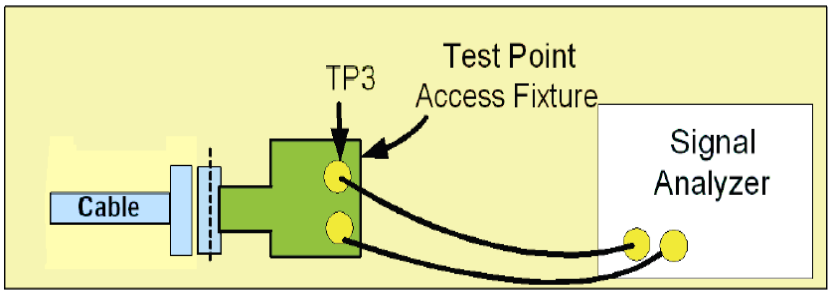


Figure 21 Test Point 3 Connection for DisplayPort 1.2 Sink Tests

Table 26 defines the test point fixtures and instruments used for DisplayPort 1.2 (1.2b) Sink Tests:

Table 26 Test Point Fixtures and Instruments for DisplayPort 1.2 Sink Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Calibration of Stress Signal

For the calibration of the stress signal, you must test the stress signal in the manner shown in the Figure 22 for RBR and Figure 23 for HBR and HBR2.

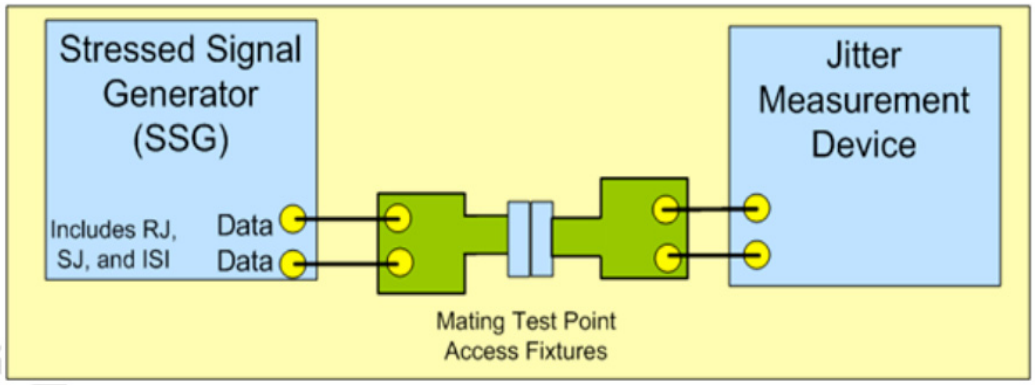


Figure 22 Test Point 3 Connection for Stress Signal Calibration of RBR

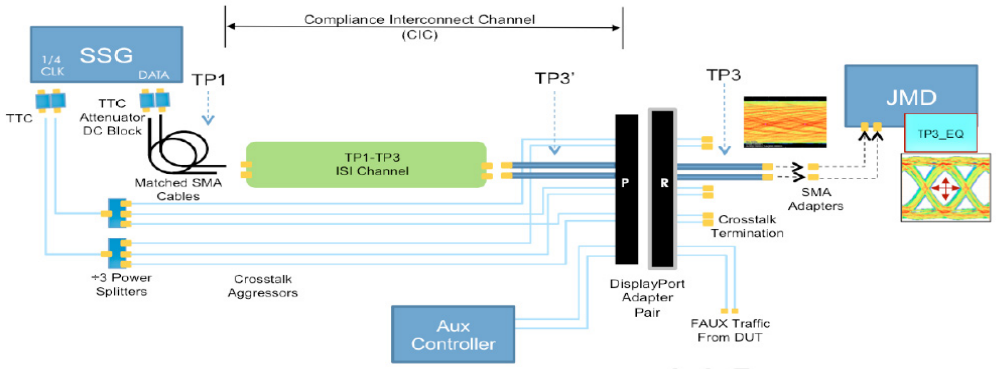


Figure 23 Test Point 3 Connection for Stress Signal Calibration of HBR and HBR2

Table 27 defines the Test Point 3 Connections for Stress Signal Calibration:

Table 27 Test Point Connections for Stress Signal Calibration

Test Requirement	Device Used
Stress Signal Generator (SSG)	Bit Error Rate Tester ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Jitter Measurement Device (JMD)	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Sink Tests

Perform the following steps before you run the compliance tests on the sink device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 24).

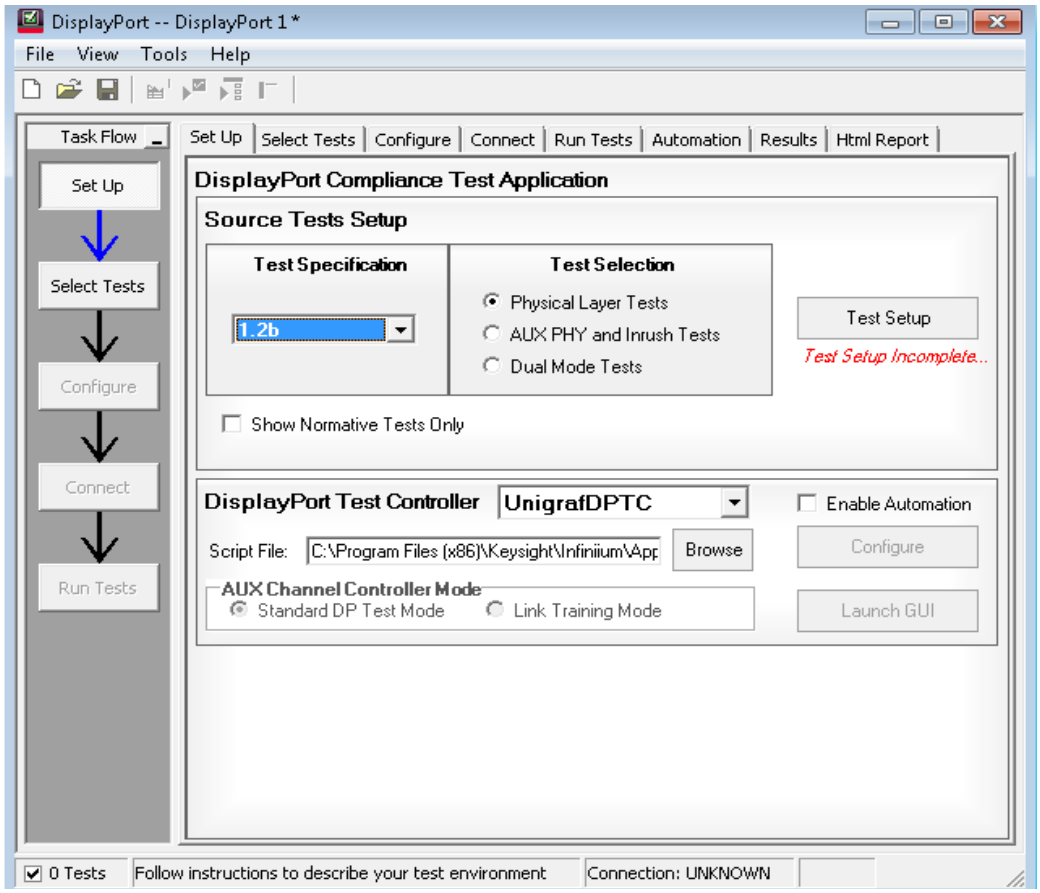


Figure 24 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.2b Standards, select **1.2b** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.2 Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

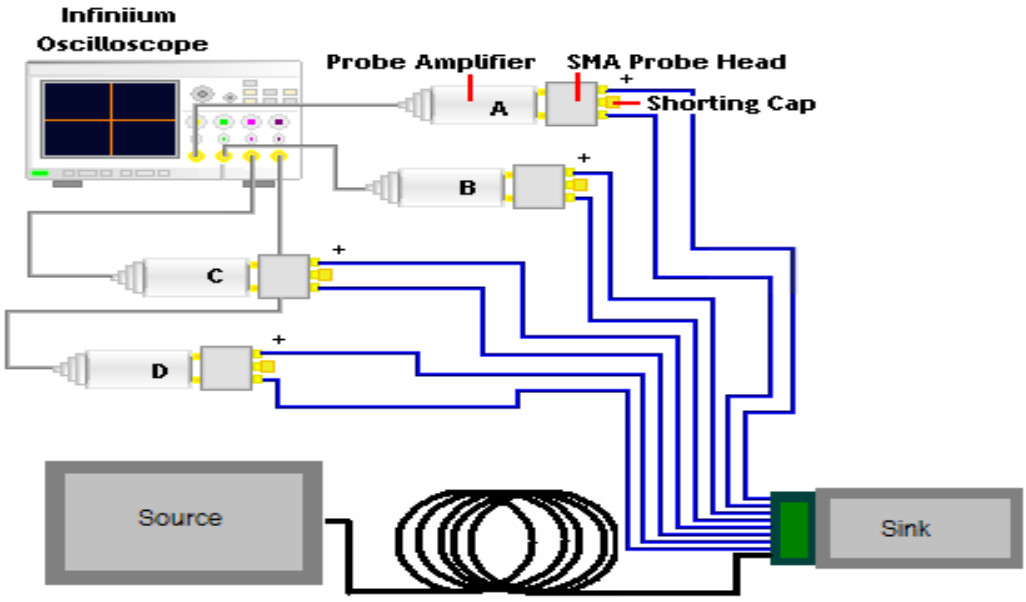


Figure 25 Sample connection diagram for DisplayPort 1.2 Sink Tests

Sink Eye Diagram Test

Test ID

12140001, 12140002, 12140003, 12140004 – Sink Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a)

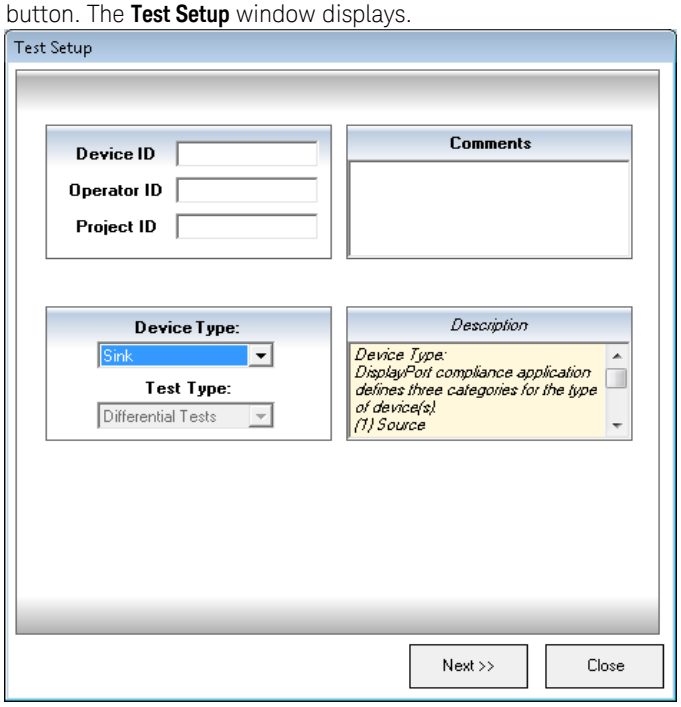
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



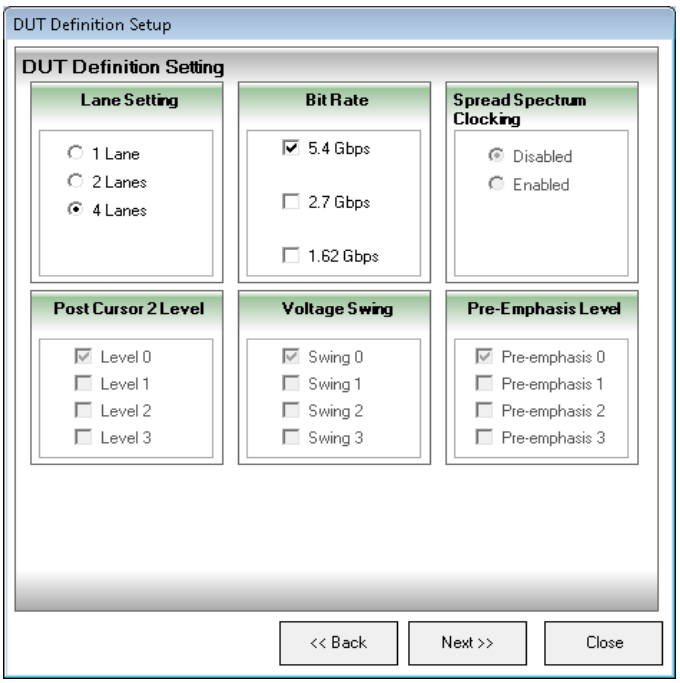
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

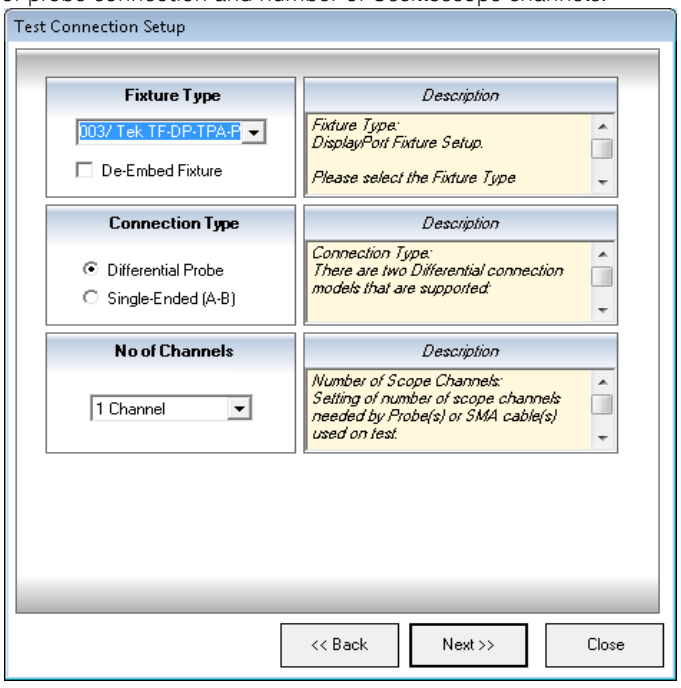
b Select **Device Type:** as **Sink**, **Test Type:** automatically grays out.

c Click **Next**.

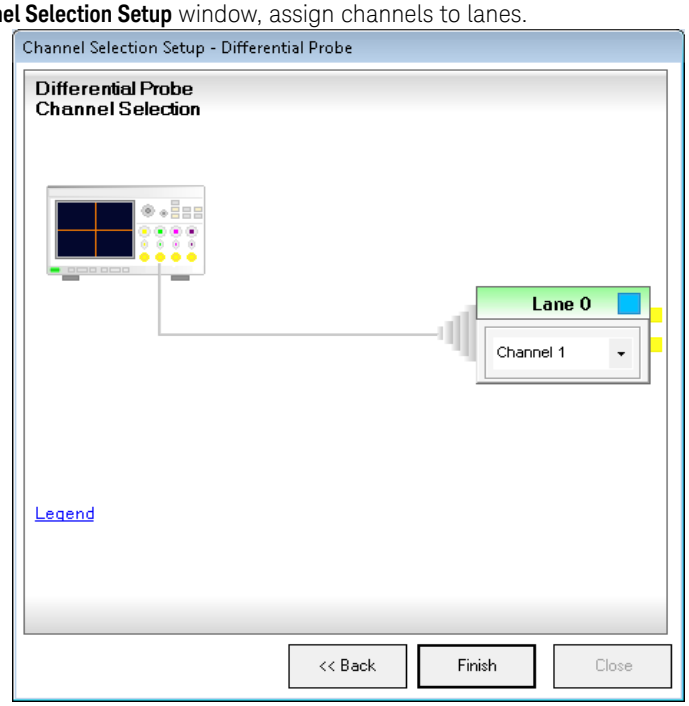
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

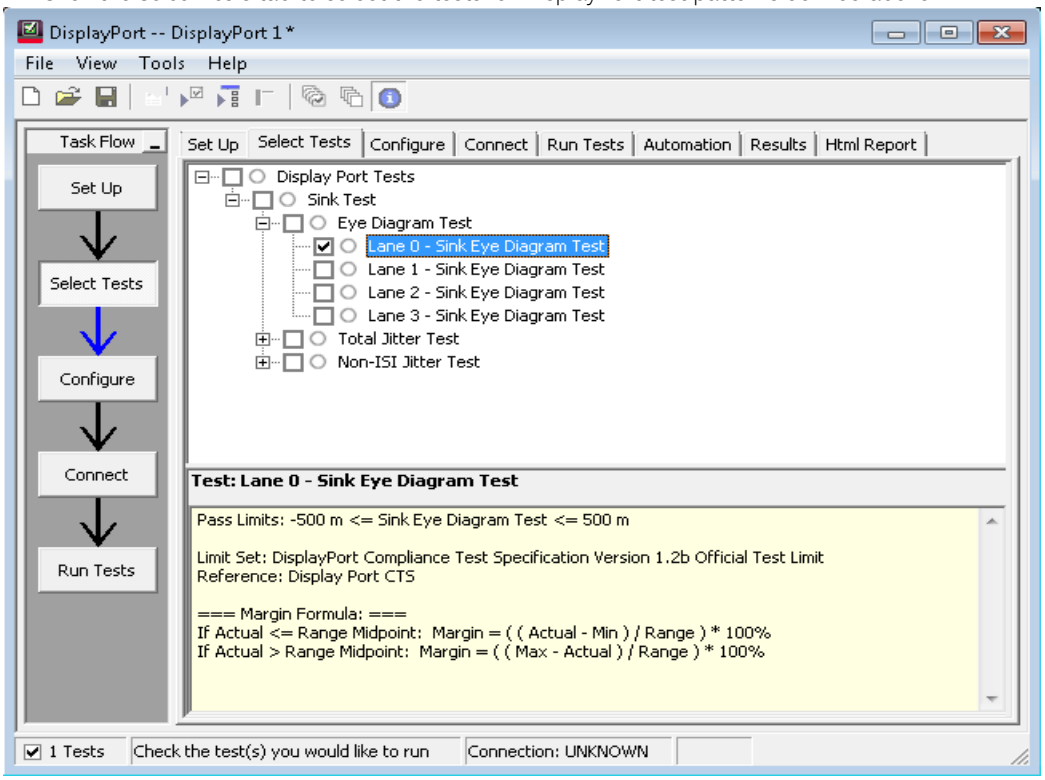


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Sink Tests" on page 186 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer).
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 28 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 28 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

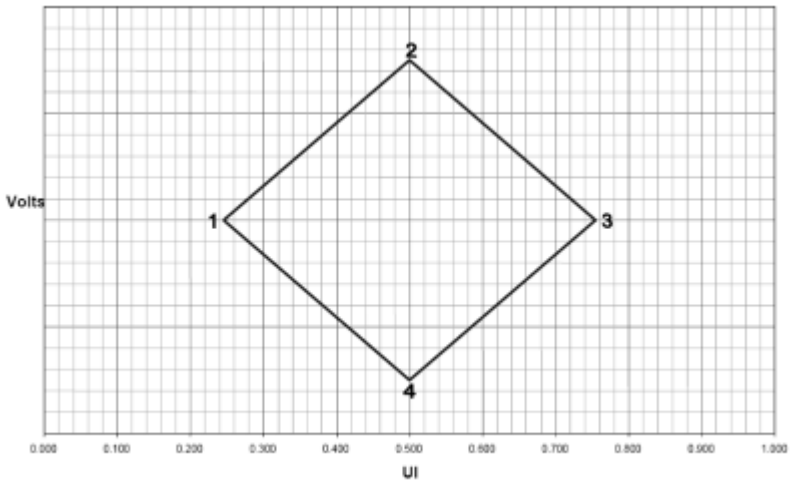


Figure 26 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 29 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045

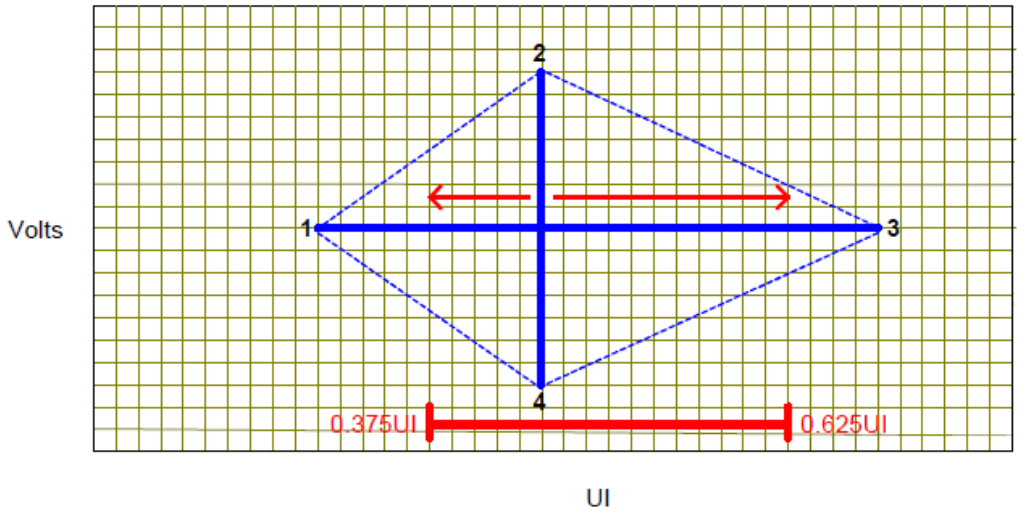


Figure 27 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001, 12210002, 12210003, 12210004 – Sink Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

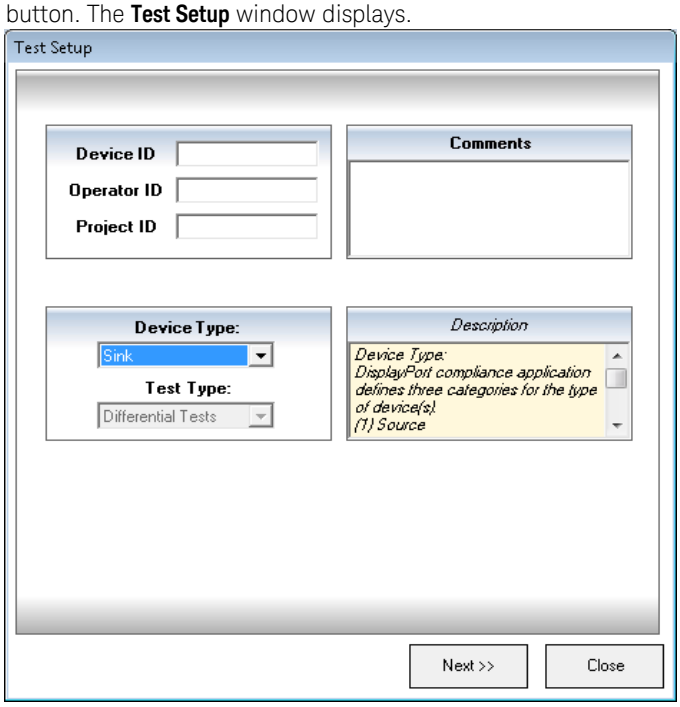
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



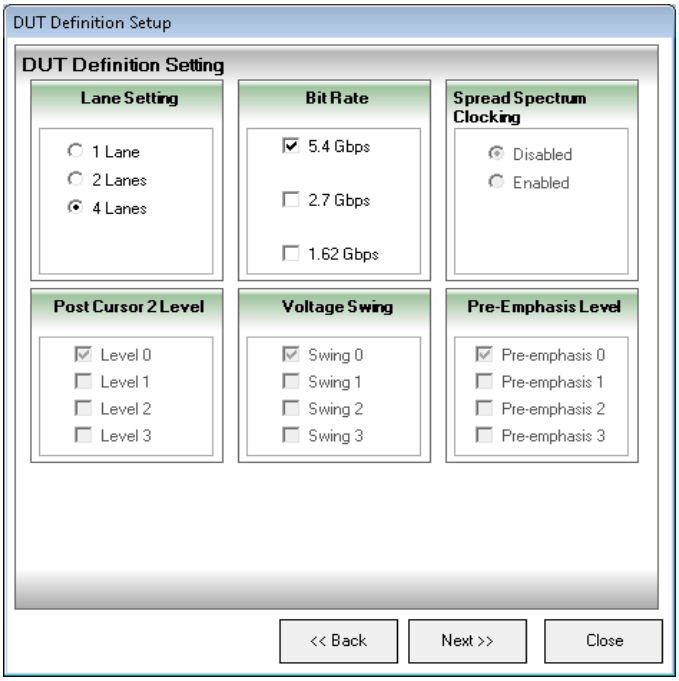
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

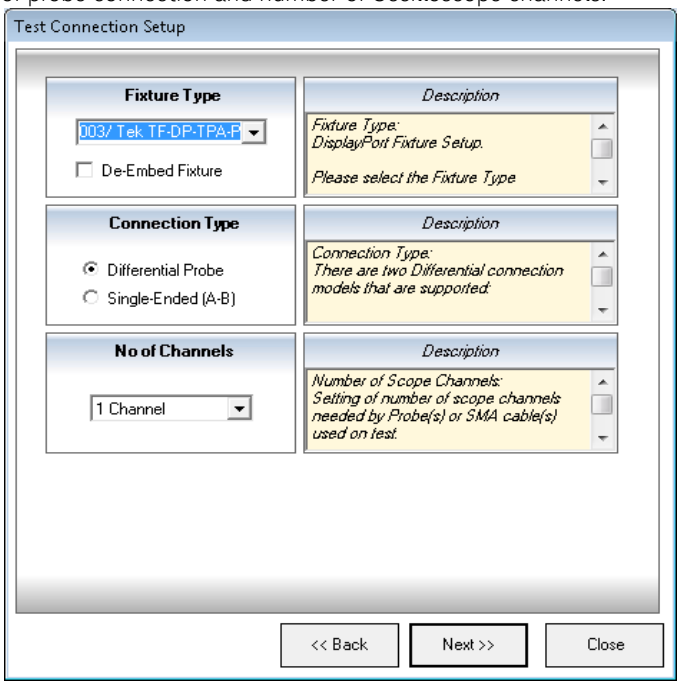
b Select **Device Type:** as **Sink**, **Test Type:** automatically grays out.

c Click **Next**.

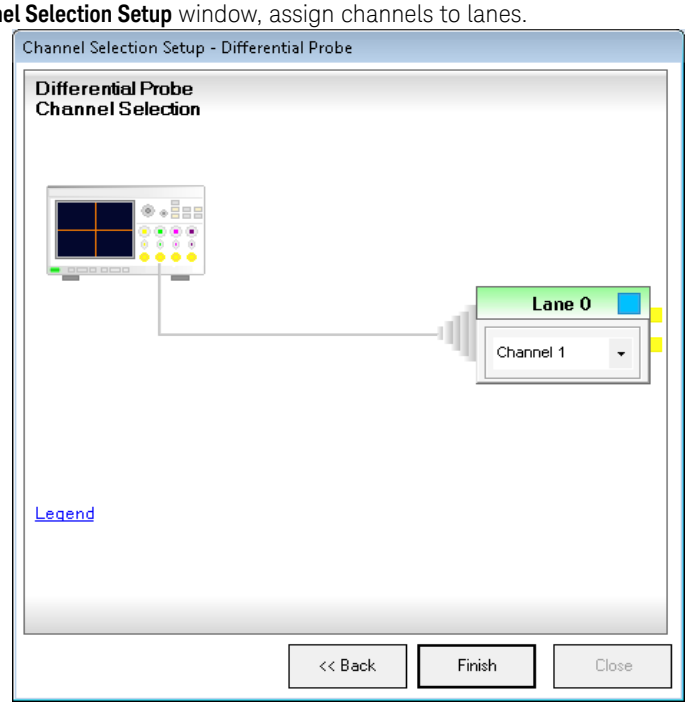
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

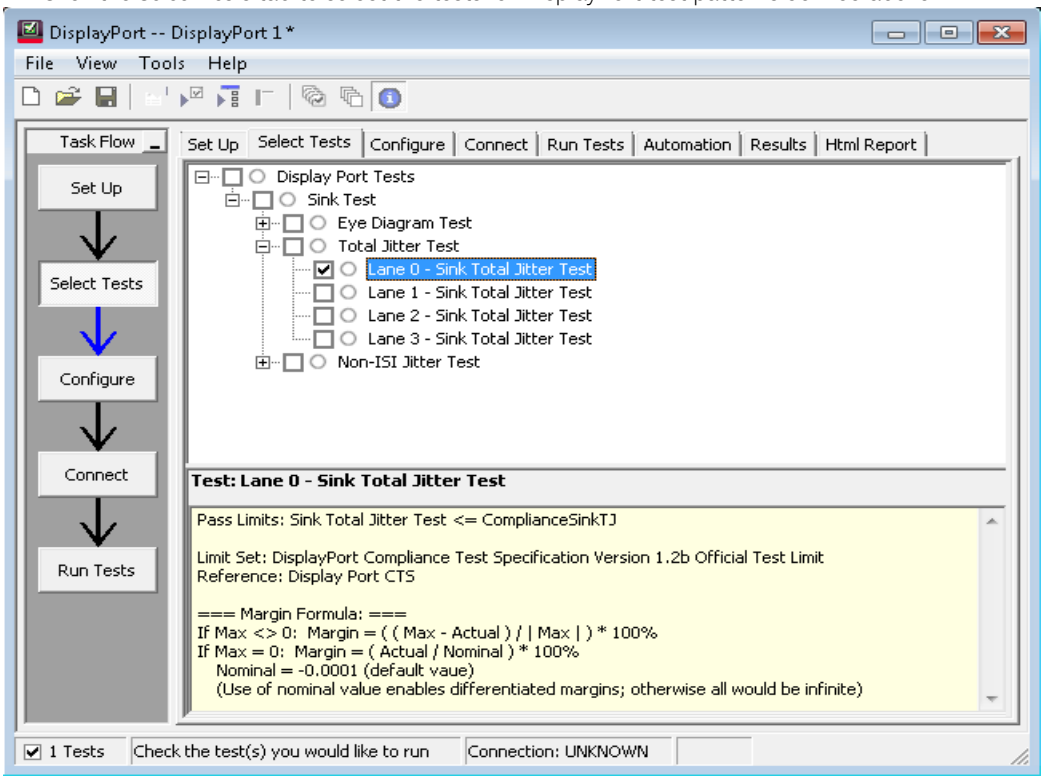


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Sink Tests" on page 186 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 30 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 31 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Test

Test ID

12220001, 12220002, 12220003, 12220004 – Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Calculate Non-ISI Jitter using the following equation:

$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

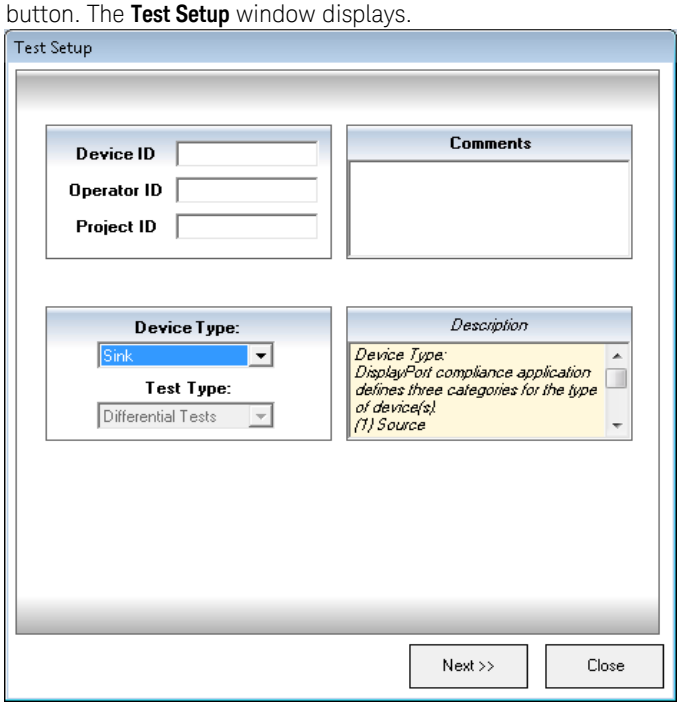
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



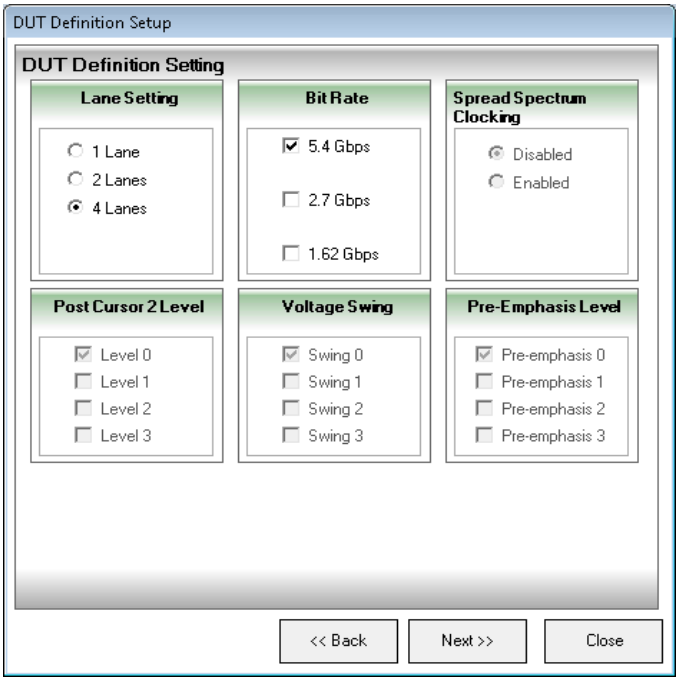
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

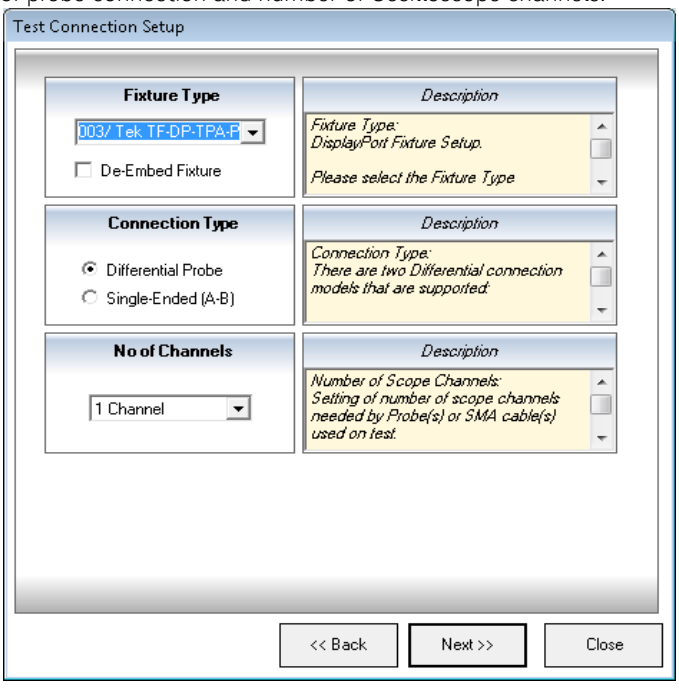
b Select **Device Type:** as **Sink**, **Test Type:** automatically grays out.

c Click **Next**.

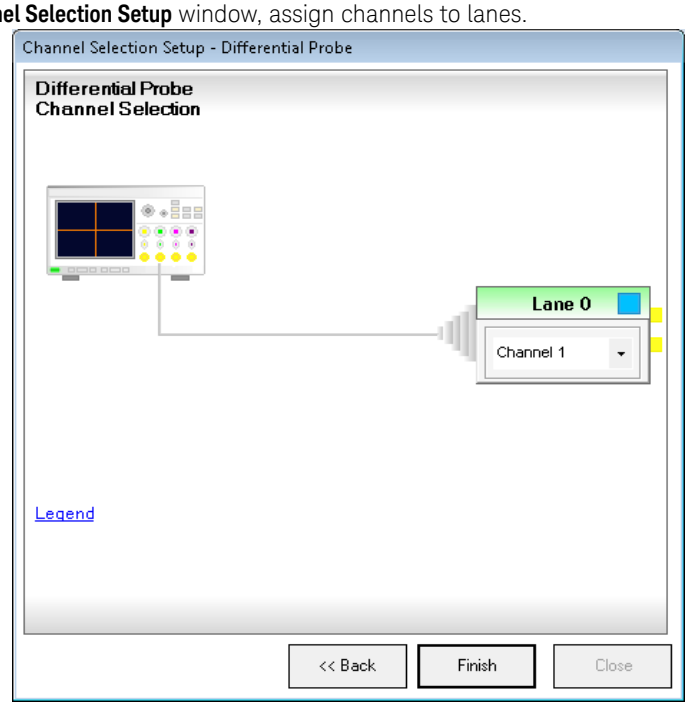
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

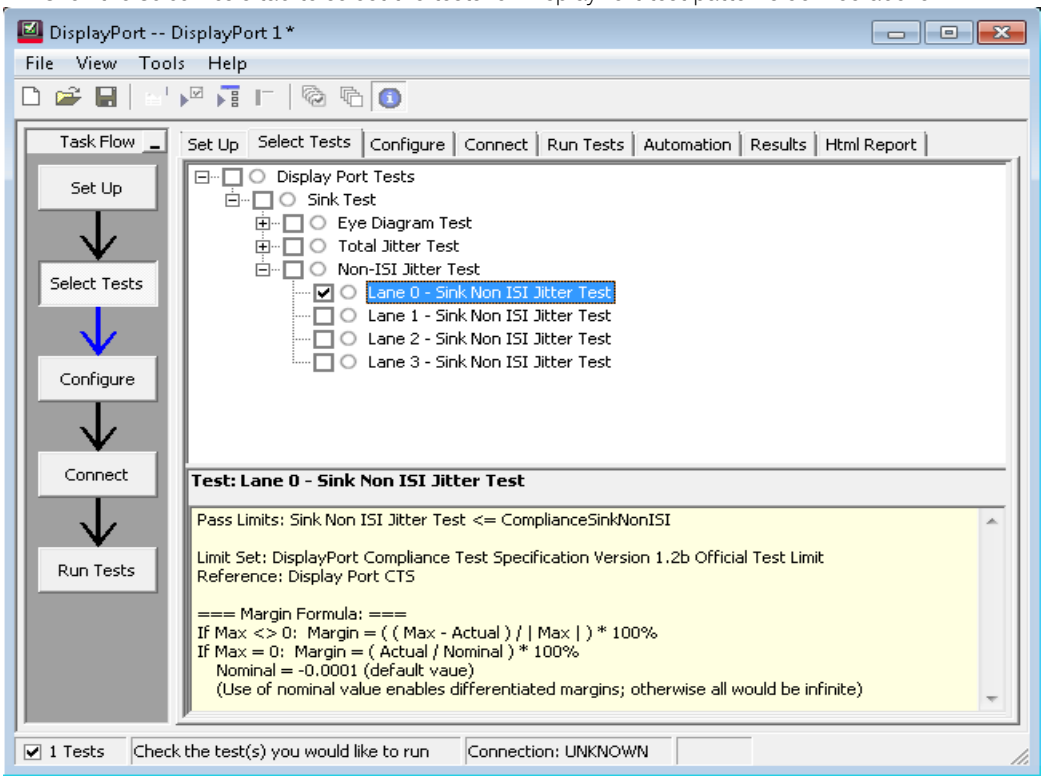


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Sink Tests" on page 186 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 32 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 33 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

5 DisplayPort 1.2 Cable Tests

Overview

Test Point Definition for DisplayPort 1.2 (1.2b) Cable Tests

NOTE Cable Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Cable DUT at Test Point 3 (TP3) as shown in Figure 28. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

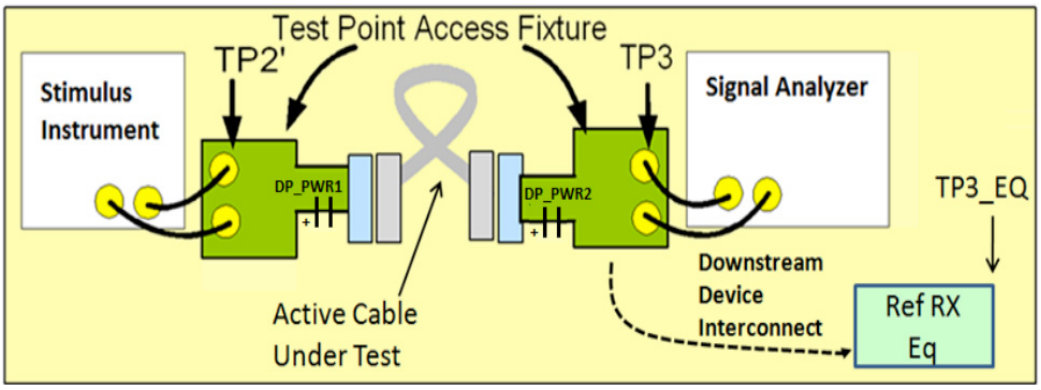


Figure 28 Test Point 3 Connection for DisplayPort 1.2 Cable Tests

Table 34 defines the test point fixtures and instruments used for DisplayPort 1.2 (1.2b) Cable Tests:

Table 34 Test Point Fixtures and Instruments for DisplayPort 1.2 Cable Tests

Test Requirement	Device Used
Stimulus Instrument	Pulse Pattern Generator ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Table 35 defines the input signal parameters applied by the stimulus instrument at TP2:

Table 35 Input Signal Parameters by Stimulus Instrument

RBR	▪ Reference Table 3-22 and Table 3-24, DP 1.2a ▪ Edge Rate (20-80): 155-165ps (260mUI) ▪ Eye Height: 400mV ▪ Total Jitter: 270mUI ▪ ISI: 100mUI ▪ Random Jitter (rms): 7.9mUI ▪ Sinusoidal Jitter: ~75mUI at 20MHz (Adjust to achieve Total Jitter)
HBR	▪ Reference Table 3-22 and Table 3-23, DP 1.2a ▪ Edge Rate (20-80): 90-100ps (260mUI) ▪ Eye Height: 350mV ▪ Total Jitter: 420mUI ▪ ISI: 144mUI ▪ Random Jitter (rms): 13.2mUI ▪ Sinusoidal Jitter: ~117mUI at 20MHz (Adjust to achieve Total Jitter)

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Cable Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 29).

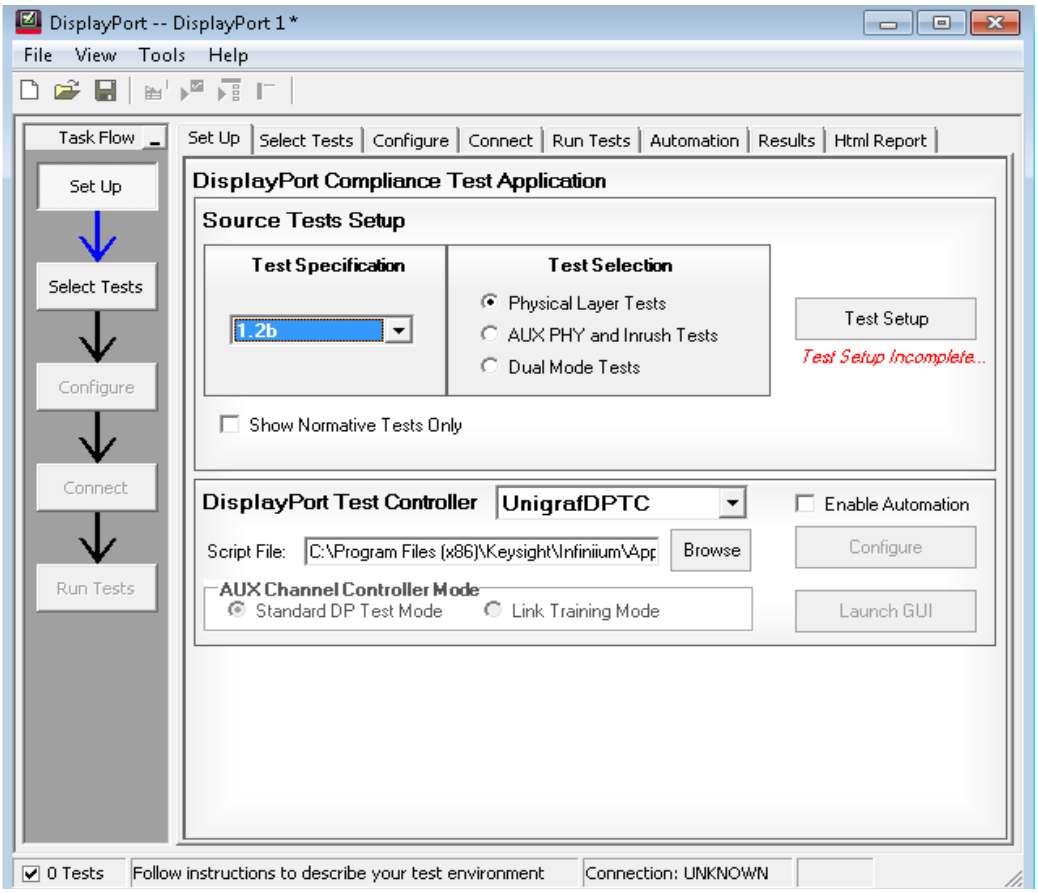


Figure 29 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.2b Standards, select **1.2b** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.2 Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

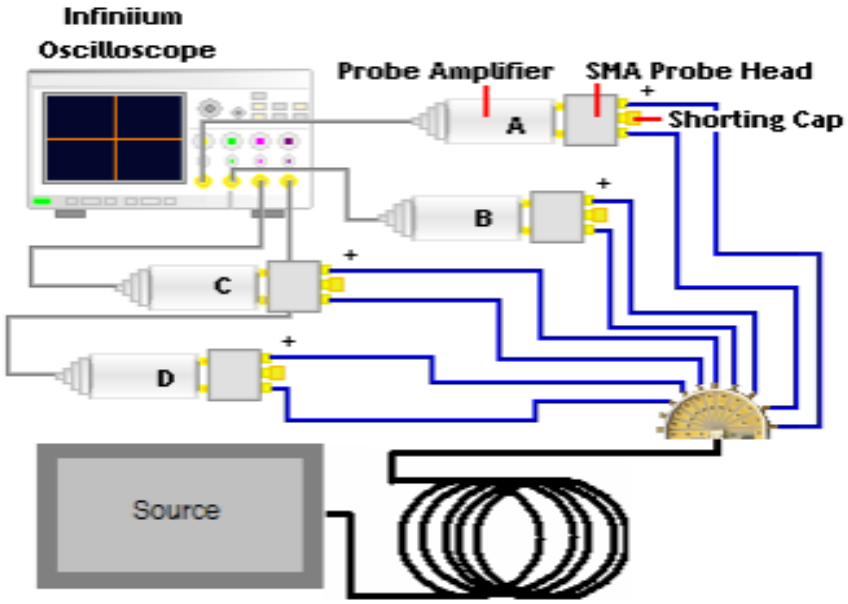


Figure 30 Sample connection diagram for DisplayPort 1.2 Cable Tests

Cable Eye Diagram Test

Test ID

12150001, 12150002, 12150003, 12150004 – Cable Eye Diagram Test

Test Overview

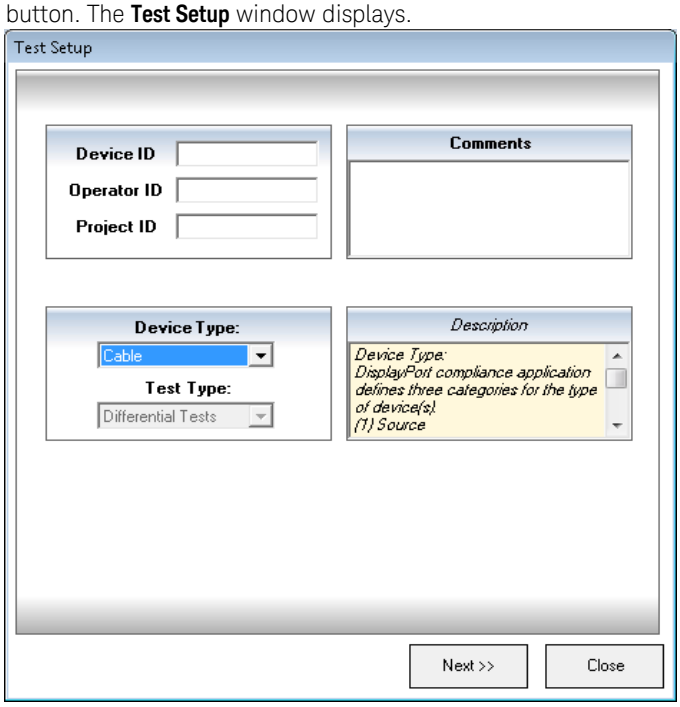
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 35
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



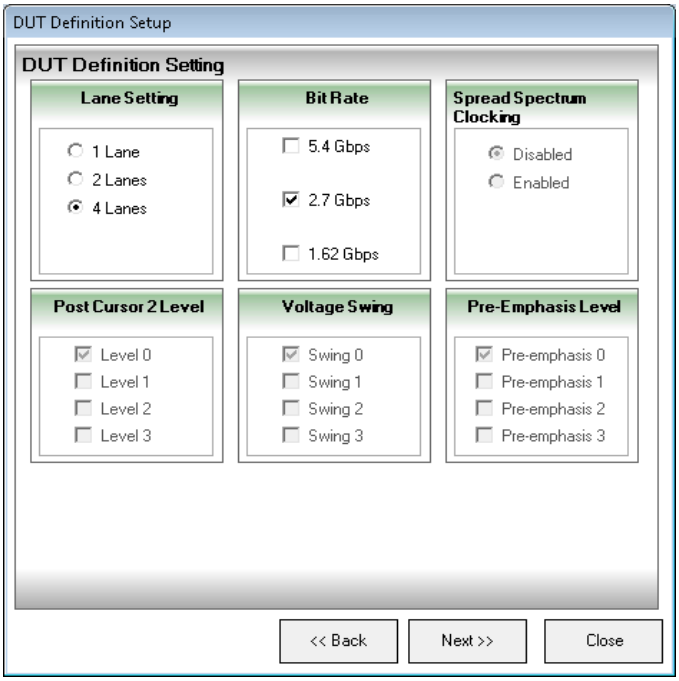
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

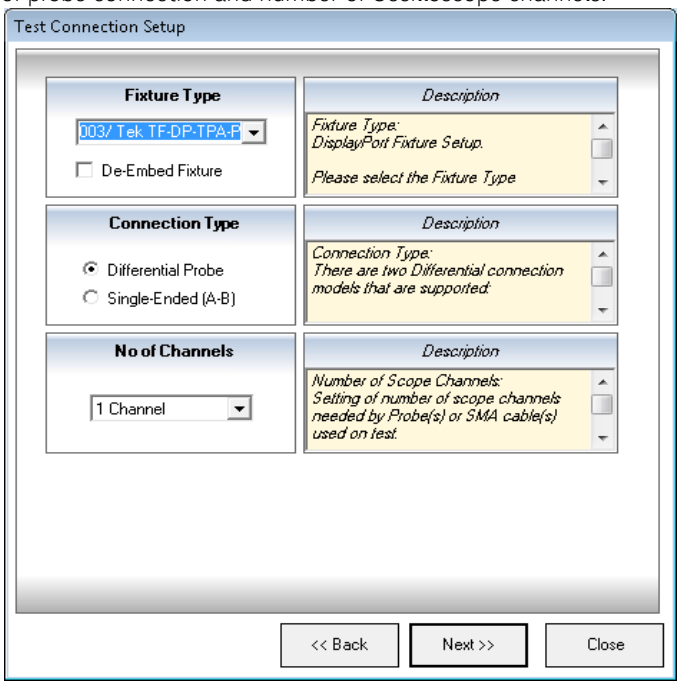
b Select **Device Type:** as **Cable**, **Test Type:** automatically grays out.

c Click **Next**.

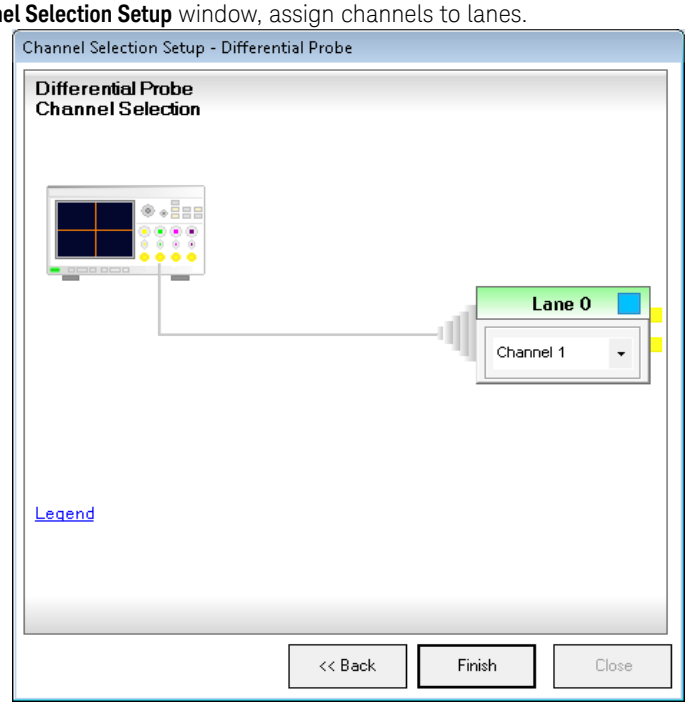
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

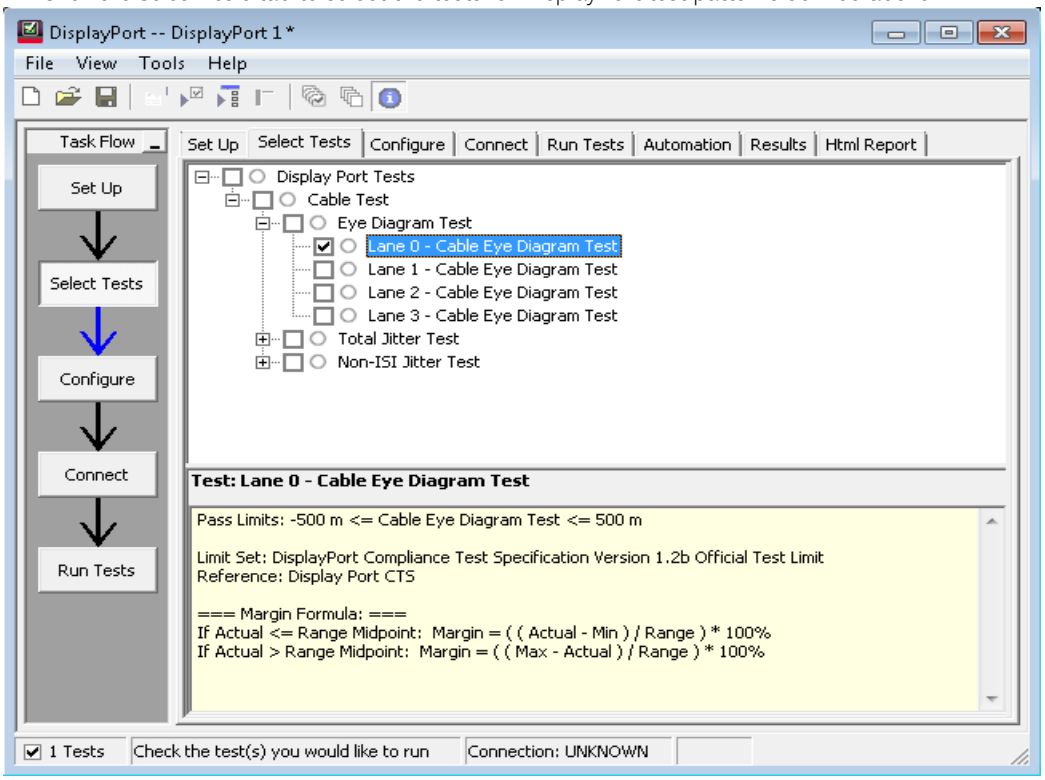


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Cable Tests" on page 212 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1. Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2. Acquire and verify the input signal.
   a. Verify the trigger and the amplitude of the input signal.
   b. Scale the vertical display of the input signal to the optimum value.
   c. Measure V_{TOP} and V_{BASE} of the input signal.
3. Create FUNC3 signal, which is the magnify signal of the input signal.
4. Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a. Scale the vertical display of the equalized signal to the optimum value.
   b. Measure V_{TOP} and V_{BASE} of the equalized signal.
   c. Measure the data rate of the equalized signal.
5. Set up the parameter of the measurement:
   a. Enable measurement of all edges to obtain a statistical value of the measurement.
   b. Set up the measurement threshold.
   c. Set up the Clock Recovery as described in the section “Clock Recovery”.
6. Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7. Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8. Set up the parameter for the Mask Test.
   a. Load the eye mask based on the settings in the Configuration Variable.
   b. Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c. Run the eye mask until 1,000,000 UI are folded.
9. Measure the jitter of the eye diagram using the Histogram.
10. Check for any signal trajectories that may have entered into the mask.
11. Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 36 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 36 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

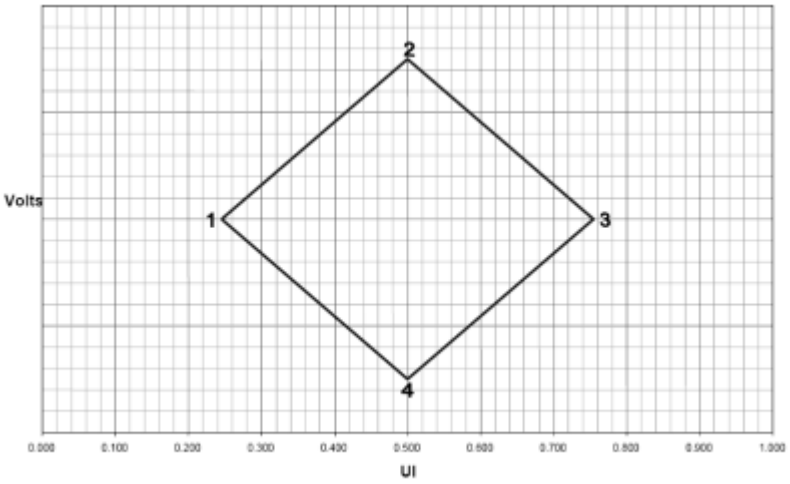


Figure 31 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001, 12230002, 12230003, 12230004 – Cable Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

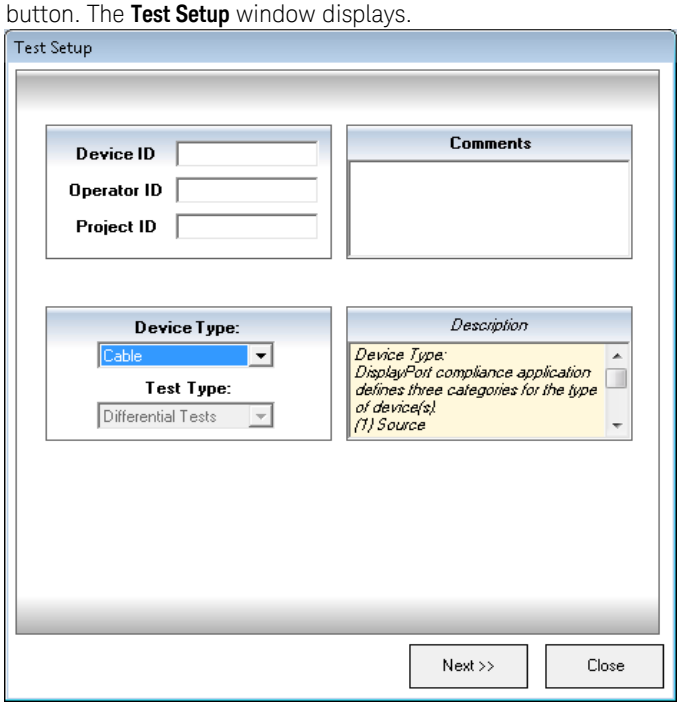
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 35

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



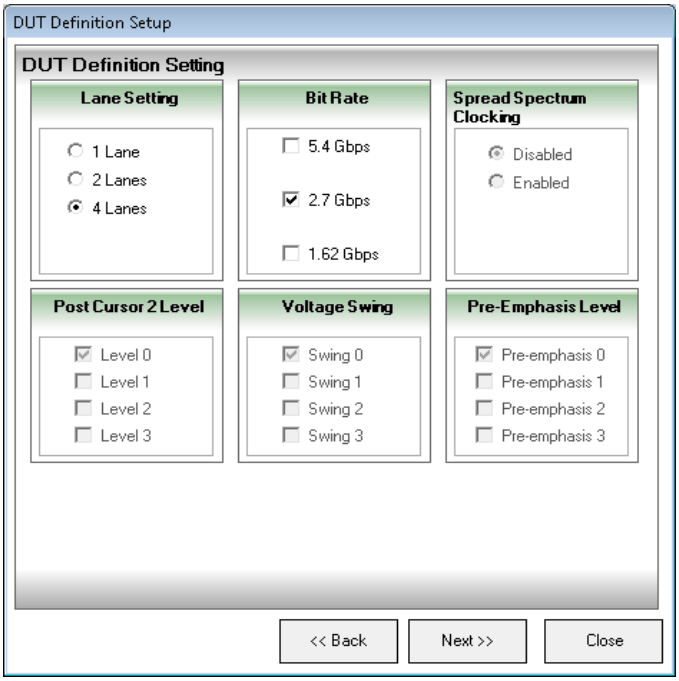
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

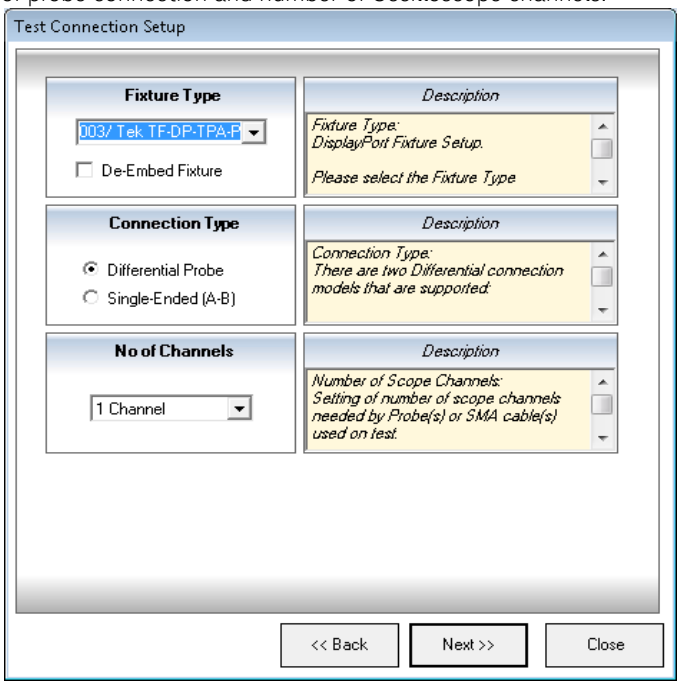
b Select **Device Type:** as **Cable**, **Test Type:** automatically grays out.

c Click **Next**.

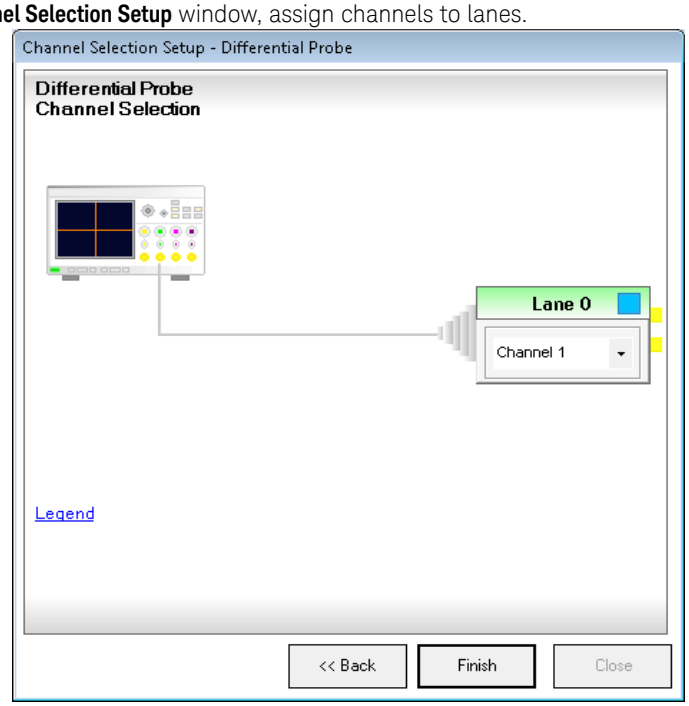
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

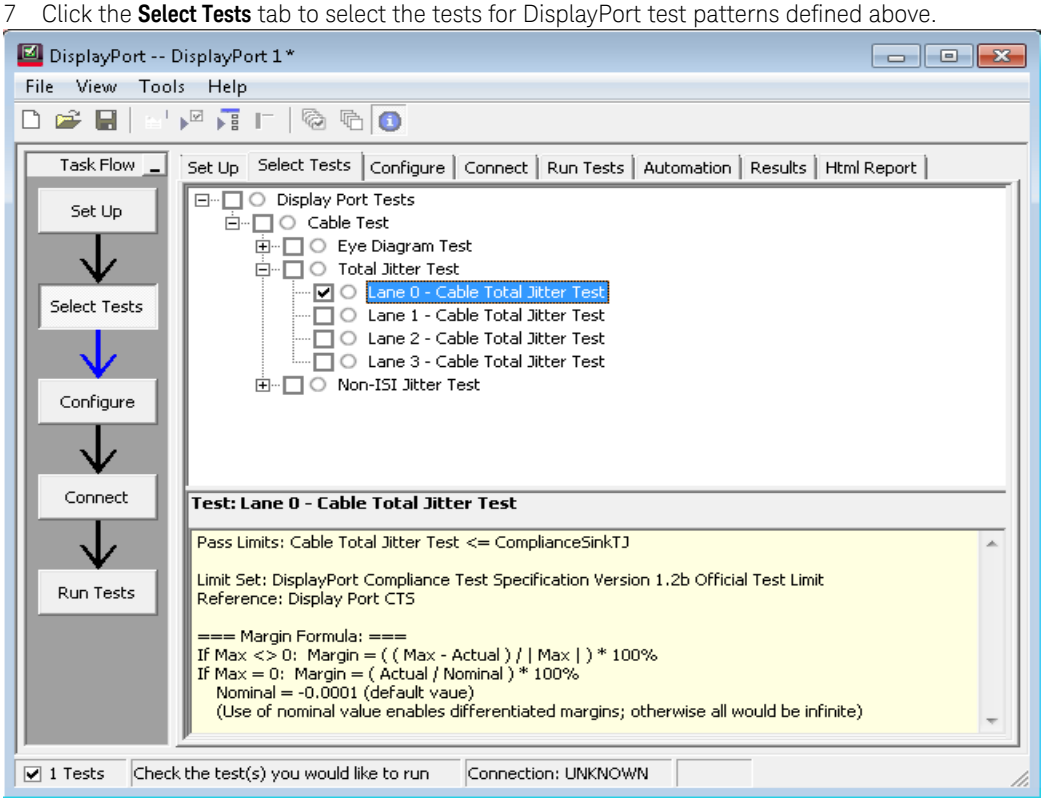


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Cable Tests" on page 212 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 37 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001, 12240002, 12240003, 12240004 – Cable Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Calculate Non-ISI Jitter using the following equation:

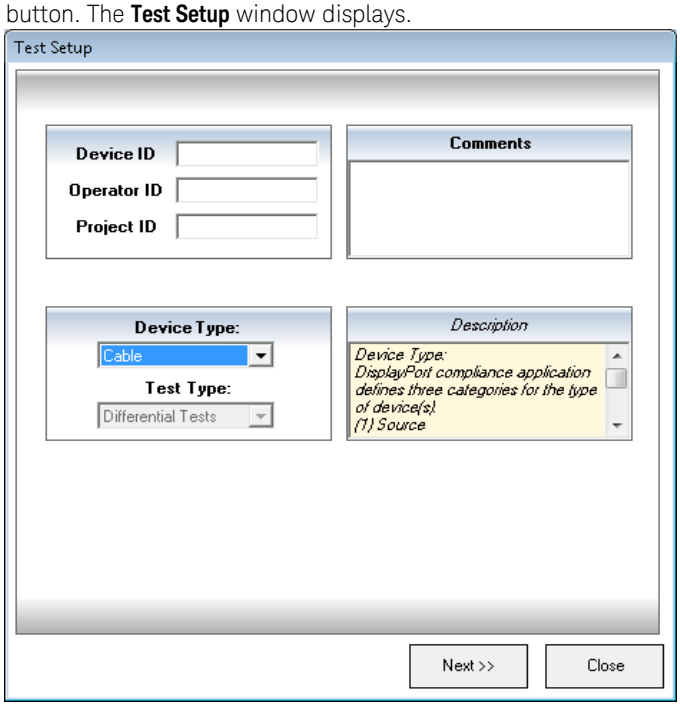
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 35

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



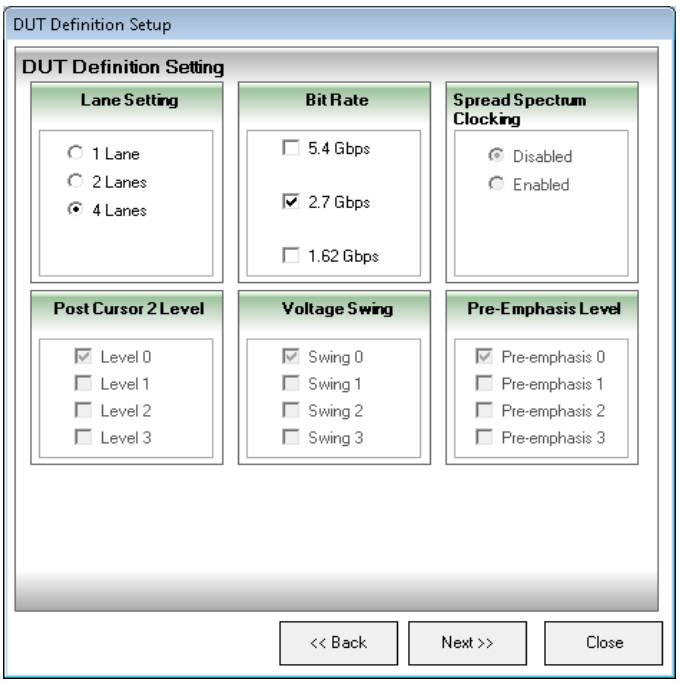
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

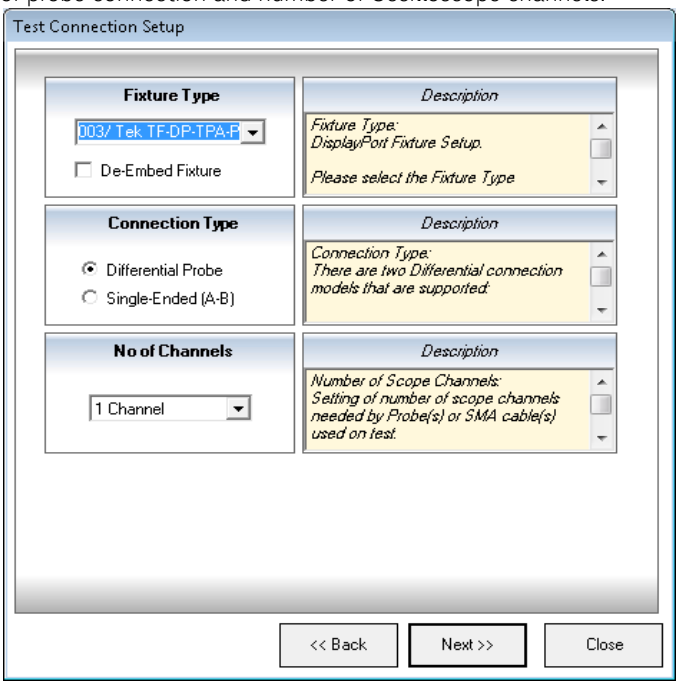
b Select **Device Type:** as **Cable**, **Test Type:** automatically grays out.

c Click **Next**.

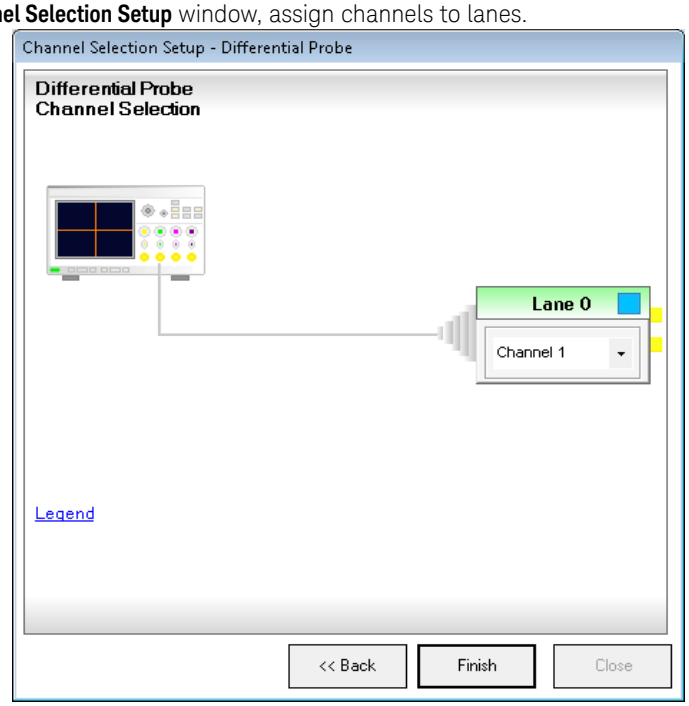
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of Oscilloscope channels.

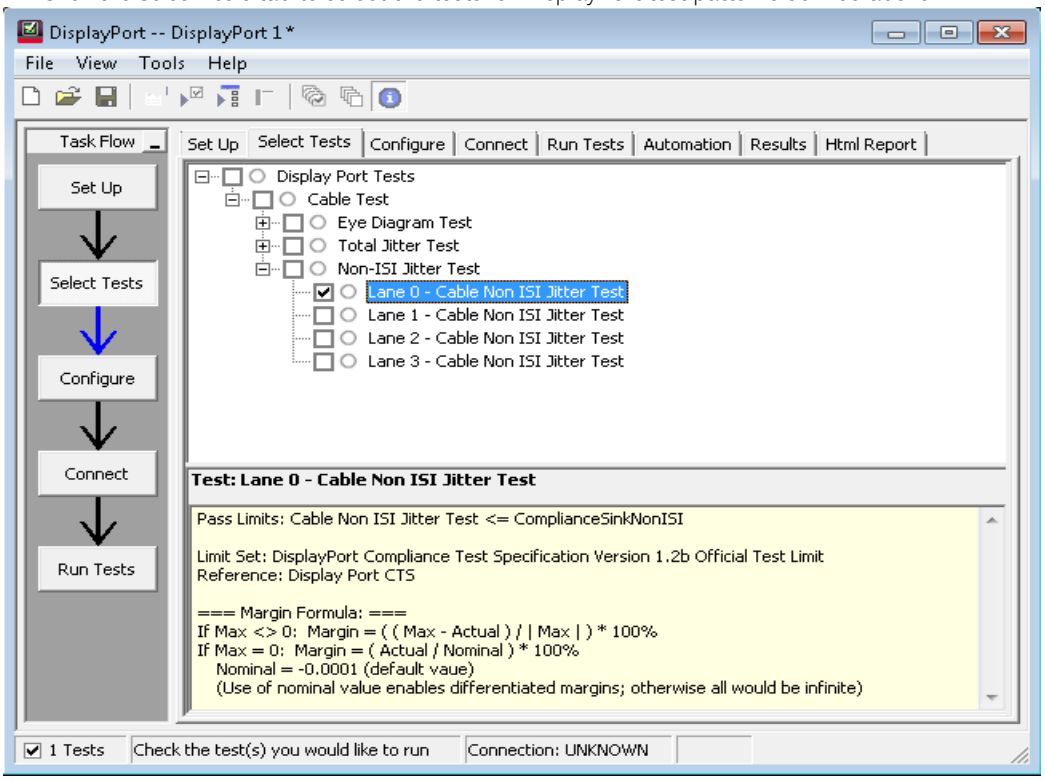


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Cable Tests" on page 212 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 38 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

6 DisplayPort 1.2 AUX Channel Tests

This section describes the normative and informative AUX Channel physical layer tests and inrush tests for compliance verification of DisplayPort1.2 source and sink.

Overview

Test Point for AUX Channel Tests

You must test the Source devices at Test Point 2 (TP2) while the Sink devices must be tested at Test Point 3 (TP3). See Figure 32.

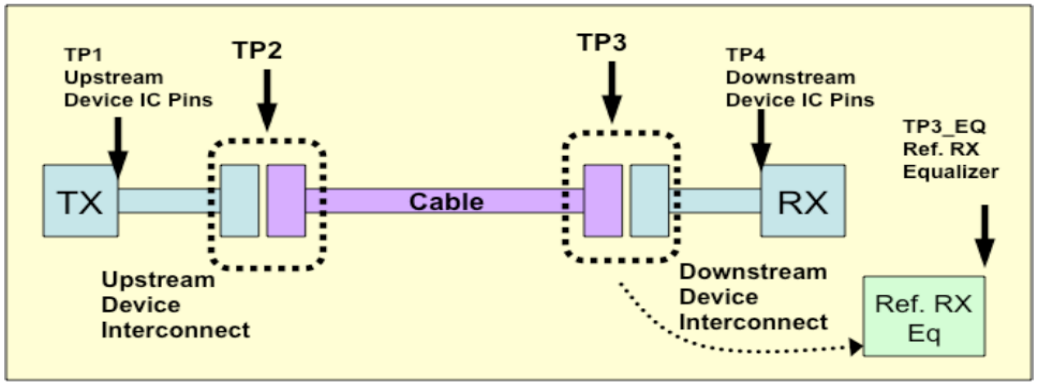


Figure 32 Test Point Connections for AUX Channel Tests

Table 39 defines the test point fixtures and instruments used for AUX Channel Tests:

Table 39 Test Point Fixtures and Instruments for AUX Channel Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope
Stimulus	Stimulus must be applied to the DUT to cause AUX Channel transactions to occur. This stimulus shall not be included in or affect the measurements. Reference Sink needed as stimulus for the Source DUT: ▪ Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Reference Source needed as stimulus for the Sink DUT: ▪ Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 AUX Channel Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 33).

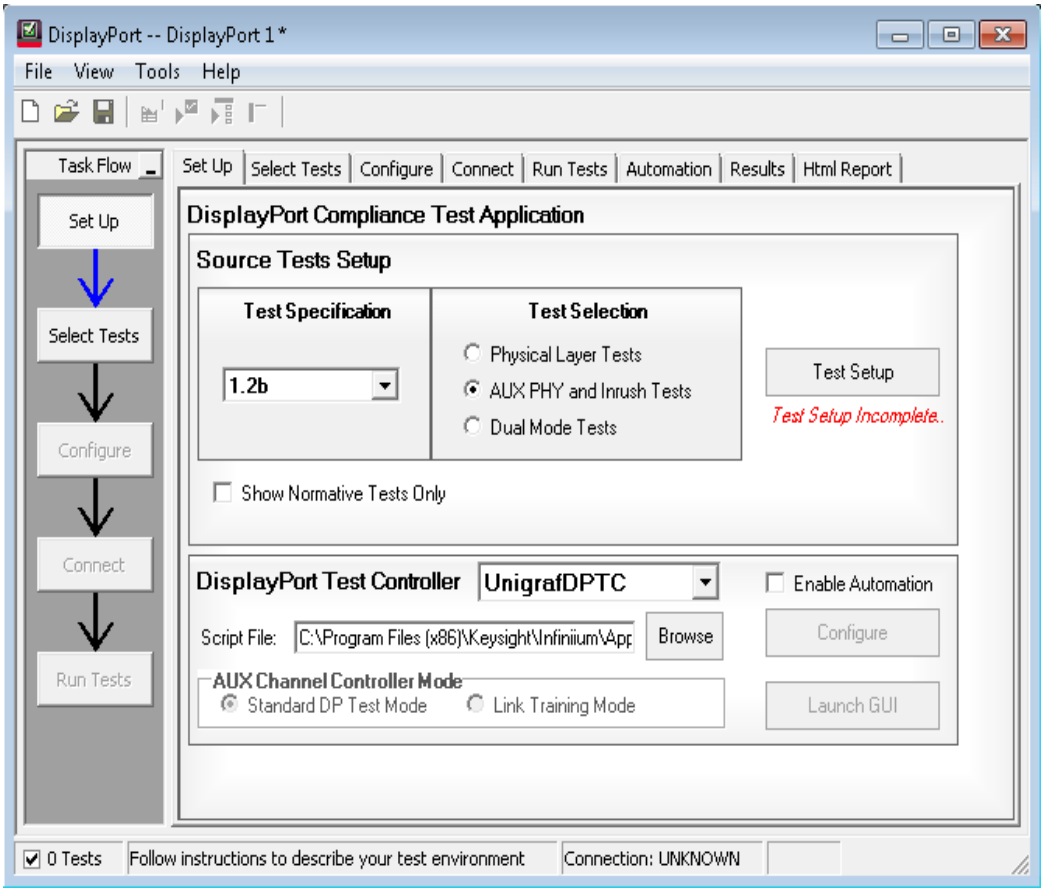


Figure 33 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.2b Standards, select **1.2b** from the drop-down options in the **Test Specification** area and select **AUX PHY and Inrush Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

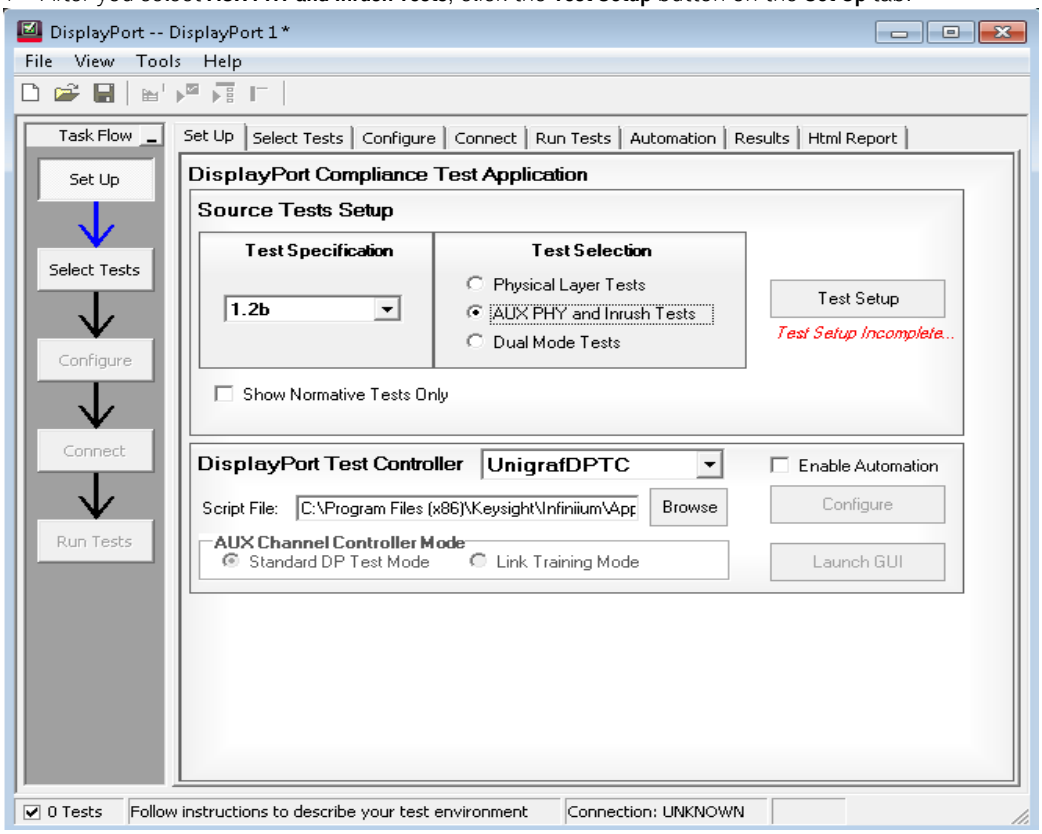
10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

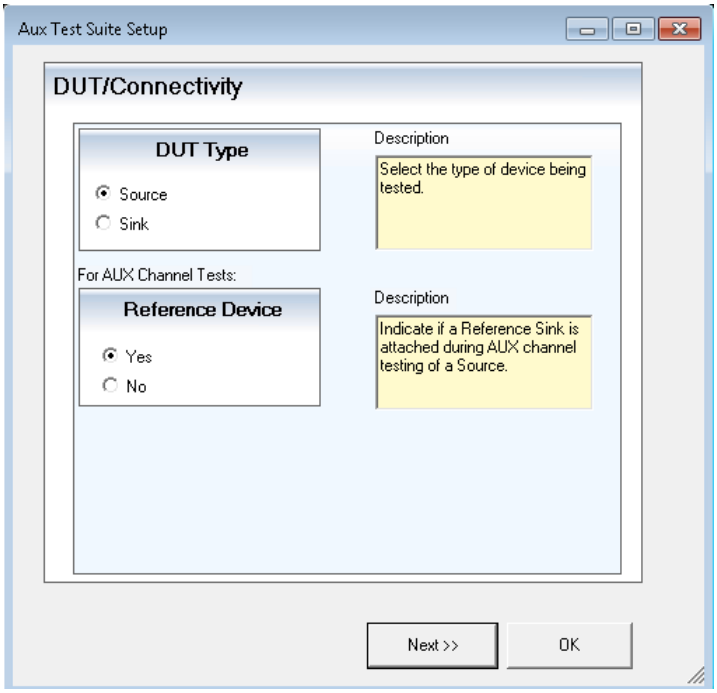
Setting Up for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

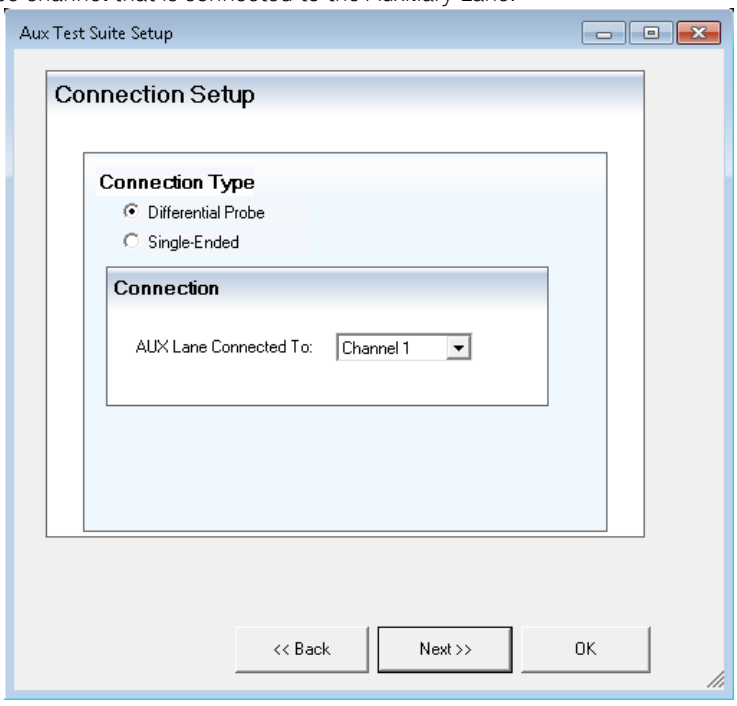
1 After you select **AUX PHY and Inrush Tests**, click the **Test Setup** button on the **Set Up** tab.



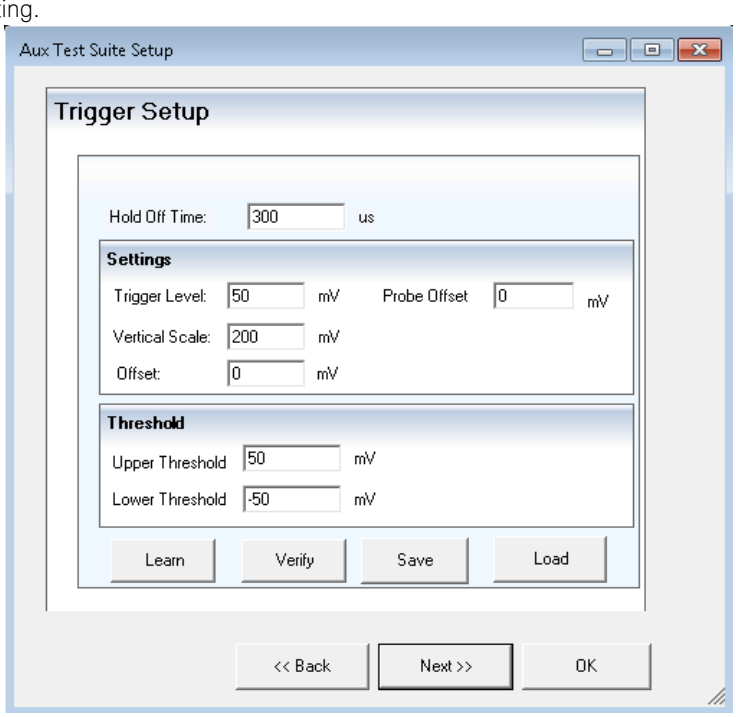
2 On the **DUT/Connectivity** page, select **Source** or **Sink** in the **DUT Type** area. In the **Reference Device** area, select **Yes** if a reference sink/source is attached to device under test during testing. Click **Next**.



3 On the **Connection Setup** page, depending on the probe connection you are using, select either **Differential Probe** or **Single-Ended** in the **Connection Type** area and in the **Connection** area, select the Oscilloscope channel that is connected to the Auxiliary Lane.



4 On the **Trigger Setup** page, define the Oscilloscope parameters to trigger on an Auxiliary signal during testing.



Hold Off Time – The Oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each AUX transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.

Trigger Level – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure 34 and Figure 35 shows correct and incorrect trigger levels.

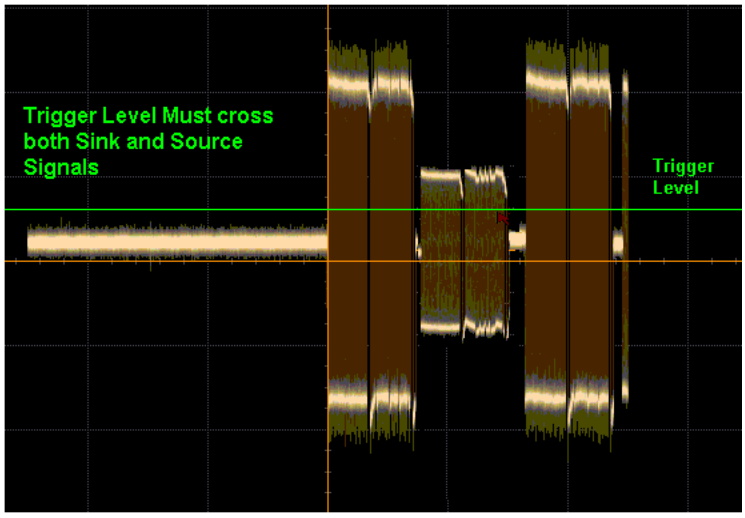


Figure 34 Correct Trigger Level

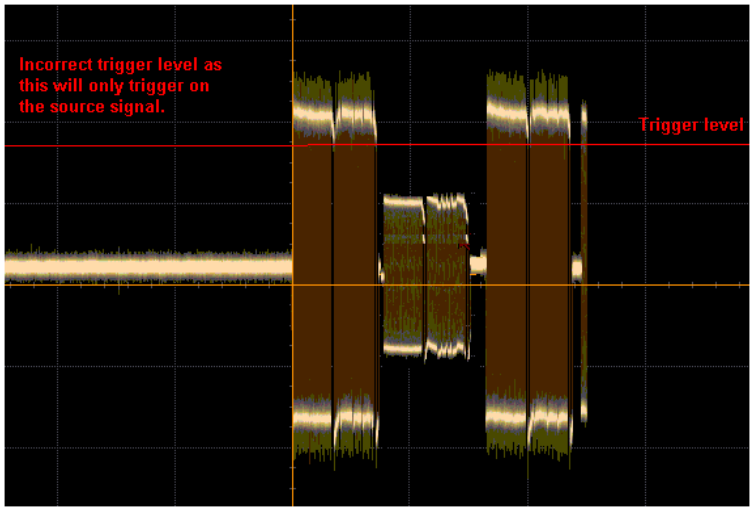


Figure 35 Incorrect Trigger Level

Vertical Scale – The Oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.

Offset – Set the offset so that the center point is aligned with the center of the oscilloscope display.

Upper Threshold/Lower Threshold – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply. Figure 36 and Figure 37 shows correct and incorrect threshold levels.

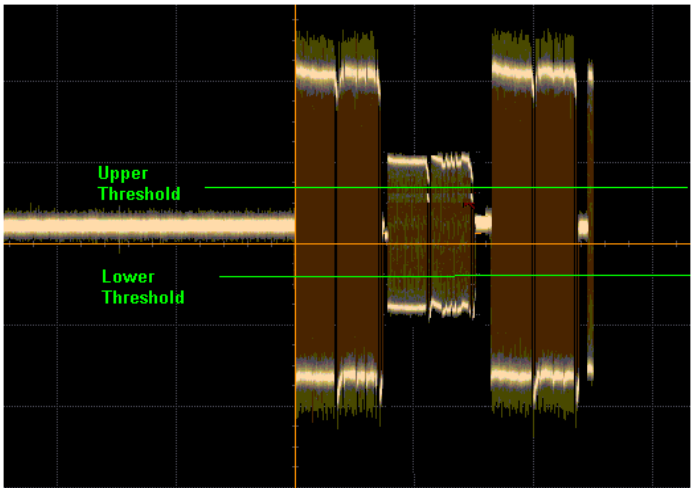


Figure 36 Correct Threshold set

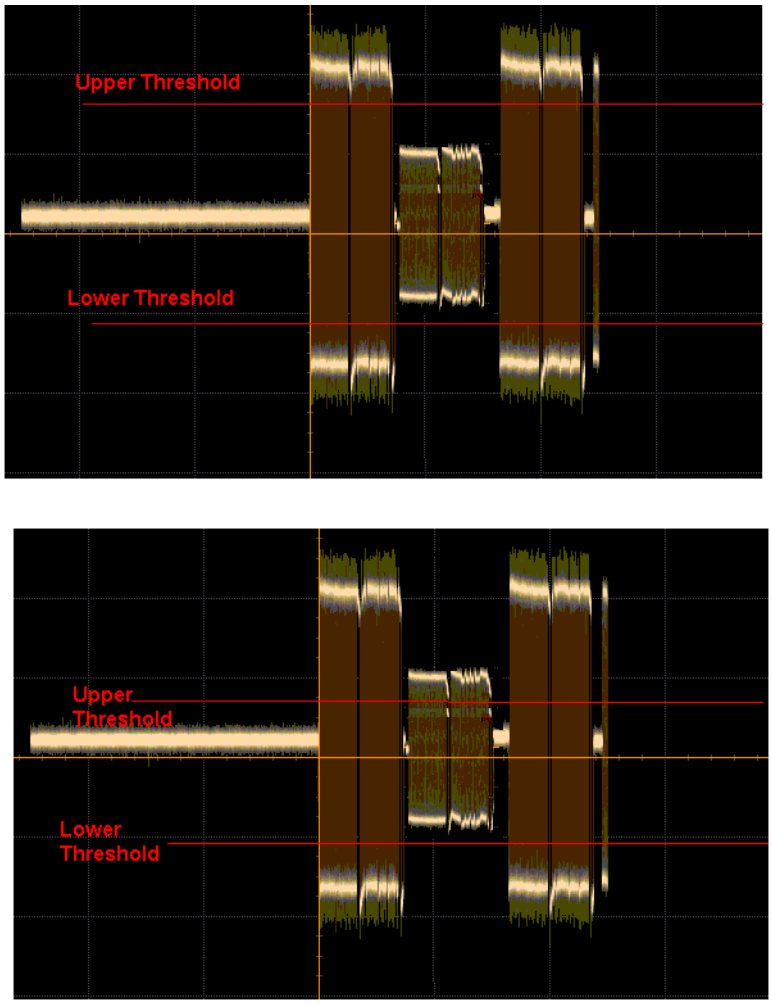


Figure 37 Wrong Thresholds set

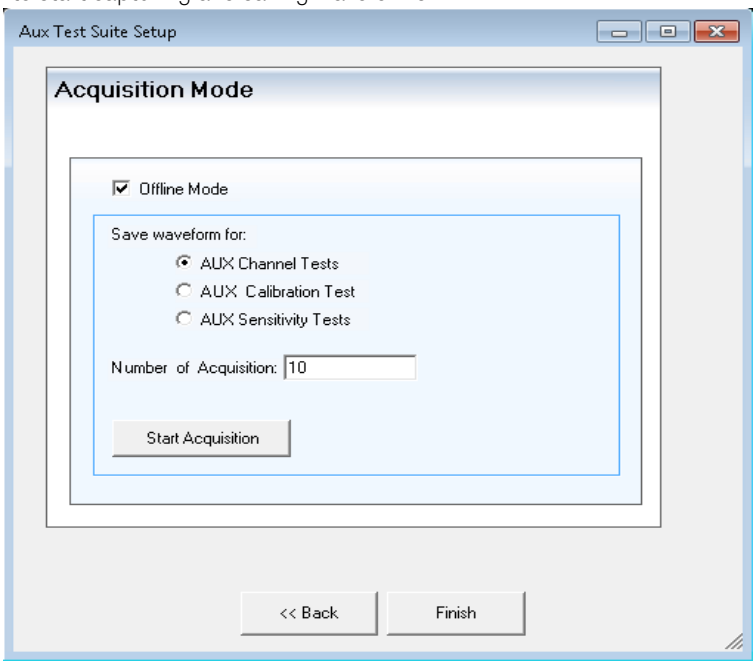
c On the **Trigger Setup** page, you may click the **Learn** button, which guides you through getting the trigger setup parameters. However, please note that the learning guide may not necessarily work many a times because the actual Auxiliary signals may vary for different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.

d Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.

e You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

5 On the **Acquisition Mode** page, either **Finish** the setup wizard or enable **Offline Mode**, which is de-selected, by default. Offline Mode lets you save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.

6 If you enable **Offline Mode**, define the number of waveforms to be saved. If required, click **Start Acquisition** to start capturing and saving waveforms.



7 Click **Finish** to close the setup wizard. The **Set Up** tab displays.

8 Click the **Select Tests** tab and select the AUX Channel tests you want to run.

Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

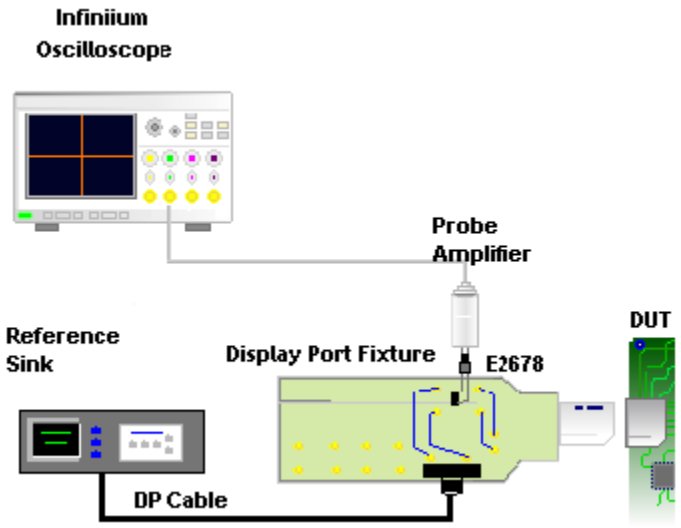


Figure 38 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

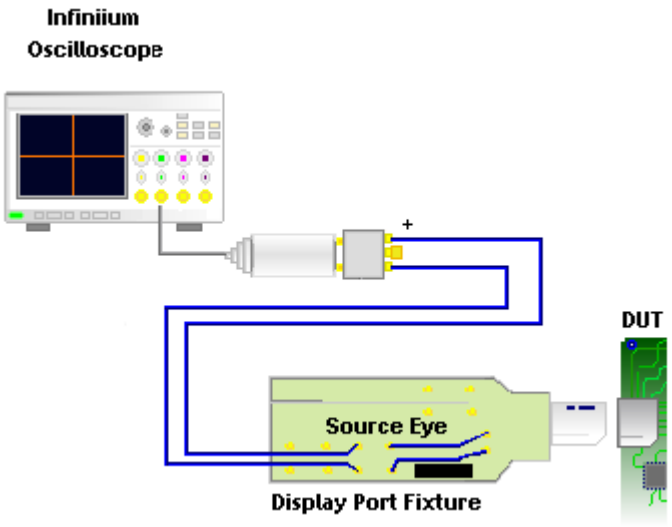


Figure 39 Sample connection diagram for source AUX channel tests without connecting to a reference sink

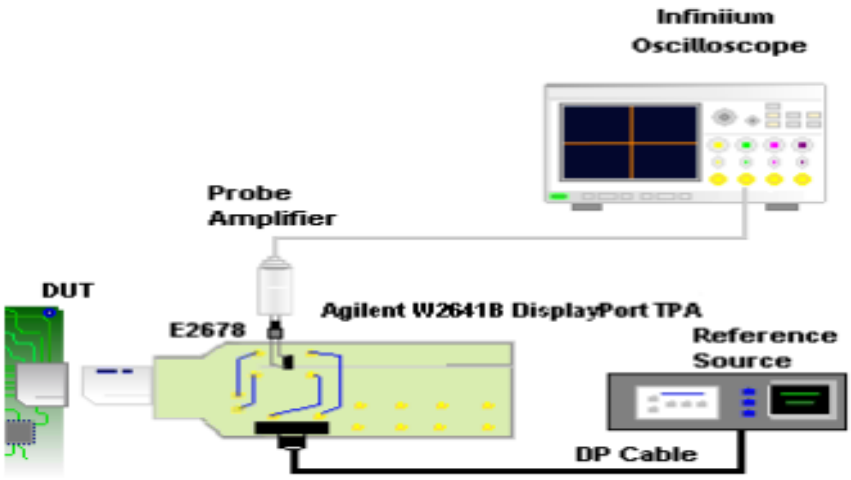


Figure 40 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until 10 waveforms are folded.

9 Check for any signal trajectories entering into the mask.

10 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 40 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

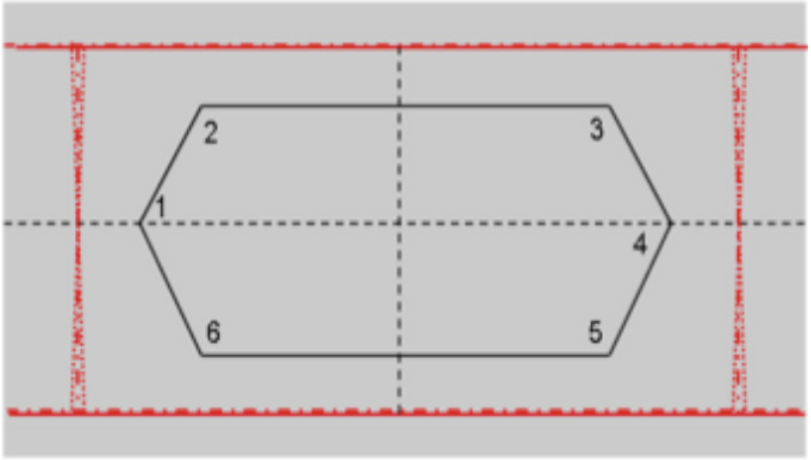


Figure 41 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2.6, Figure 3-29 and Table 3-8*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1. Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
2. Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
3. Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).
4. Set up the parameter of the measurement:
   - *a* Enable measurement of all edges to obtain a statistical value of the measurement.
   - *b* Set up the measurement threshold.
   - *c* Set up the Clock Recovery.
5. Generate FUNC3 signal, which is the second differential signal of the AUX Channel.
6. Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7. Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.
8. If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:
   - *a* Set up the parameter of the Mask Test:
     - i Load the eye mask based on the settings in the Configuration Variable.
     - ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
     - iii Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.
   - *b* Check for any signal trajectories entering into the mask.

9 Set up the waveform histogram on the AUX Channel eye diagram.

a Set up the vertical waveform histogram on the AUX Channel eye diagram to measure the peak to peak voltage.

10 Report the measurement results.

PASS Condition

Table 41 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 42 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

7 DisplayPort 1.2 Inrush Tests

Overview

This section describes the normative and informative inrush tests for compliance verification of DisplayPort1.2 source and sink, which is a power consumer.

Test Point for Inrush Tests

The test fixture for inrush tests implements the schematic shown in Figure 42.

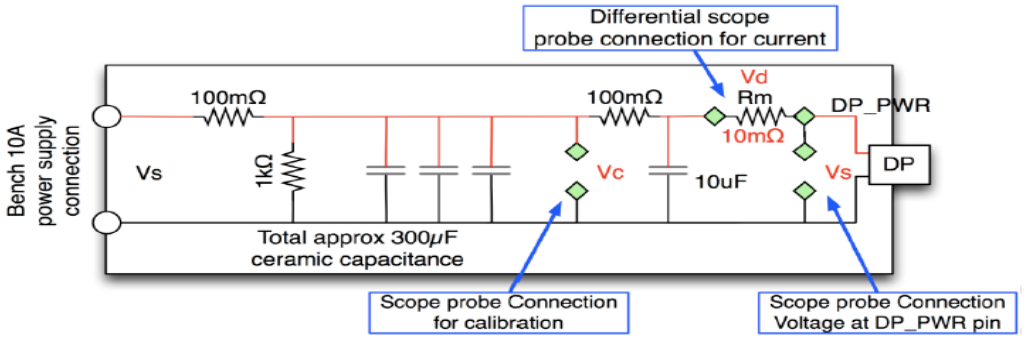


Figure 42 Schematics for testing Power Consumer Device

The test fixture must be designed and used according to the following guidelines:

- A high gate voltage FET on the DP_PWR line is recommended to allow a fast connect capability, which allows a single connection event for testing. Without such an arrangement, multiple connections will be required to obtain a reasonable “worst-case” attachment event.
- Connection length between the power supply and the test fixture must be minimized. A maximum of four inches is recommended.
- The power supply must have enough outrush capability as to not negatively affect the test fixture’s outrush capability.
- The power supply must be run at 3.6V (3.3V + 10%) read across V_C.

Any Power Consumer test fixture must be calibrated using the Power User test fixture, as shown in Figure 42. Testing with the two fixtures combined should result in the approximate values given below. If required, the component values on the Power Consumer test fixture should be adjusted to match the expected results.

- V_C steady before connection = 3.6V
- V_C droop = ~3.1V
- Inrush Current = ~13.0A

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Inrush Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 43).

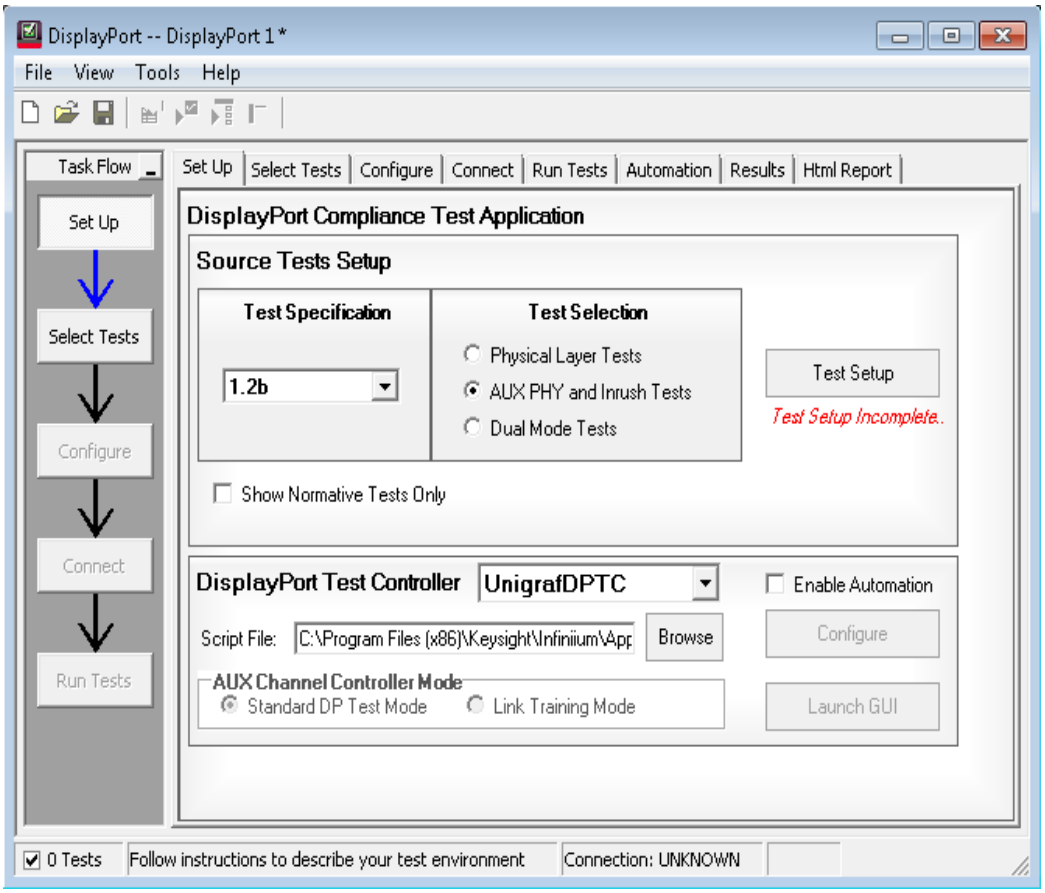


Figure 43 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.2b Standards, select **1.2b** from the drop-down options in the **Test Specification** area and select **AUX PHY and Inrush Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests. Refer to "Setting Up for AUX PHY and Inrush Tests" on page 235 to know in detail how to set up the DUT for Inrush Tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

8 DisplayPort 1.2 Dual Mode Tests

Overview

This section describes the normative and informative dual mode physical layer (differential and single-ended) tests for compliance verification of DisplayPort1.2 DUTs.

Test Point

The source device for dual mode tests must be tested at Test Point 2 (TP2), as shown in Figure 44.

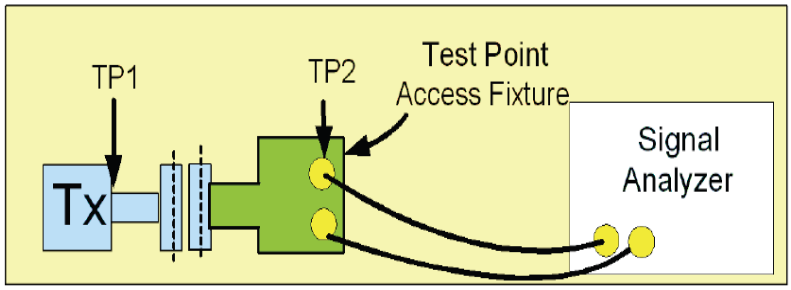


Figure 44 Test Point 2 Connection for Dual Mode Source Tests

Table 43 defines the test point fixtures and instruments used for DisplayPort 1.2 Dual Mode Tests:

Table 43 Test Point Fixtures and Instruments for DisplayPort 1.2 Dual Mode Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.2 Dual Mode Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 45).

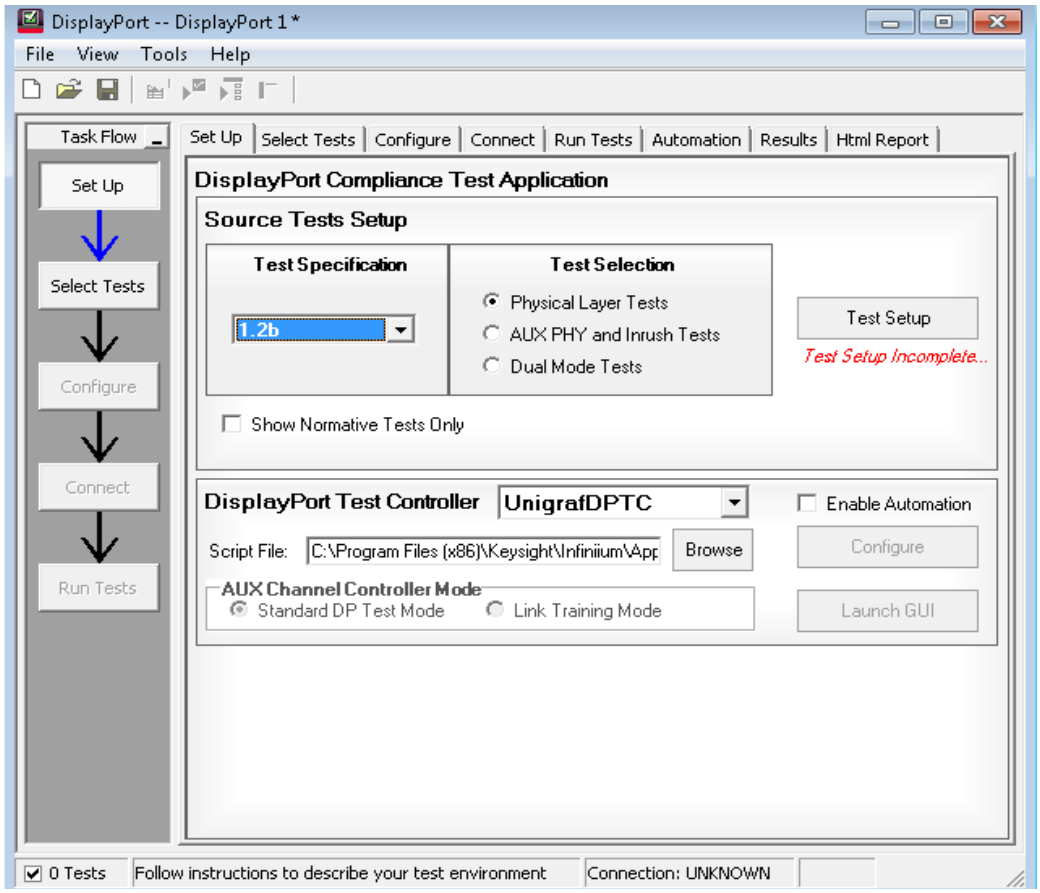


Figure 45 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.2b Standards, select **1.2b** from the drop-down options in the **Test Specification** area and select **Dual Mode Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

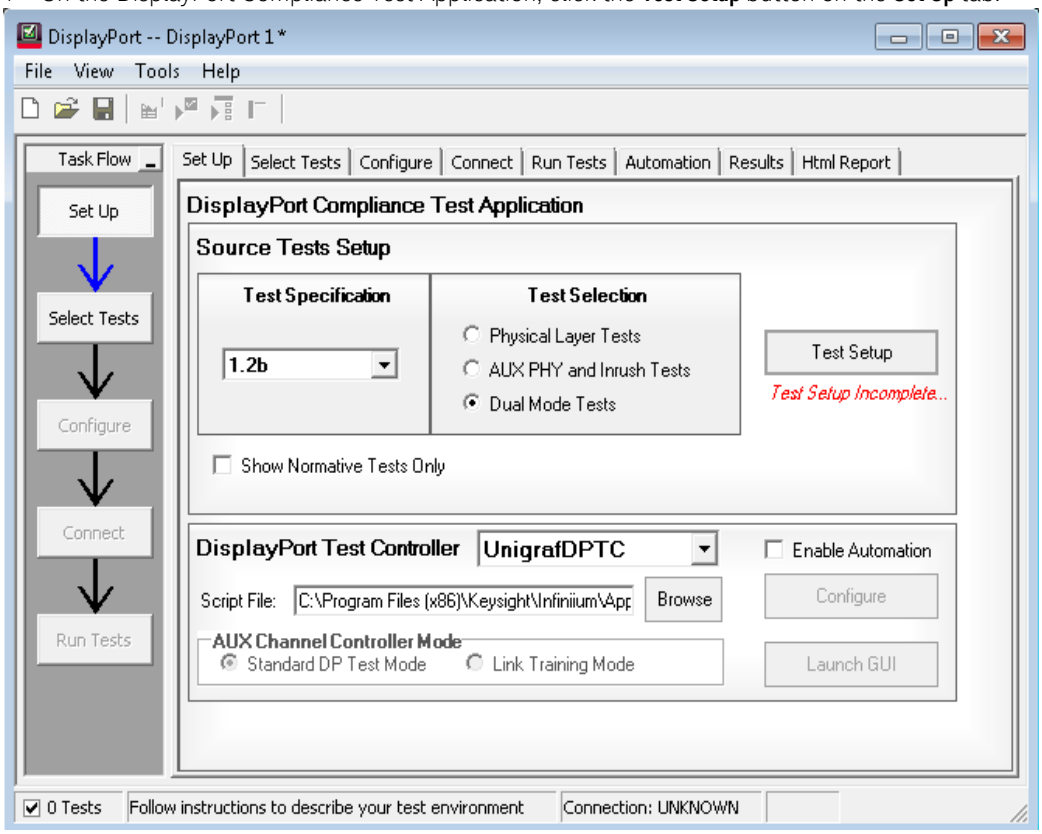
10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

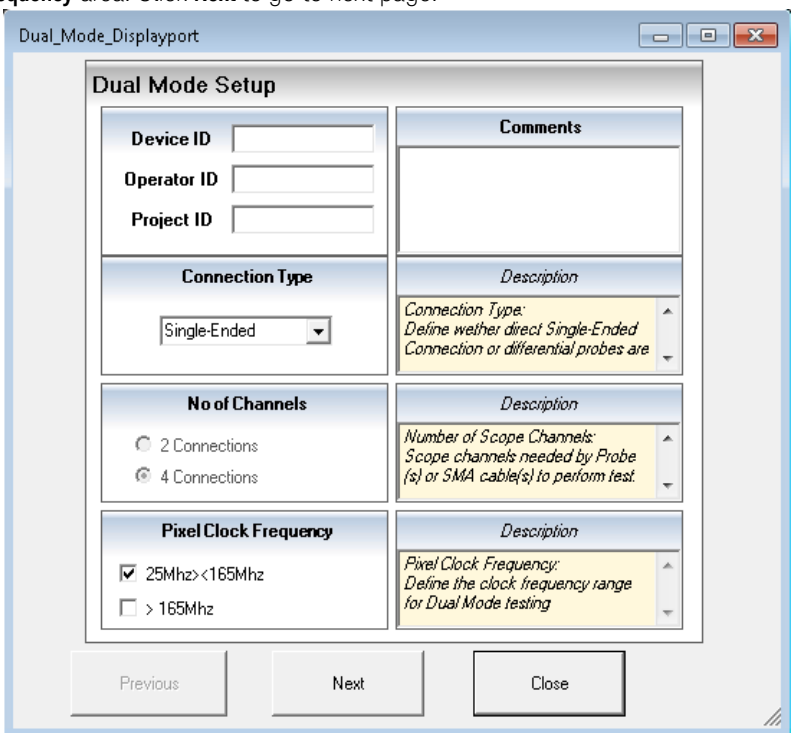
Setting Up for Dual Mode Tests

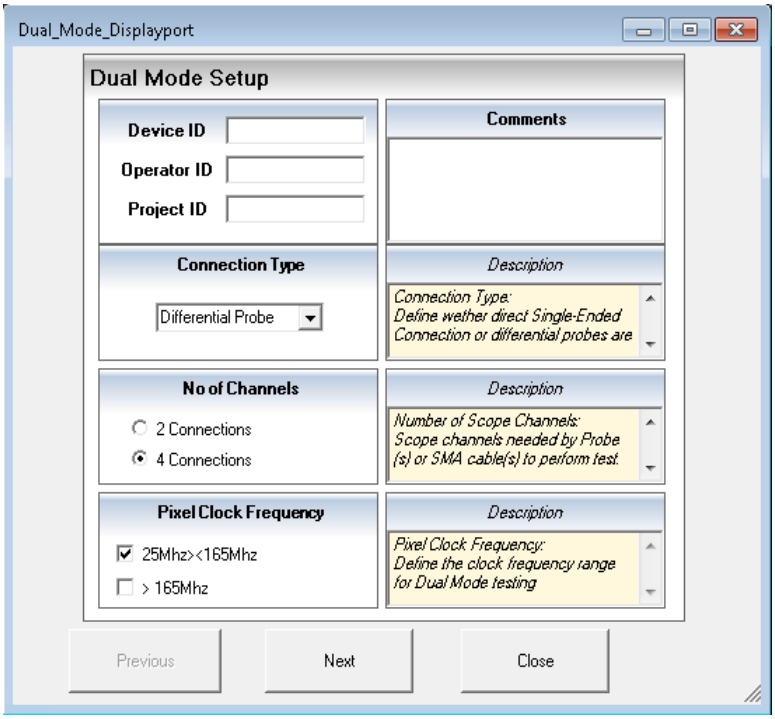
Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

1 On the DisplayPort Compliance Test Application, click the **Test Setup** button on the **Set Up** tab.

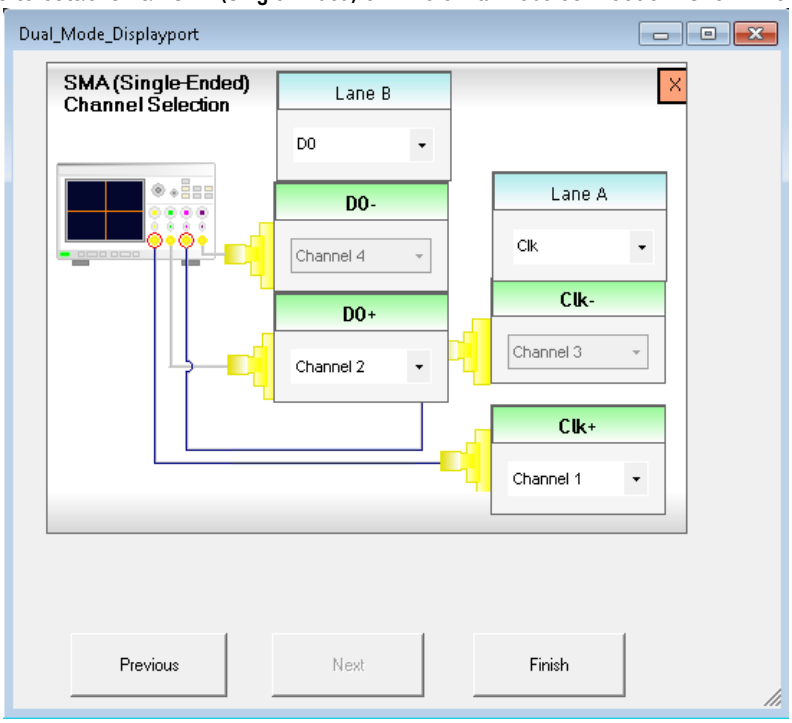


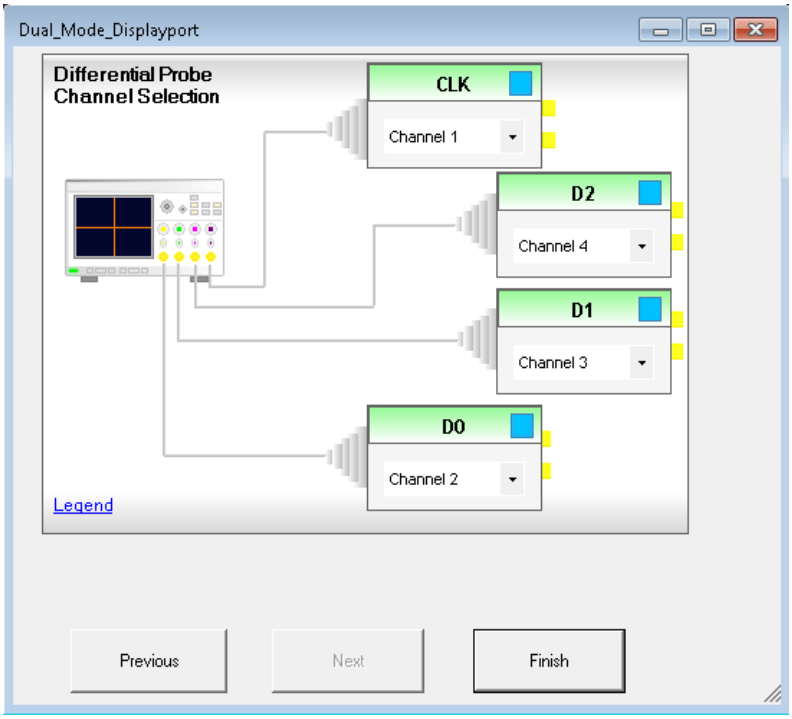
2 On the **Dual Mode Setup** page, select **Single-Ended** or **Differential Probe** from the drop-down in the **Connection Type** area. The option to select the number of oscilloscope channel connections is grayed out if you select **Single-Ended** connection type. For **Differential Probe**, you may choose either a 2-Channel or a 4-Channel setup. Select the clock frequency for Dual Mode signal in the **Pixel Clock Frequency** area. Click **Next** to go to next page.





3 On the **Channel Selection** page, you may assign the data lanes, clock lanes and oscilloscope channels to establish an **SMA (Single-Ended)** or **Differential Probe** connection. Click **Finish**.





Probing/Connection Set Up for Dual Mode Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

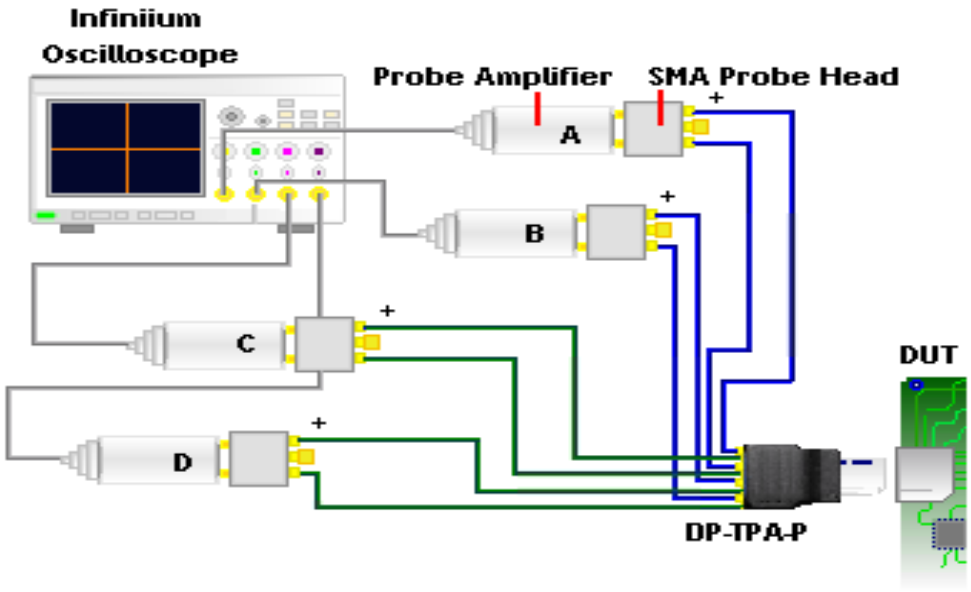


Figure 46 Sample Connection diagram for a 4-Channel Dual Mode Test

Dual Mode TMDS Clock Duty Cycle Test

Test ID

501 – Dual Mode TMDS Clock Duty Cycle (Min)

502 – Dual Mode TMDS Clock Duty Cycle (Max)

Test Overview

The objective of the test is to confirm that the duty cycle of the TMDS Clock waveform of a Source DUT operating in dual mode does not exceed the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_CLOCK

Measurement Procedure

1 Acquire and verify the input TMDS Clock signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Scale the vertical display of the input TMDS Clock signal to optimum value.
   c Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   d Measure the Clock Frequency of the input TMDS Clock signal.
2 Generate FUNC4 signal, which is the differential signal of the TMDS Clock signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit Clock, input TMDS Clock signal).
4 Overlap the TMDS Clock signal to fold the differential signal of the TMDS Clock signal.
   a Acquire the signal until 10,000 clock periods are folded.
5 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the minimum and maximum duty cycle.
   a The minimum duty cycle is measured as the earliest crossing of the TMDS Clock signal falling edge.
   b The maximum duty cycle is measured as the latest crossing of the TMDS Clock signal falling edge.
6 Report the measurement results.

PASS Condition

PASS: 40% < TMDS_CLOCK duty cycle < 60%.

FAIL: TMDS_CLOCK duty cycle < 40% or TMDS_CLOCK duty cycle > 60%

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.18*

Expected/Observable Results

The measured duty cycle of the dual mode TMDS Clock signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode TMDS Clock Jitter Test

Test ID

For 25MHz ≤ TMDS Clock Frequency ≤ 165MHz

- 503 – Dual Mode TMDS Clock Jitter

For TMDS Clock Frequency > 165MHz

- 803 – Dual Mode TMDS Clock Jitter

Test Overview

The objective of the test is to confirm that the TMDS Clock waveform of a Source DUT operating in dual mode does not carry excessive jitter than that defined in the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_CLOCK

Measurement Procedure

1 Acquire and verify the input TMDS Clock signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Scale the vertical display of the input TMDS Clock signal to optimum value.
   c Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   d Measure the Clock Frequency of the input TMDS Clock signal.
2 Generate FUNC4 signal, which is the differential signal of the TMDS Clock signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit Clock, input TMDS Clock signal).
4 Overlap the TMDS Clock signal to fold the differential signal of the TMDS Clock signal.
   a Acquire the signal until 400,000 clock periods are folded.
5 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.
6 Report the measurement results.

PASS Condition

For 25MHz ≤ TMDS Clock Frequency ≤ 165MHz

- PASS: Measured TMDS Clock Jitter ≤ 0.20 Tbit and Data Jitter ≤ 0.25 Tbit

For 165MHz < TMDS Clock Frequency ≤ 300MHz

- PASS: Measured TMDS Clock Jitter ≤ 120 ps and Data Jitter ≤ 150 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.18*
- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured jitter of the dual mode TMDS Clock signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Eye Diagram Test

Test ID

601, 602, 603 – Dual Mode Eye Diagram Testing

Test Overview

The objective of the test is to evaluate the waveform ensuring that the timing variables and amplitude trajectories of a Source DUT operating in dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit First Order PLL, input TMDS Clock signal).
3 Fold the differential signal of the data signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
4 Set up the waveform histogram on the data signal eye diagram to measure the left edge and right edge.
5 Set up the parameter of the Mask Test.
   a Load the Eye mask.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Run the Eye mask until the 400,000 UI are folded.
6 Check for any signal trajectories entering into the mask.
7 Measure the jitter of the eye diagram using the histogram.
8 Measure the eye height of the eye diagram using the histogram.
9 Measure the peak-to-peak voltage at 0.5UI of the eye diagram using the histogram.

10 Overlap the TMDS Clock Signal to fold the differential signal of the data signal.

a Acquire the signal until 400,000 clock period are folded.

11 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.

12 Report the measurement results.

PASS Condition

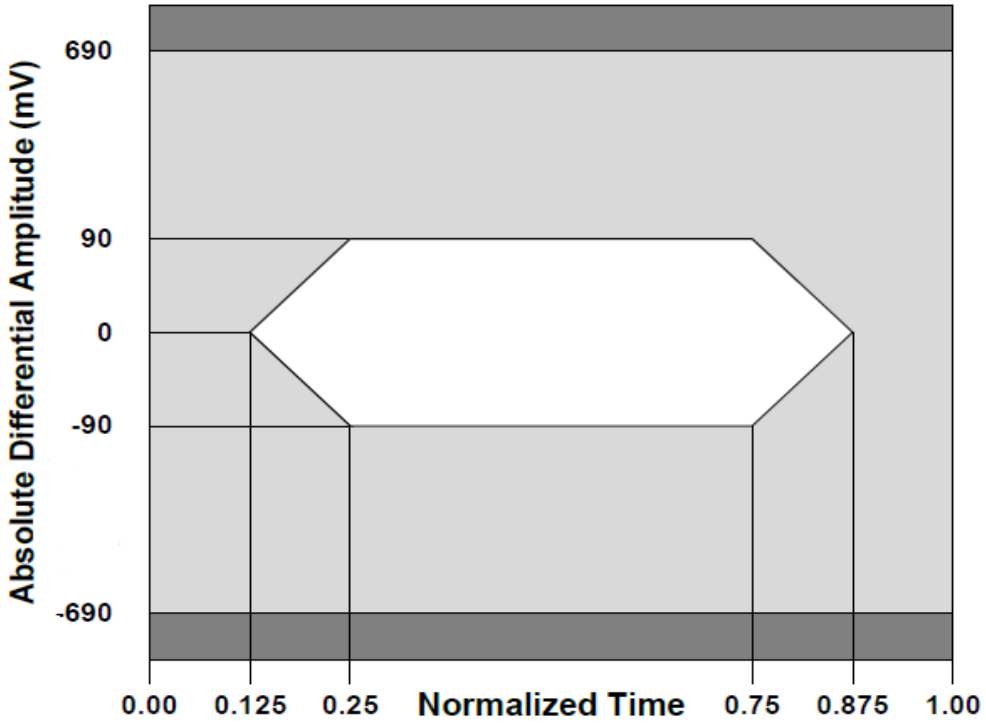


Figure 47 TMDS Data EYE Mask for TMDS Clock Frequencies from 25MHz to 165MHz

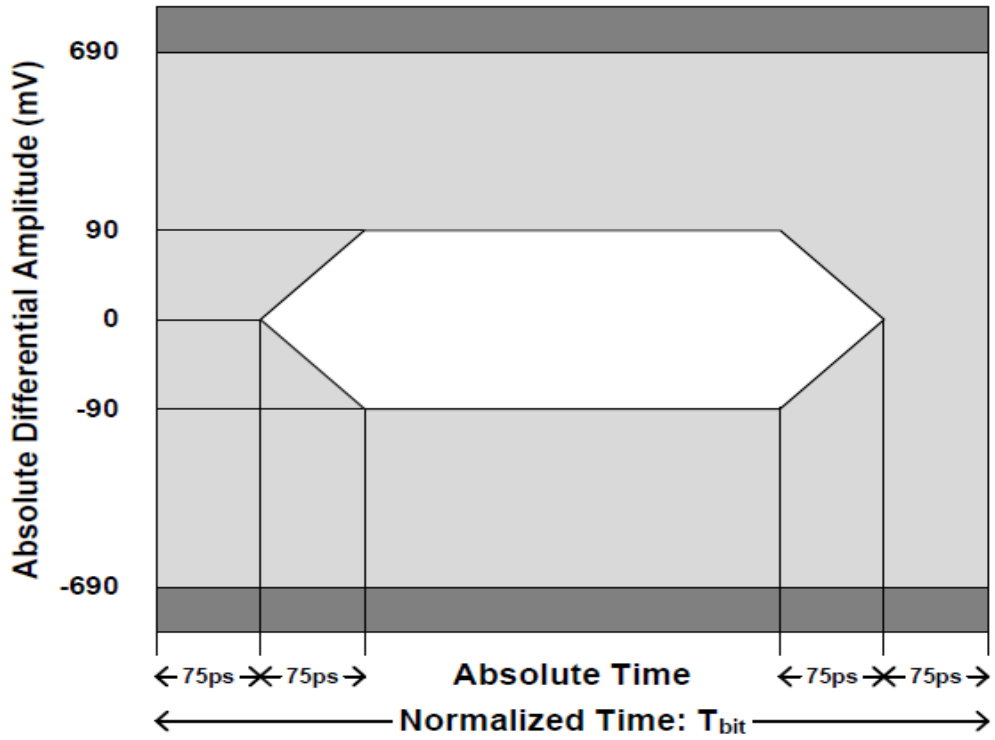


Figure 48 TMDS Data EYE Mask for TMDS Clock Frequencies above 165MHz

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.19*
- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2, Figure 3-10* (for 25MHz < TMDS Clock Frequency < 165MHz) and *Figure 3-11* (for TMDS Clock Frequency > 165MHz)

Expected/Observable Results

The measured eye diagram for the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Dual Mode Data Jitter Test

Test ID

For 25MHz ≤ TMDS Clock Frequency ≤ 165MHz

- 611, 612, 613 – Dual Mode Data Jitter

For TMDS Clock Frequency > 165MHz

- 911, 912, 913 – Dual Mode Data Jitter

Test Overview

The objective of the test is to confirm that the data waveform of a Source DUT operating in dual mode does not carry excessive jitter than that defined in the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit First Order PLL, input TMDS Clock signal).
3 Fold the differential signal of the data signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
4 Set up the waveform histogram on the data signal eye diagram to measure the left edge and right edge.
5 Set up the parameter of the Mask Test.
   a Load the Eye mask.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Run the Eye mask until the 400,000 UI are folded.
6 Check for any signal trajectories entering into the mask.
7 Measure the jitter of the eye diagram using the histogram.

8 Measure the eye height of the eye diagram using the histogram.

9 Measure the peak-to-peak voltage at 0.5UI of the eye diagram using the histogram.

10 Overlap the TMDS Clock Signal to fold the differential signal of the data signal.

a Acquire the signal until 400,000 clock period are folded.

11 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.

12 Report the measurement results.

PASS Condition

For 25MHz $\leq$ TMDS Clock Frequency $\leq$ 165MHz

- PASS: Measured TMDS Clock Jitter $\leq$ 0.20 Tbit and Data Jitter $\leq$ 0.25 Tbit

For 165MHz < TMDS Clock Frequency $\leq$ 300MHz

- PASS: Measured TMDS Clock Jitter $\leq$ 120 ps and Data Jitter $\leq$ 150 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.19*
- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured jitter of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Data Peak-Peak Differential Voltage Test

Test ID

811, 812, 813 – Dual Mode Peak-Peak Differential Voltage (Min)

821, 822, 823 – Dual Mode Peak-Peak Differential Voltage (Max)

Test Overview

The objective of the test is to evaluate and confirm that the data waveform ensuring that the timing variables and amplitude trajectories of a Source DUT operating in a dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit First Order PLL, input TMDS Clock signal).
3 Fold the differential signal of the data signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
4 Set up the waveform histogram on the data signal eye diagram to measure the left edge and right edge.
5 Set up the parameter of the Mask Test.
   a Load the Eye mask.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Run the Eye mask until the 400,000 UI are folded.
6 Check for any signal trajectories entering into the mask.
7 Measure the jitter of the eye diagram using the histogram.
8 Measure the eye height of the eye diagram using the histogram.

9 Measure the peak-to-peak voltage at 0.5UI of the eye diagram using the histogram.

10 Overlap the TMDS Clock Signal to fold the differential signal of the data signal.

a Acquire the signal until 400,000 clock period are folded.

11 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.

12 Report the measurement results.

PASS Condition

For all TMDS Clock Frequencies:

- Minimum Peak-Peak Differential Voltage: 180mV
- Maximum Peak-Peak Differential Voltage: 1380mV

Test References

See:

- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured peak-peak differential voltage of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Inter-Pair Skew Test

Test ID

711 – D0/D1 - Dual Mode Inter Pair Skew Test

712 – D0/D2 - Dual Mode Inter Pair Skew Test

713 – D1/D2 - Dual Mode Inter Pair Skew Test

Test Overview

The objective of the test is to evaluate and confirm that the skew or time delay between differential data lane of a Source DUT operating in a dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input Lane A data signal.
   c Verify the trigger and the amplitude of the input Lane B data signal.
   d Scale the vertical display of the input TMDS Clock signal to optimum value.
   e Scale the vertical display of the input Lane A data signal to optimum value.
   f Scale the vertical display of the input Lane B data signal to optimum value.
   g Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   h Measure V_{TOP} and V_{BASE} of the input Lane A data signal.
   i Measure V_{TOP} and V_{BASE} of the input Lane B data signal.
   j Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
3 Set up the parameter of the Inter Pair Skew measurement.
   a Set up two display grids such that each grid displays one test lane data signal.
   b Set up the measurement threshold of each test lane data signal on the Transition Voltage = 0V.
   c Decode the data signal for each test lane.
   d Search the desired pattern from the decoded data signal.

e Measure the time difference between the corresponding edges of both the test lanes using the equation:

$$T_{Transition\_LaneA} - T_{Transition\_LaneB}$$

f Repeat the previous step until you measure 100 edges.

g Calculate the Inter Pair Skew using the equation:

$$\text{Inter Pair Skew} = \{1/\text{Number of Edges}\} \sum |T_{Transition\_LaneA} - T_{Transition\_LaneB}|$$

4 Report the measurement results.

PASS Condition

For all TMDS Clock Frequencies, Inter-Pair Skew $\leq$ 976 ps

Test References

See:

- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured inter pair skew of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Intra-Pair Skew Test

Test ID

701, 702, 703 – Dual Mode Intra Pair Skew Test

Test Overview

The objective of the test is to evaluate and confirm that the skew or time delay between the respective sides of the differential data lane of a Source DUT operating in a dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
3 Set up the parameter to perform High Level Voltage (V_{High}) and Low Level Voltage (V_{Low}) for each single-ended data signal:
   a Scale the vertical display of the single-ended input data signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find V_{High} by measuring the average voltage at 0.6UI to 0.75UI of the High level.
   d Find V_{Low} by measuring the average voltage at 0.6UI to 0.75UI of the Low level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{High} + V_{Low})/2$$

4 Set up the parameter of the Intra Pair Skew measurement.

a Set up measurement threshold od each single-ended data signal based on the Transition Voltage measured.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure the time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge using the equation:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure the time difference between the falling edge of the data true signal (D+) and the complement's (D-) falling edge using the equation:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the Intra Pair Skew using the equation:

$$\text{Intra Pair Skew} = \{1/\text{Number of Edges}\} \sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})]/2\}$$

5 Report the measurement results.

PASS Condition

For all TMDS Clock Frequencies, Intra-Pair Skew $\leq$ 60 ps

Test References

See:

- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured intra pair skew of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

9 DisplayPort 1.3 Source Tests

Overview

This section describes the normative and informative main link physical layer tests for compliance verification of DisplayPort 1.3 source, sink and cable devices.

Test Point Definition for DisplayPort 1.3 Tests

Five different test points are identified for the physical layer measurement. See Figure 49.

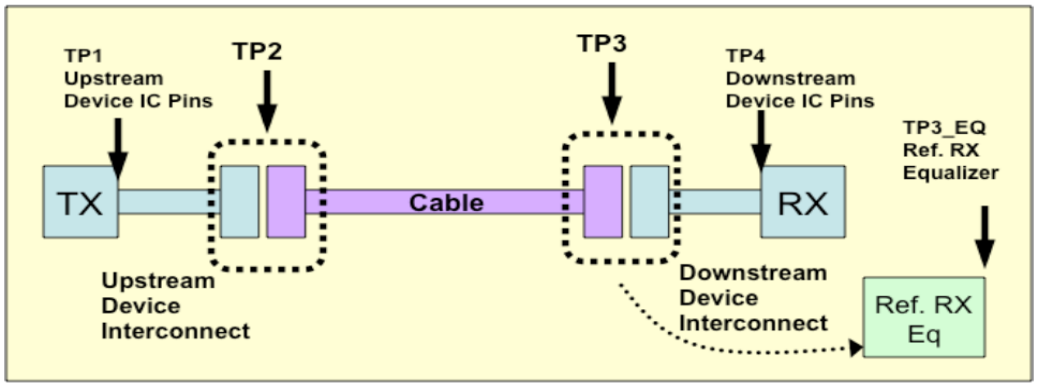


Figure 49 Test Points in a DisplayPort InterConnect System

Table 44 defines the Test Points used for various DisplayPort 1.3 Tests:

Table 44 Test Points for DisplayPort Tests

Test Point	Description
TP1	At the pins of the Transmitter Device
TP2	At the test interface on a test access fixture as close as possible to the DP mated connection to a Source device
TP3	At the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device
TP3_EQ	At TP3, when a defined cable model with equalizer is applied. There are two defined cable models: ▪ Worst Cable Model as defined in VESA DisplayPort 1.3 Standard, ▪ Zero length, zero loss cable. The equalizer is also defined in VESA DisplayPort 1.3 Standard
TP4	At the pins of a receiving device

Cable Models

The two cable models defined in VESA DisplayPort 1.2a Standard (that are used for DisplayPort 1.3 also) are:

1 Worst Case Cable Model—To achieve the TP3_EQ signal with the worst case cable model:

- Acquire the signal at TP2.
- Embed the TP2 signal with a “worst case” HBR cable model using an InfiniiSim Waveform Transformation Toolset software to emulate the insertion loss as defined in Figure 4-10 of the VESA DisplayPort 1.2a Standard.
  - For the DisplayPort Compliance Test Application, the “*CIC_rev0p6.s4p*” cable model transfer function is used.

- Finally, apply the HBR, HBR2 or HBR3 equalization using the Serial Data Equalization software as defined in Figure 3-34 (for HBR), Figure 3-33 (for HBR2), Figure 3-31 and Figure 3-32 (for HBR3) of the VESA DisplayPort 1.3 Standard.

2 Zero Length Cable Model—To achieve the TP3_EQ signal with the zero length cable model:

- Acquire the signal at TP2.
- No cable model is embedded for the Zero Length cable model.
- Finally, apply the HBR, HBR2 or HBR3 equalization using the Serial Data Equalization software as defined in Figure 3-34 (for HBR), Figure 3-33 (for HBR2), Figure 3-31 and Figure 3-32 (for HBR3) of the VESA DisplayPort 1.3 Standard.

Equalization

When equalization is required, use the CTLE (Continuous Time Linear Equalization) transfer function, as given in Figure 3-34 (for HBR), Figure 3-33 (for HBR2), Figure 3-31 (for HBR3) and the DFE (Decision Feedback Equalization) transfer function as in Figure 3-32 (for HBR3) of the VESA DisplayPort 1.3 Standard.

For main link, use the CTLE model or the DFE model with the following transfer function for HBR (2.7 Gbps):

The HBR Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2} \cdot \sqrt{\omega^2 + \omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.725 \times 10^9)$$

$$\omega_{p1} = 2\pi(1.35 \times 10^9)$$

$$\omega_{p2} = 2\pi(2.5 \times 10^9)$$

Figure 50 Transfer Function of the CTLE/DFE model for HBR

Table 45 CTLE Model for HBR

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.725 GHz	0.725 GHz
Pole 1 Frequency	1.35 GHz	1.35 GHz
Pole 2 Frequency	2.5 GHz	2.5 GHz

For main link, use the CTLE model or the DFE model with the following transfer function for HBR2 (5.4 Gbps):

The HBR2 Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 51 Transfer Function of the CTLE/DFE model for HBR2

Table 46 CTLE Model for HBR2

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.64 GHz	0.64 GHz
Pole 1 Frequency	2.7 GHz	2.7 GHz
Pole 2 Frequency	4.5 GHz	4.5 GHz

For main link, use the CTLE model or the DFE model with the following transfer function for HBR3 (8.1 Gbps):

The HBR3 CTLE Reference Equalizer transfer function is given by:

$$H(s) = \frac{\omega p1\ \omega p2}{\omega z} \cdot \frac{s + \omega z}{(s + \omega p1)(s + \omega p2)}$$

Which has magnitude given by:

$$|H(j\omega)| = \frac{\omega p1\ \omega p2}{\omega} \cdot \frac{\sqrt{\omega^2 + \omega z^2}}{\sqrt{\omega^2 + \omega p1^2} \cdot \sqrt{\omega^2 + \omega p2^2}}$$

where:

$$\omega z = 2\pi(0.505 \times 10^9)$$

$$\omega p1 = 2\pi(3.033 \times 10^9)$$

$$\omega p2 = 2\pi(6.000 \times 10^9)$$

Figure 52 Transfer Function of the CTLE/DFE model for HBR3

Table 47 CTLE Model for HBR3

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.505 GHz	0.505 GHz
Pole 1 Frequency	3.033 GHz	3.033 GHz
Pole 2 Frequency	6.0 GHz	6.0 GHz

HBR3 Reference DFE: The HBR3 Reference Equalizer includes a CTLE cascaded with a one-tap adaptive DFE with a coefficient limited to less than 50mV. The DFE behavior is described as:

$$y_k = x_k - d1 sgn(y_{k-1})$$

where, y_k is the DFE differential output voltage, y_k* is the decision function output voltage, x_k is the differential input voltage after CTLE, d1 is the feedback coefficient, k is the UI sample.

A flowchart representing the HBR3 Reference Equalizer is shown in Figure 53.

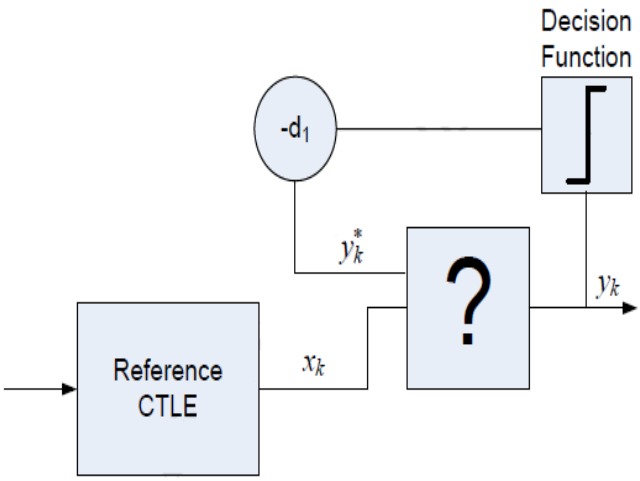


Figure 53 HBR3 Reference Equalizer based on the DFE

Table 48 DFE Model for HBR2

DFE Parameter	Value
Number of Taps	1
DFE Mode	Auto
Eye Width	0.0 UI
Max Tap value	0.050
Min Tap value	0.0

Clock Recovery

When Clock Recovery is required, the clock recovery technique follows the definition of the receiver PLL as defined in Section 3.5.2.5 of the VESA DisplayPort 1.3 Standard. For main link, use the second-order clock recovery function with a closed loop tracking bandwidth and damping factor, with respect to the PRBS7 pattern, as shown in Table 49:

Table 49 Main Link Second-Order Clock Recovery Function

Bit Rate	Bandwidth	Damping Factor
HBR3 (8.1 Gbps)	15 MHZ	1.00
HBR2 (5.4 Gbps)	10 MHz	1.00
HBR (2.7 Gbps)	10 MHz	1.51
RBR (1.62 Gbps)	5.4 MHz	1.51

Test Point Definition for DisplayPort 1.3 Source Tests

Test the Source DUT at Test Point 2 (TP2) as shown in Figure 54. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

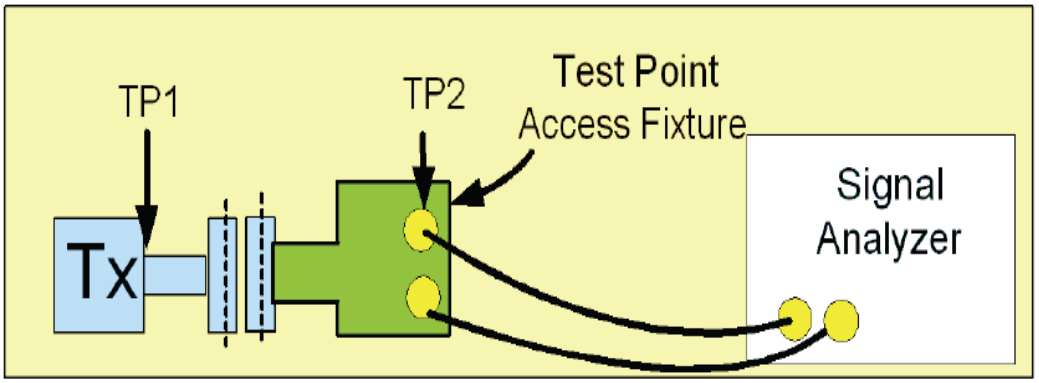


Figure 54 Test Point 2 Connection for DisplayPort 1.3 Source Tests

Table 50 defines the test point fixtures and instruments used for DisplayPort 1.3 Source Tests:

Table 50 Test Point Fixtures and Instruments for DisplayPort 1.3 Source Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters. ▪ For DisplayPort Type-C Connector ▪ N7015A Type-C High-Speed Test Fixture
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 55).

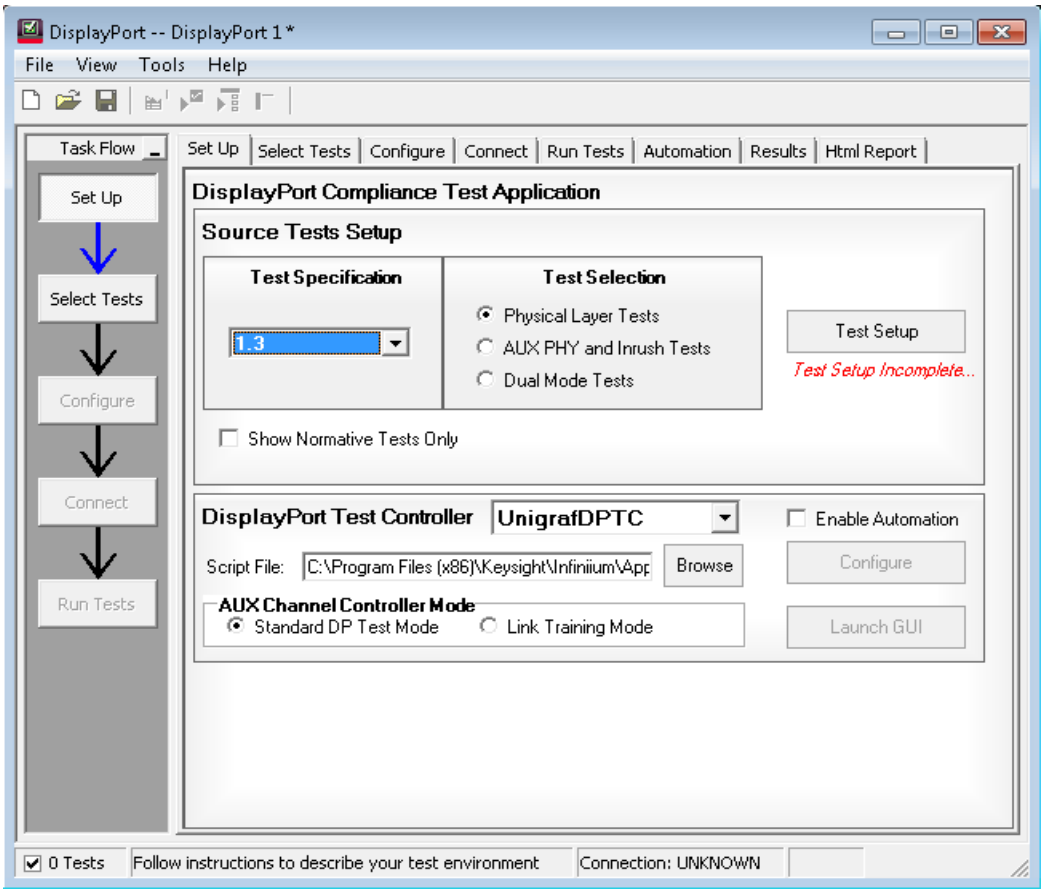


Figure 55 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.3 Standards, select **1.3** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.3 Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

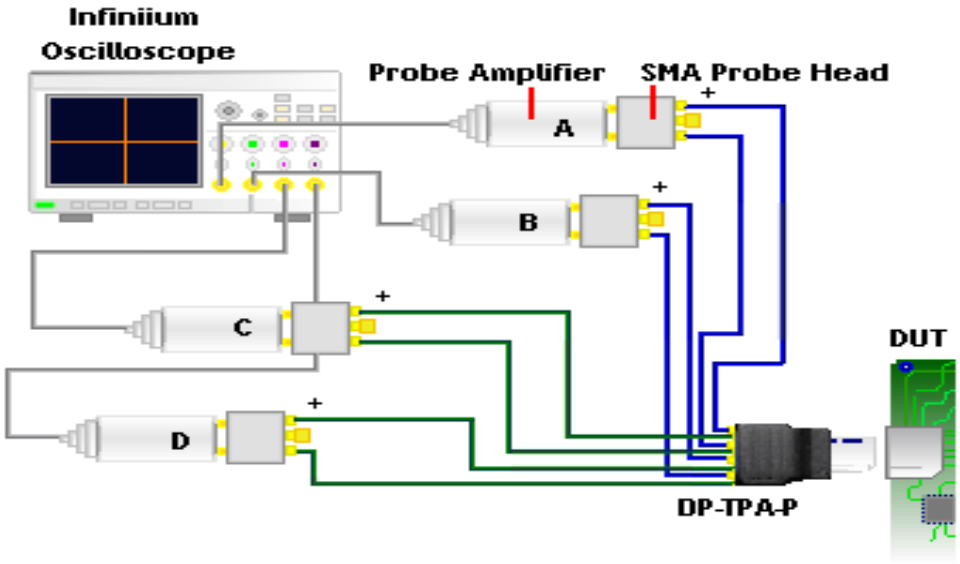


Figure 56 Sample connection diagram for DisplayPort 1.3 Source Tests

Source Eye Diagram Test

Test ID

For Standard DP Pattern:

- 1210001, 1210002, 1210003, 1210004 – Eye Diagram Test

For Arbitrary Pattern:

- 1310001, 1310002, 1310003, 1310004 – Eye Diagram Test

Test Overview

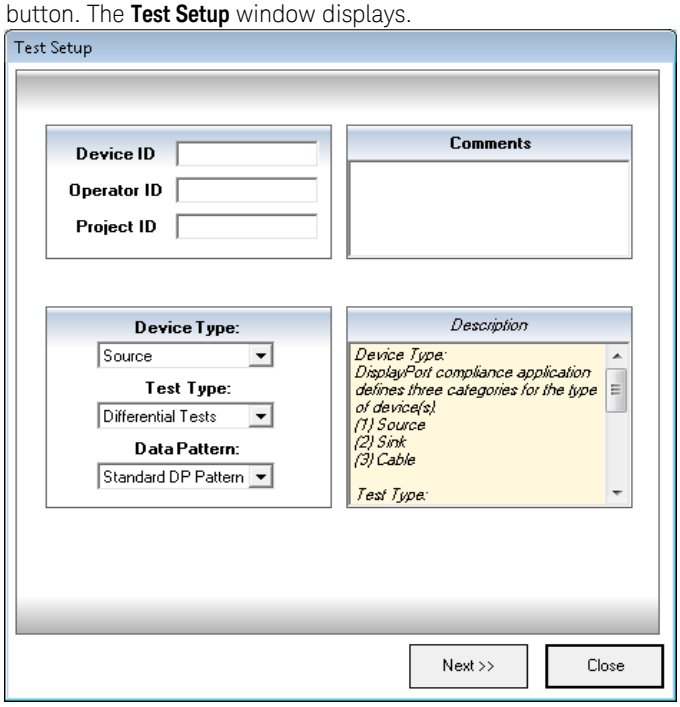
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



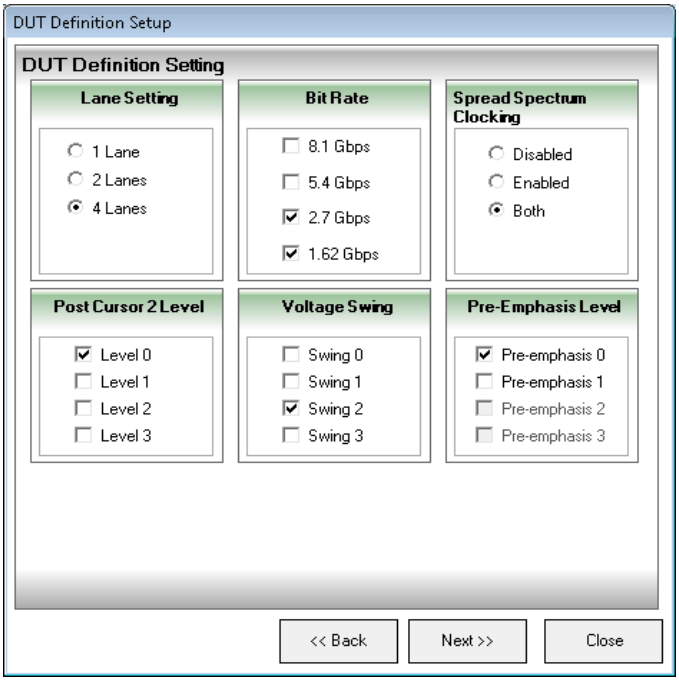
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

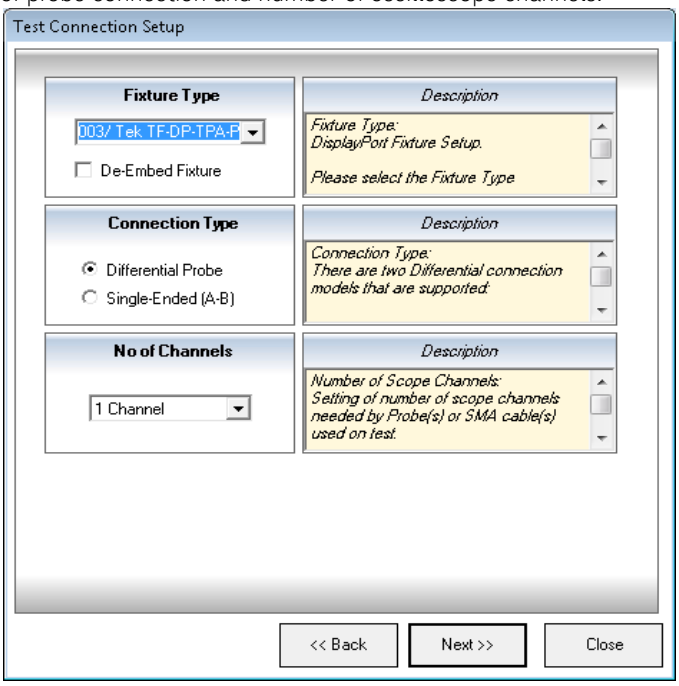
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

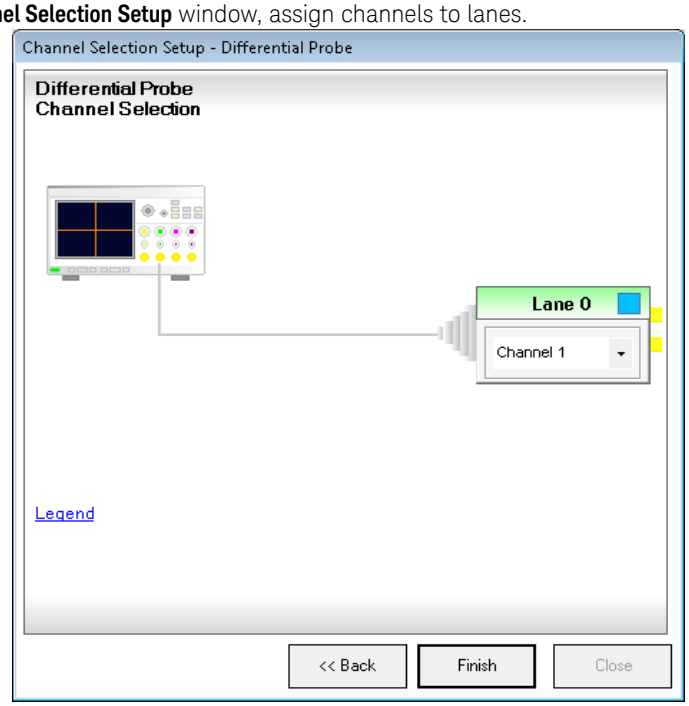
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

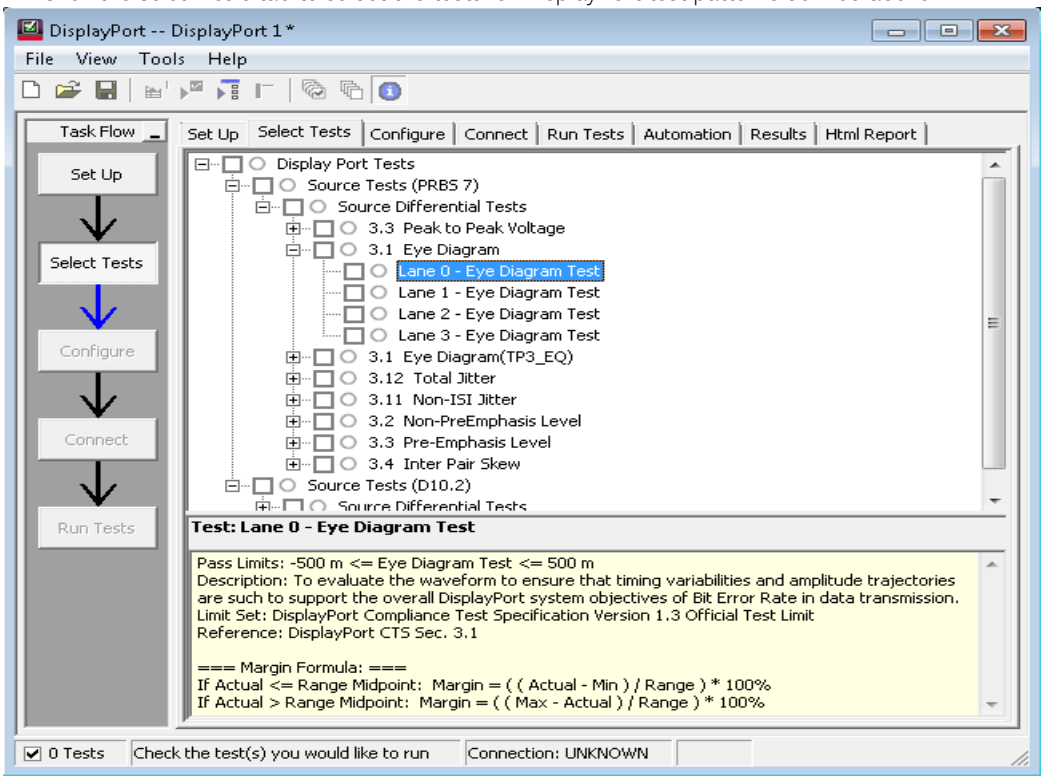


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.
11 Check for any signal trajectories that may have entered into the mask.
12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 51 shows the voltage and time coordinates for the mask used in the eye diagram.

Table 51 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	High (2.7 Gb/s)
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

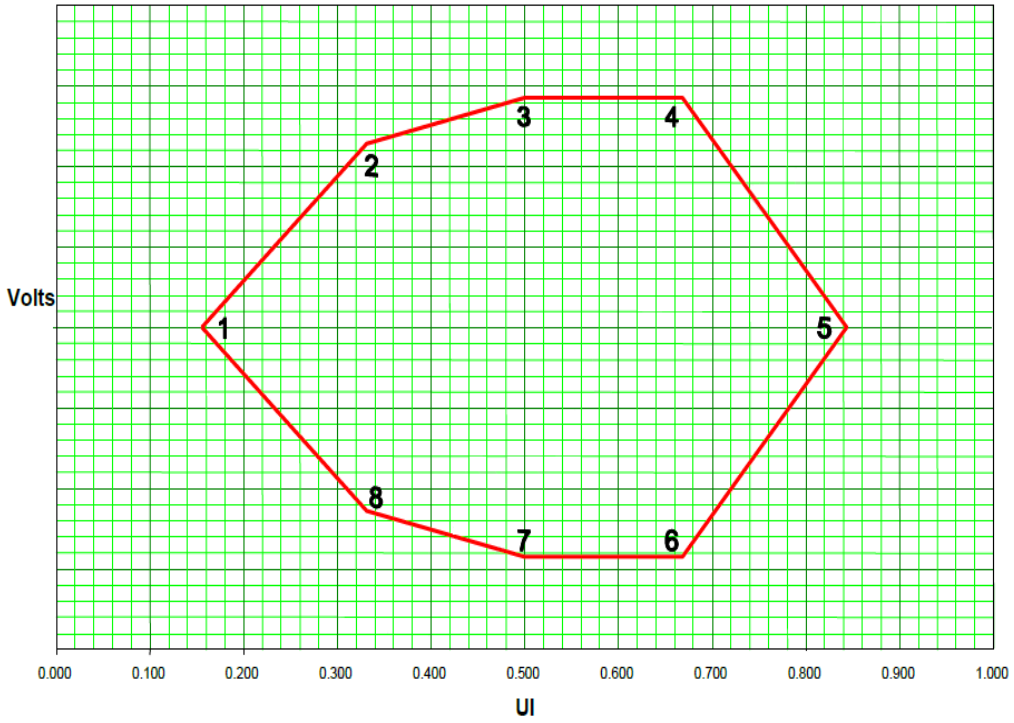


Figure 57 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1.3, Section 3.5.2.8.2, Table 3-20 for RBR, Table 3-19 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

For Standard DP Pattern:

- 1220001, 1220002, 1220003, 1220004 – Total Jitter Test

For Arbitrary Pattern:

- 1320001, 1320002, 1320003, 1320004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

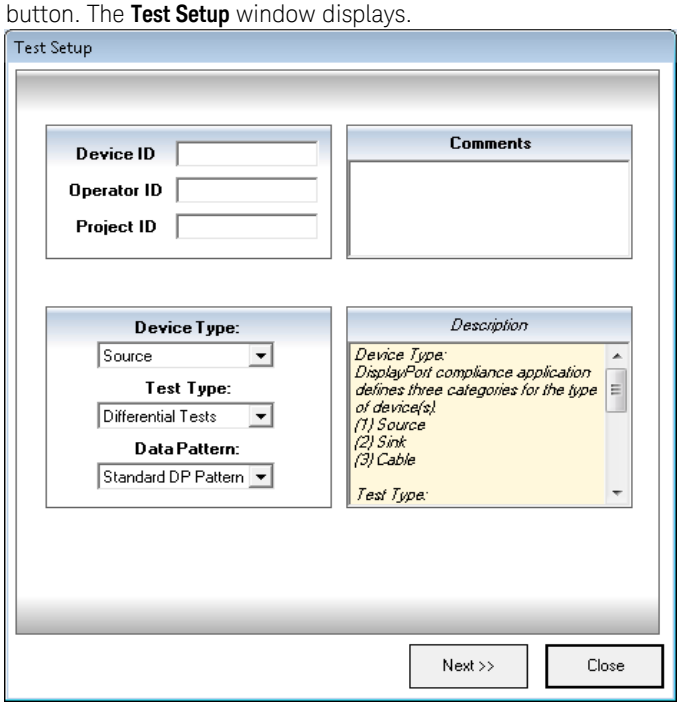
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



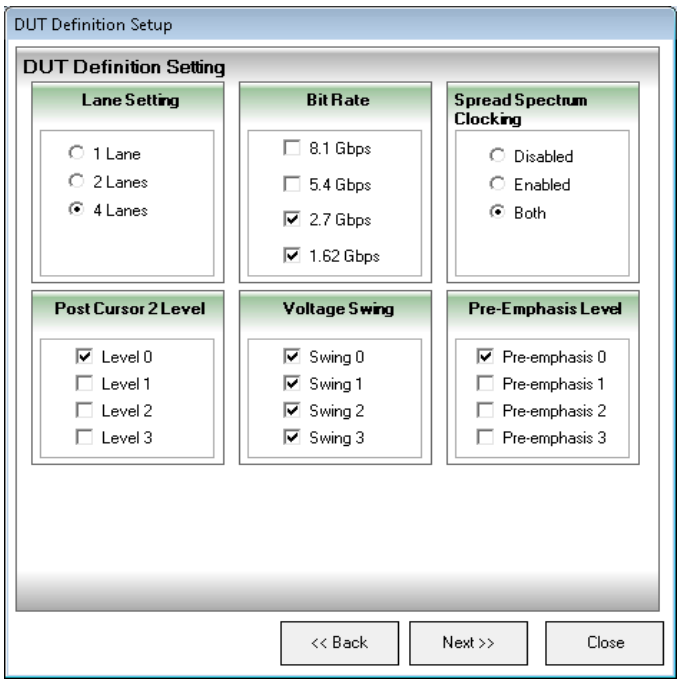
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

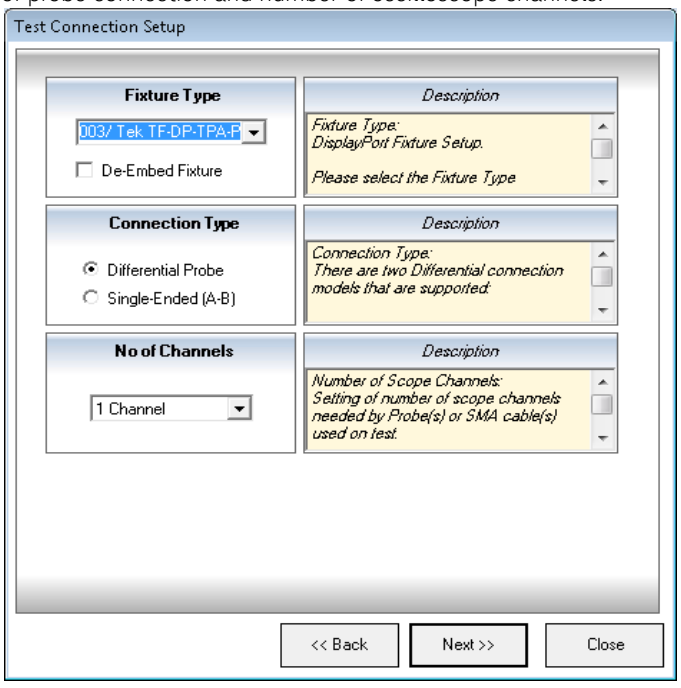
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

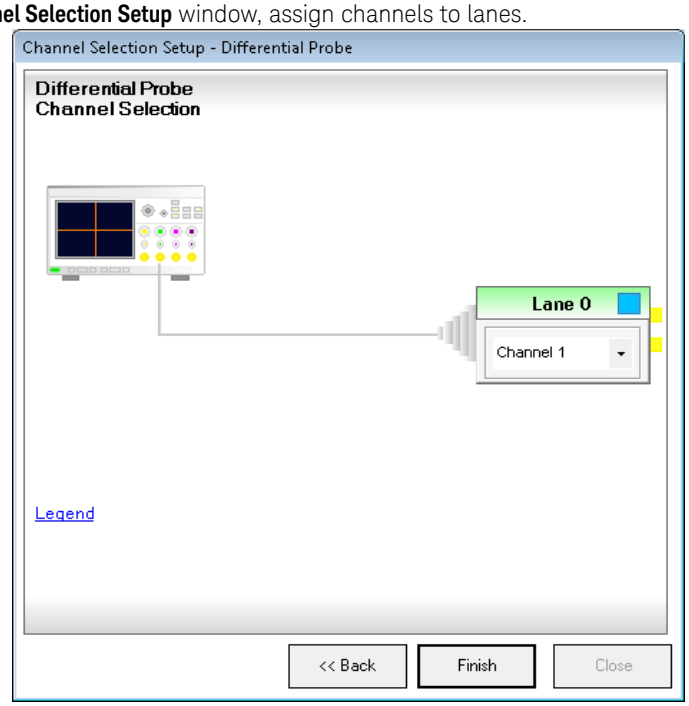
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

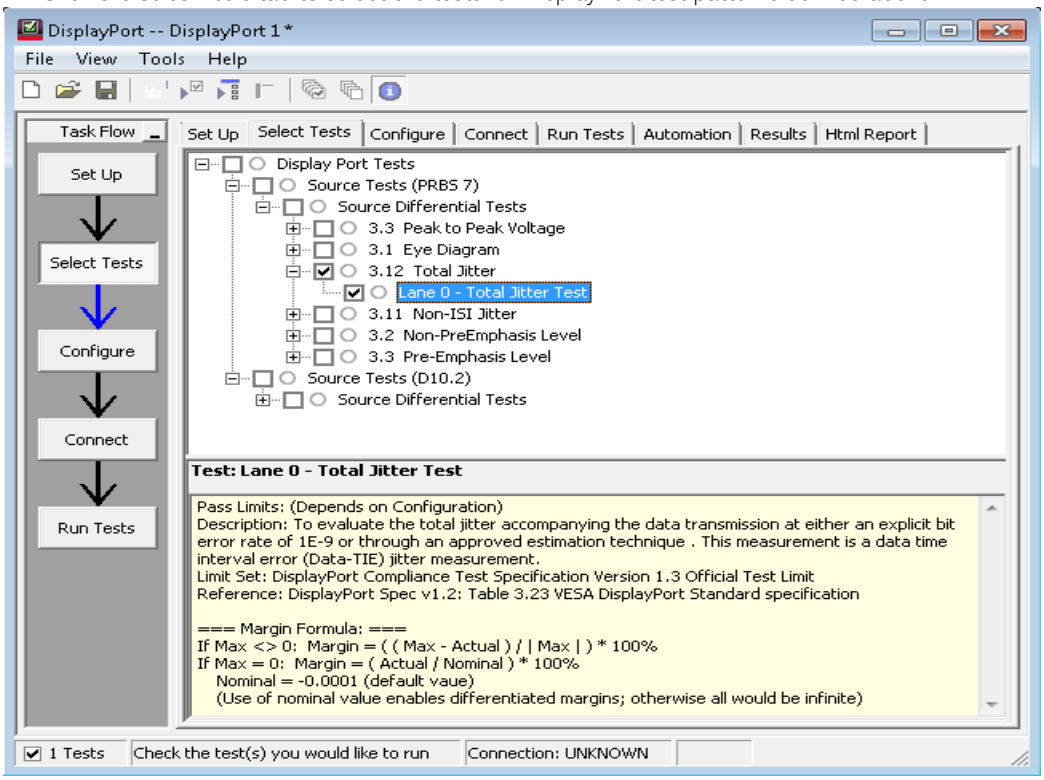


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 52 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
Ap-p	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
Ap-p	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2.7.2, Table 3-15*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non-ISI Jitter Test

Test ID

For Standard DP Pattern:

- 1230001, 1230002, 1230003, 1230004 – Non ISI Jitter Test

For Arbitrary Pattern:

- 1330001, 1330002, 1330003, 1330004 – Non ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

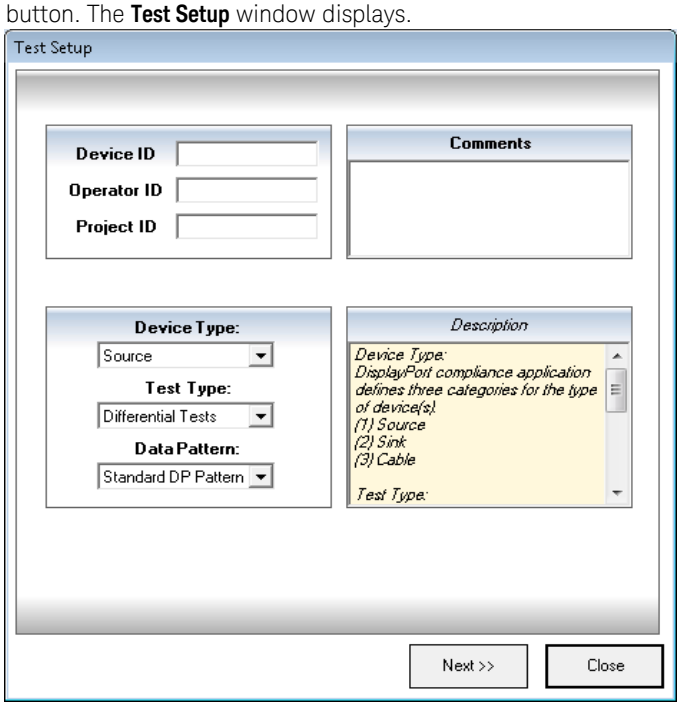
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



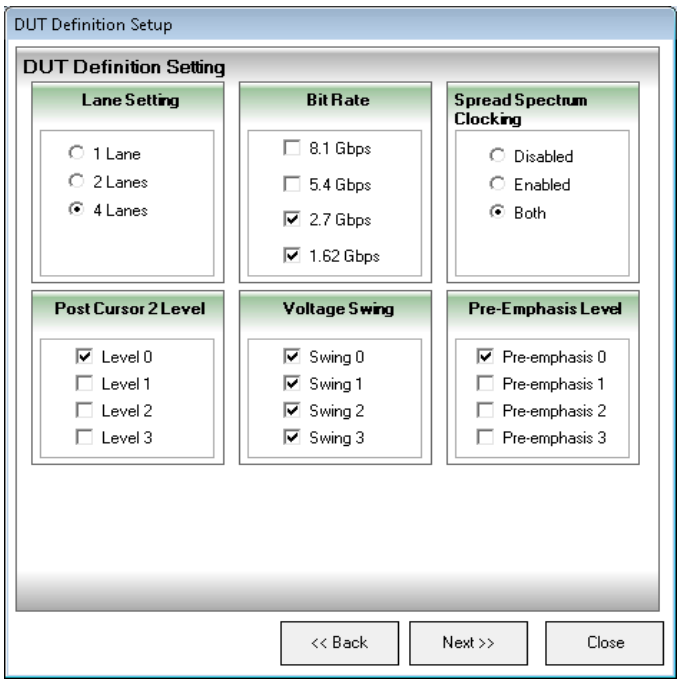
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

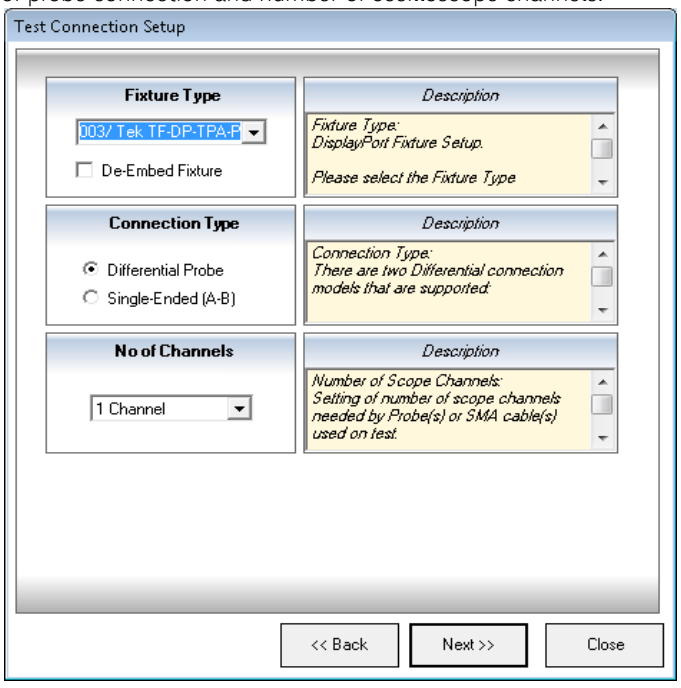
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

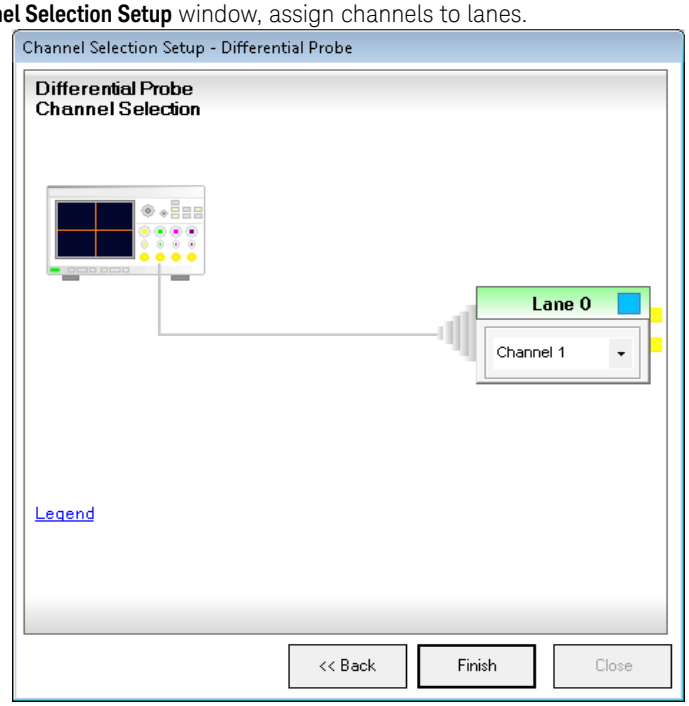
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

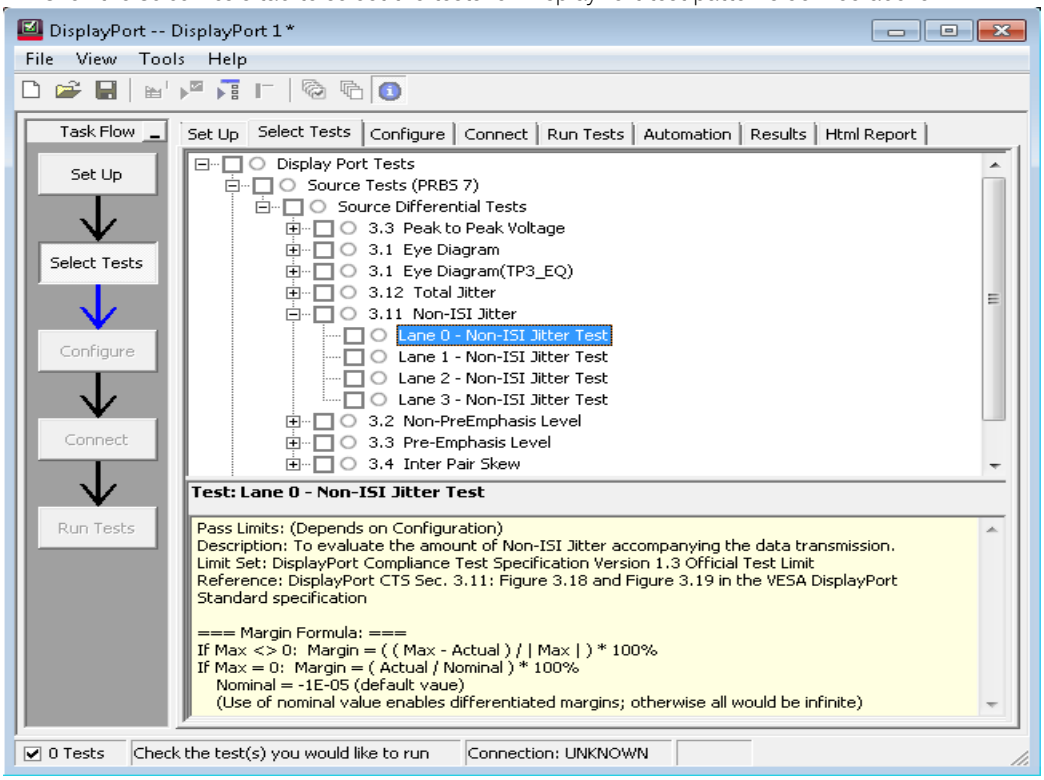


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = TJ - ISI$$

7 Report the measurement results.

PASS Condition

Table 53 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.170 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.11*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2.7.2, Table 3-15*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1261001, 1261002, 1261003, 1261004 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001, 1262002, 1262003, 1262004 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001, 1263002, 1263003, 1263004 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1264101, 1264102, 1264103, 1264104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101, 1262102, 1262103, 1262104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101, 1263102, 1263103, 1263104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For Arbitrary Pattern:

- 1364101, 1364102, 1364103, 1364104 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1362101, 1362102, 1362103, 1362104 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1363101, 1363102, 1363103, 1363104 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

Test Overview

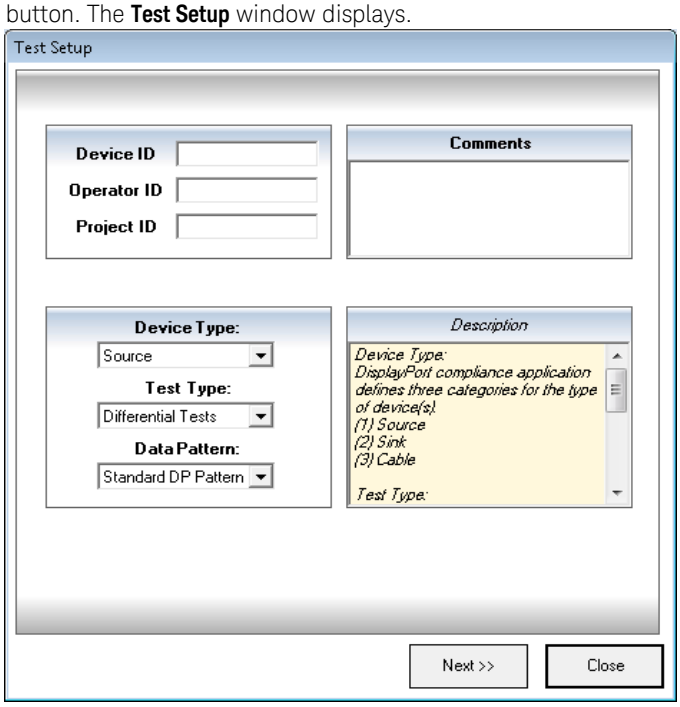
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



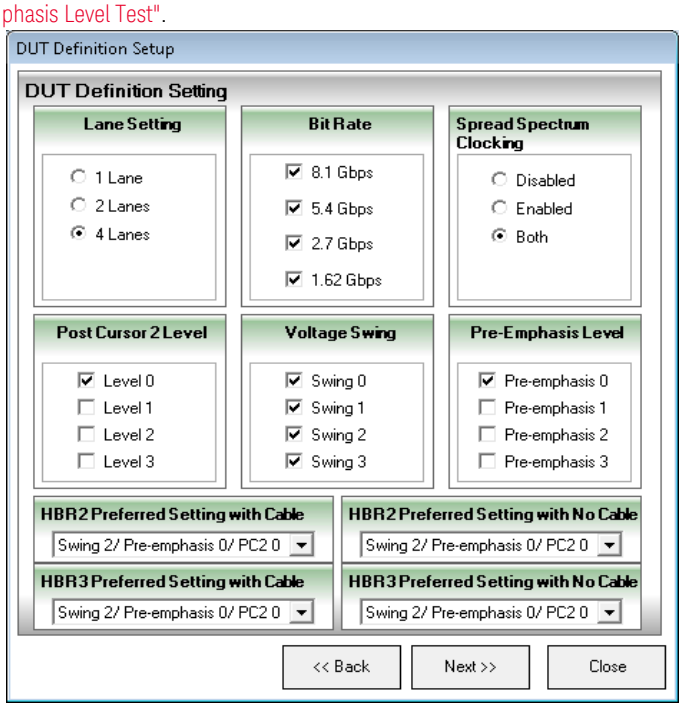
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

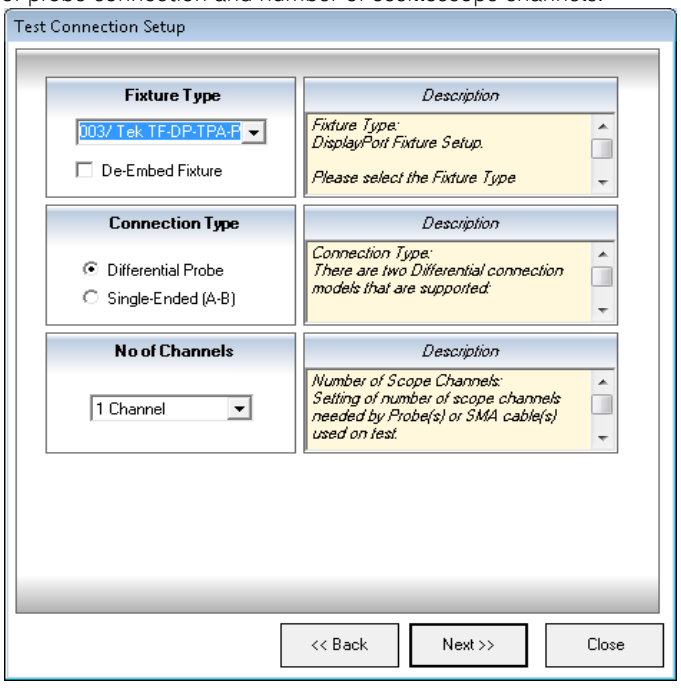
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

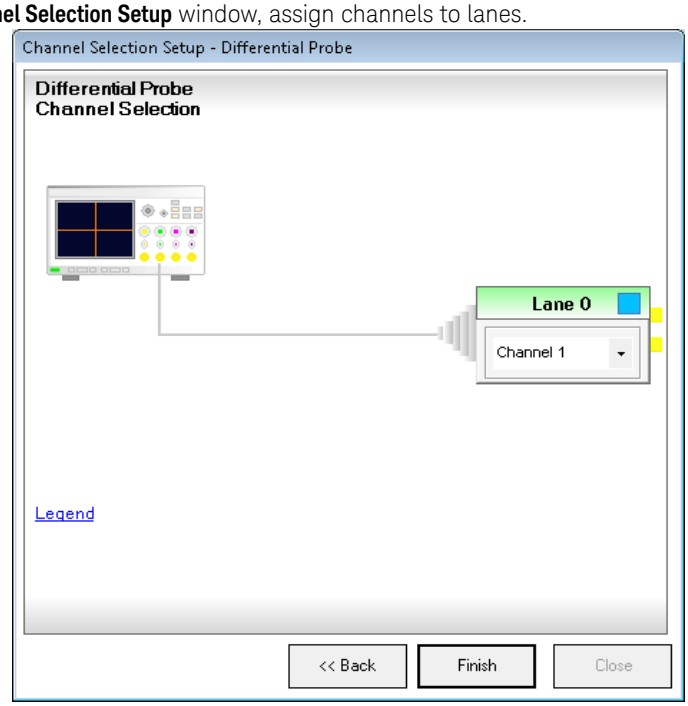
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non Pre-Emphasis Level Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

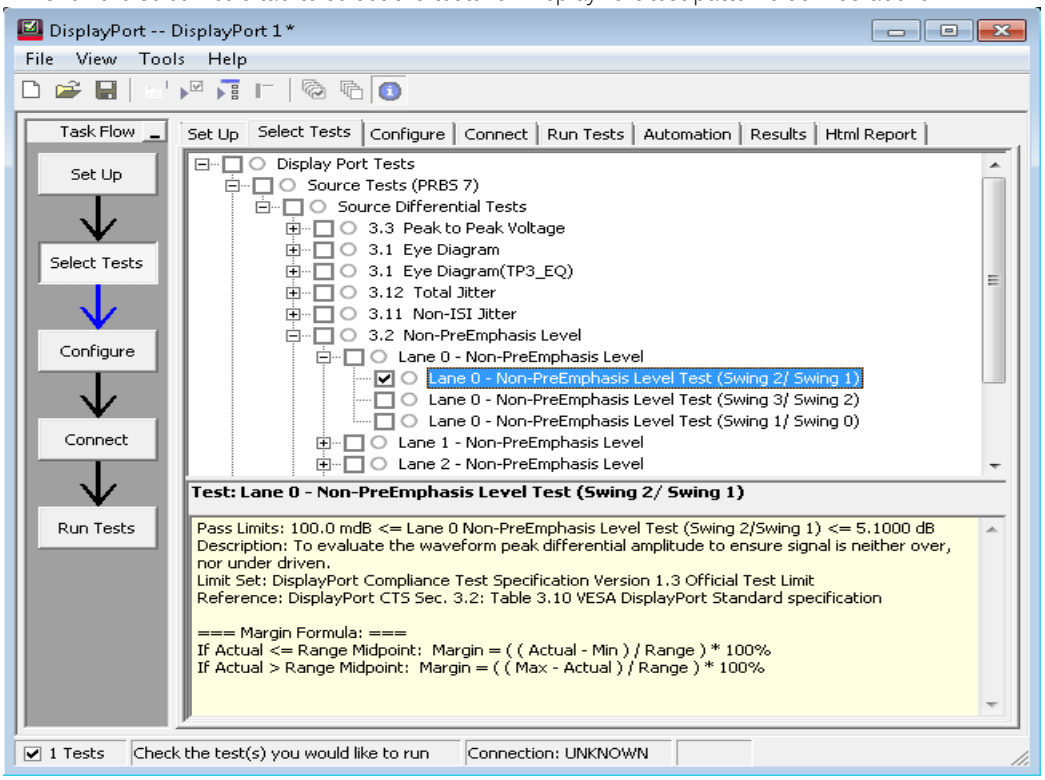


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

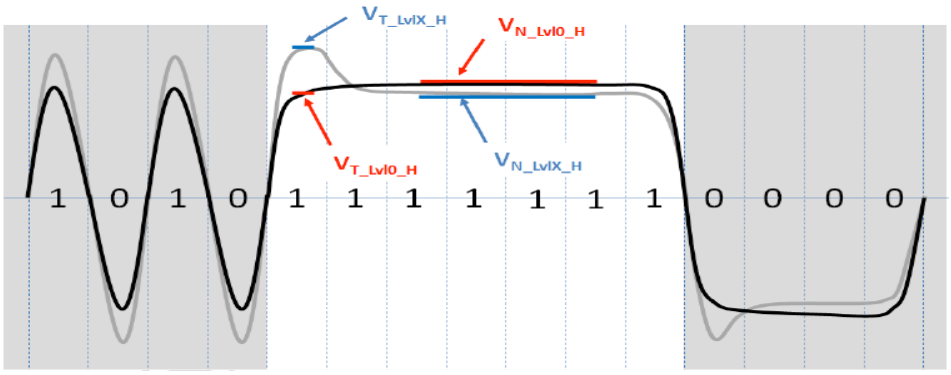


Figure 58 High Voltage measurement for RBR and HBR

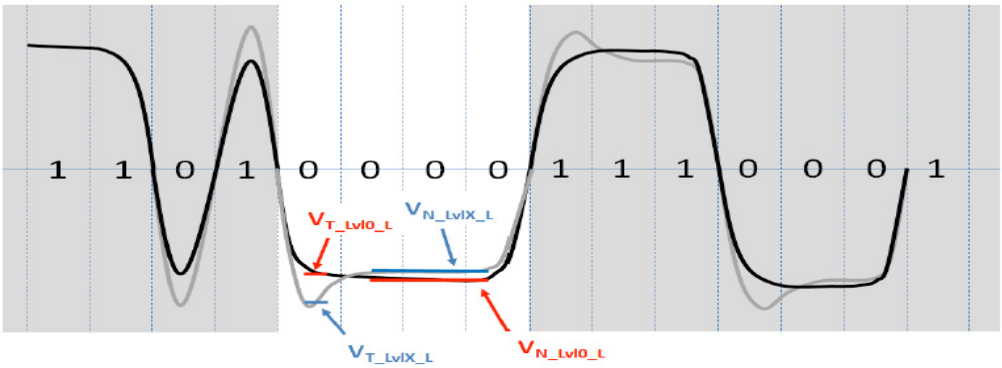


Figure 59 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

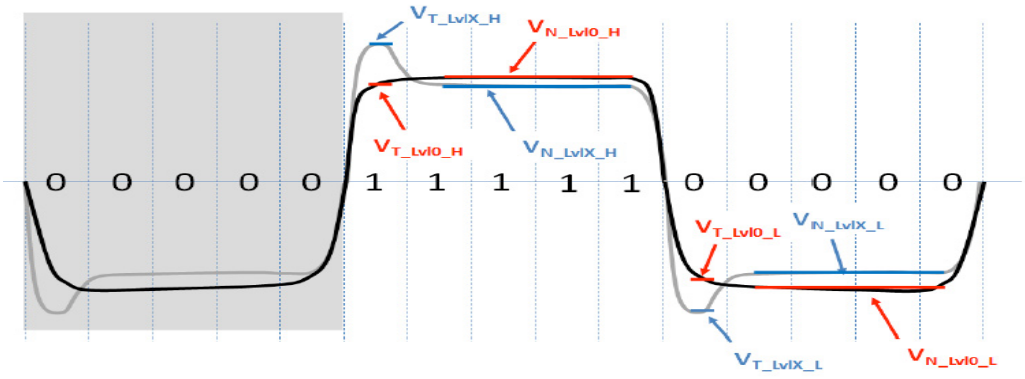


Figure 60 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * Log_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

Resultant = $20 * Log_{10}[\text{Voltage}_{\text{Peak-Peak\_LevelA}} / \text{Voltage}_{\text{Peak-Peak\_LevelB}}]$

Table 54 Compared Levels

Measurement#	$\text{Voltage}_{\text{Peak-Peak\_LevelA}}$	$\text{Voltage}_{\text{Peak-Peak\_LevelB}}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
HBR2 and HBR3		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
* if device optionally capable of Level 3		

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1 dB ≤ Resultant ≤ 4.4 dB

Table 55 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$*	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting. Support for Voltage Level 3 is optional.
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	

* Earlier versions of DisplayPort have the Main-Link DPTX output voltage ratios to ensure that the DPTX supports the required range of output voltage levels. For HBR2 and higher, you need not test or specify exclusively because the compliance test point is moved to TP3_EQ. So, the ratio of output voltage levels is removed from the table above for HBR2 and above.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.2*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-10*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1270001, 1270002, 1270003, 1270004 – Pre-Emphasis Level Test

For Standard DP Pattern (HBR2 and HBR3):

- 1270501, 1270502, 1270503, 1270504 – Pre-Emphasis Level Test

For Arbitrary Pattern:

- 1370501, 1370502, 1370503, 1370504 – Pre-Emphasis Level Test

Test Overview

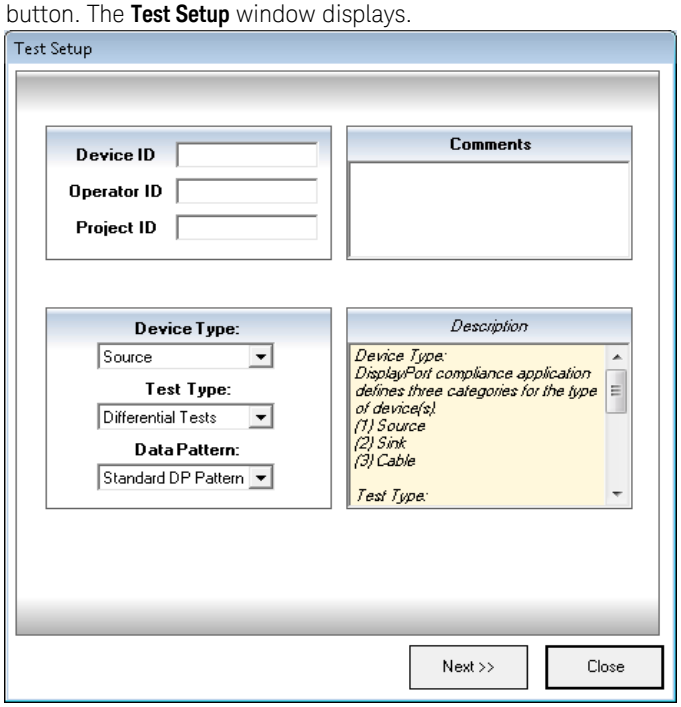
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.3 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3– PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



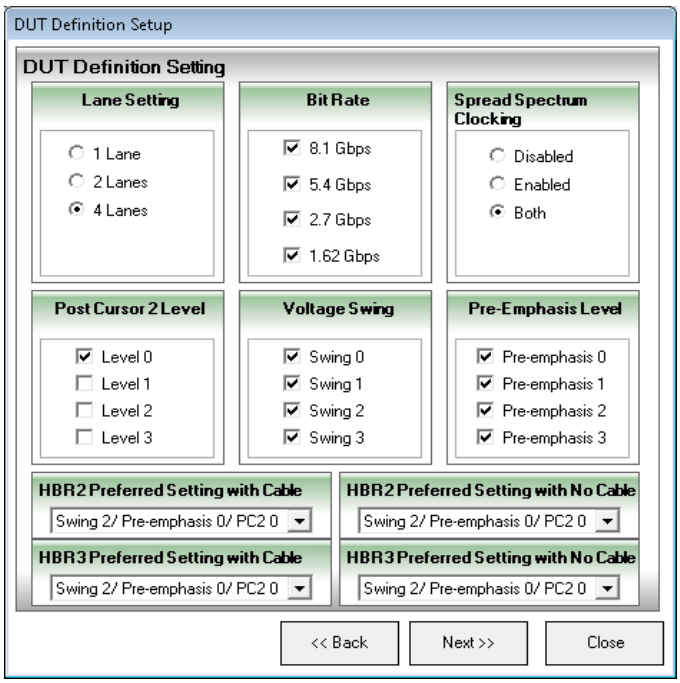
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

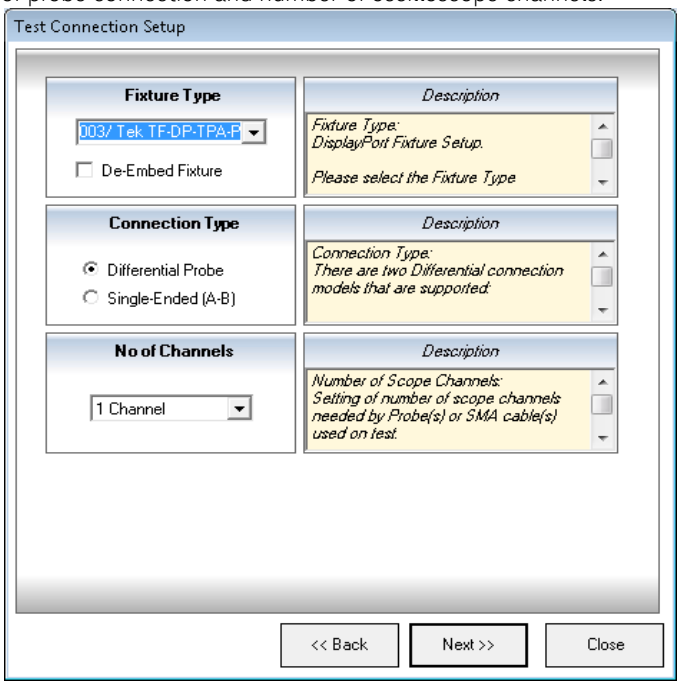
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

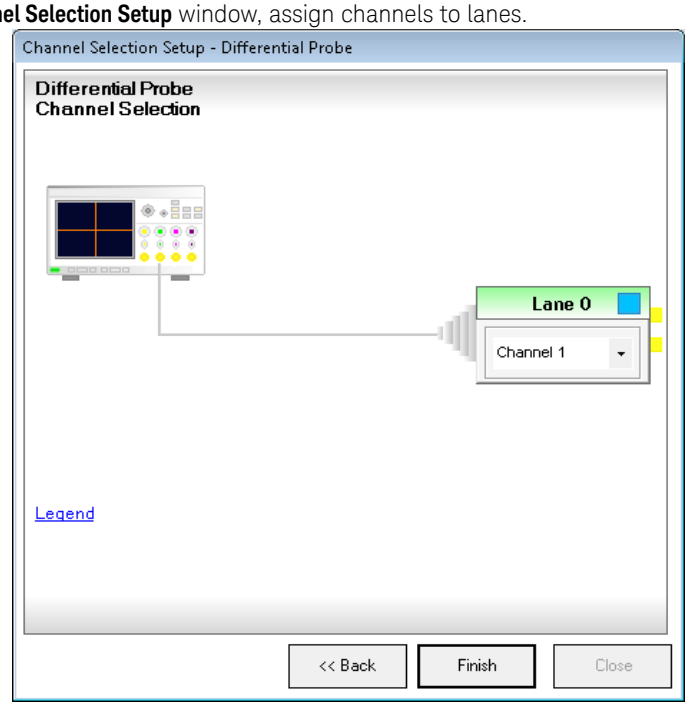
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Pre-Emphasis Level Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

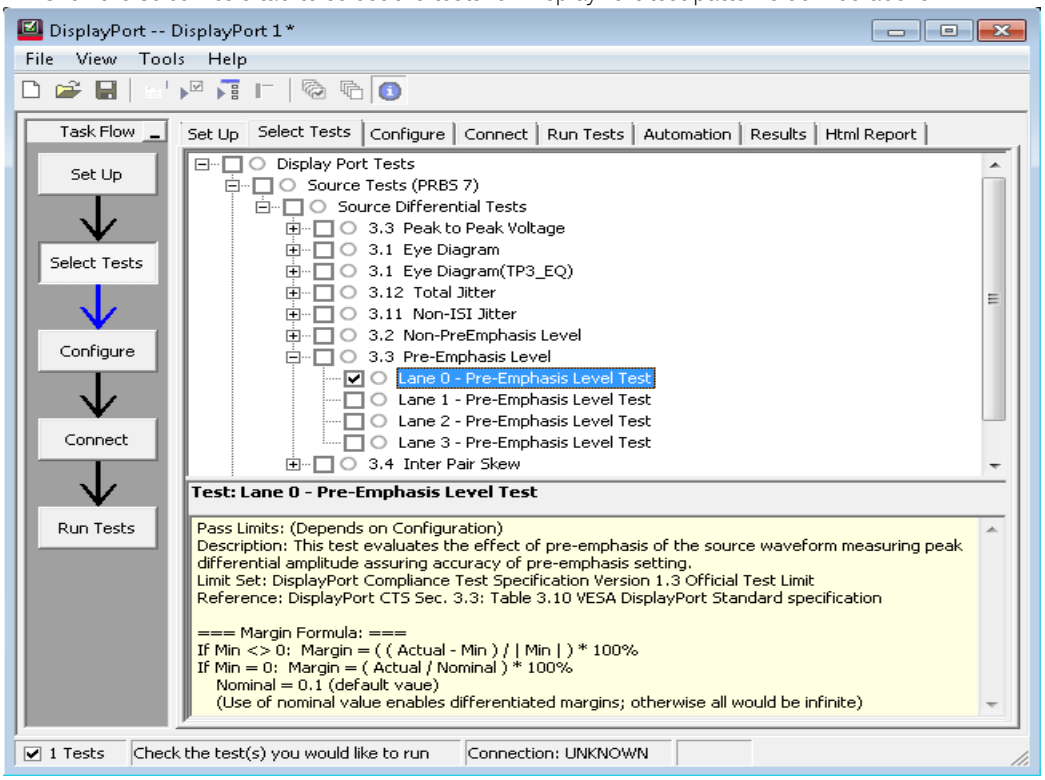


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

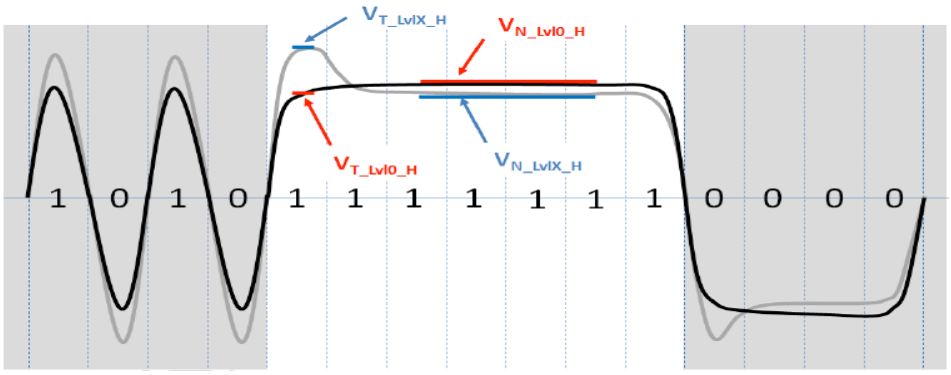


Figure 61 High Voltage measurement for RBR and HBR

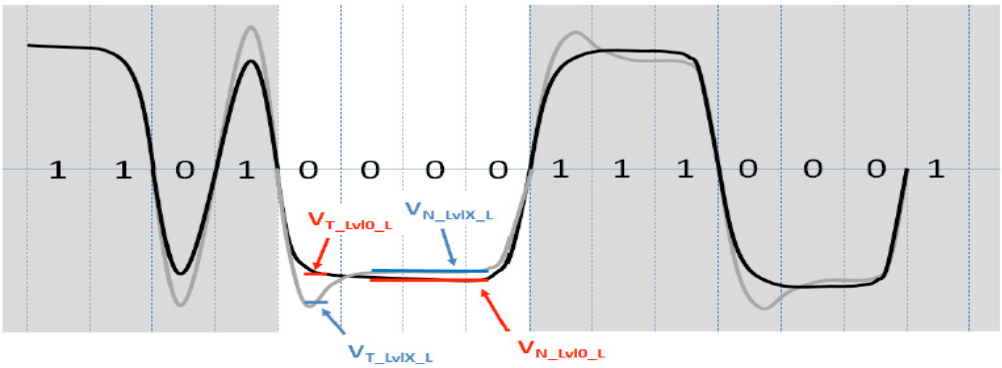


Figure 62 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

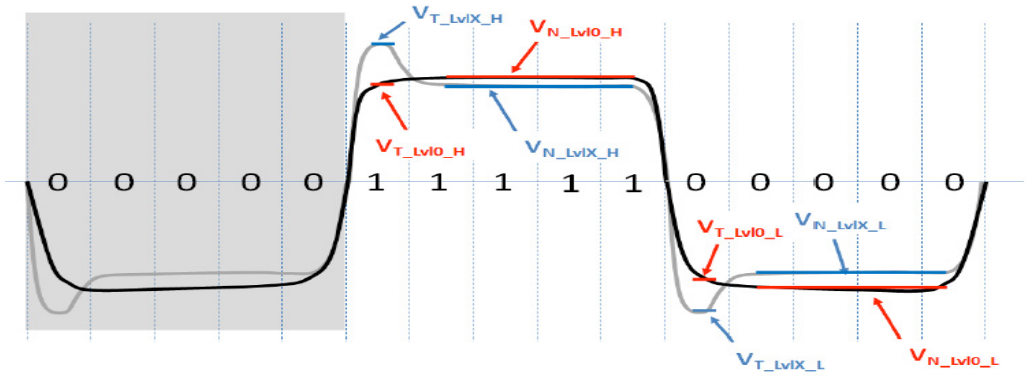


Figure 63 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl1\_PP} / \text{Voltage}_{N\_Lvl1\_PP}] - 20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl2\_PP} / \text{Voltage}_{N\_Lvl2\_PP}] - 20 * \text{Log}[\text{Voltage}_{T\_Lvl1\_PP} / \text{Voltage}_{N\_Lvl1\_PP}]$ for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl3\_PP} / \text{Voltage}_{N\_Lvl3\_PP}] - 20 * \text{Log}[\text{Voltage}_{T\_Lvl2\_PP} / \text{Voltage}_{N\_Lvl2\_PP}]$ for Voltage Swing Level 0, if supported.

Table 56 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-10*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1272001, 1272002, 1272003, 1272004 – Non Transition Voltage Range Measurement (Swing 0)
- 1273001, 1273002, 1273003, 1273004 – Non Transition Voltage Range Measurement (Swing 1)
- 1274001, 1274002, 1274003, 1274004 – Non Transition Voltage Range Measurement (Swing 2)

For Standard DP Pattern (HBR2 and HBR3):

- 1272101, 1272102, 1272103, 1272104 – Non Transition Voltage Range Measurement (Swing 0)
- 1273101, 1273102, 1273103, 1273104 – Non Transition Voltage Range Measurement (Swing 1)
- 1274101, 1274102, 1274103, 1274104 – Non Transition Voltage Range Measurement (Swing 2)

For Arbitrary Pattern:

- 1372101, 1372102, 1372103, 1372104 – Non Transition Voltage Range Measurement (Swing 0)
- 1373101, 1373102, 1373103, 1373104 – Non Transition Voltage Range Measurement (Swing 1)
- 1374101, 1374102, 1374103, 1374104 – Non Transition Voltage Range Measurement (Swing 2)

Test Overview

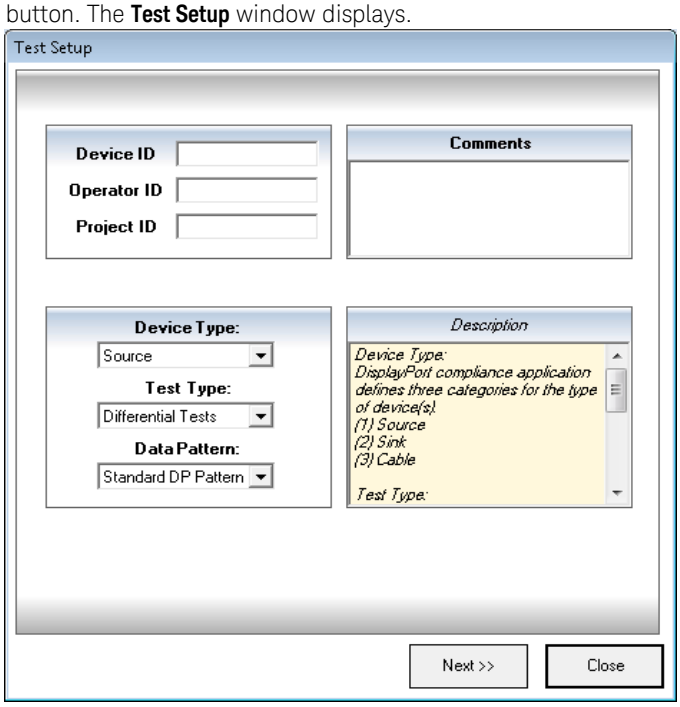
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non-Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.3 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



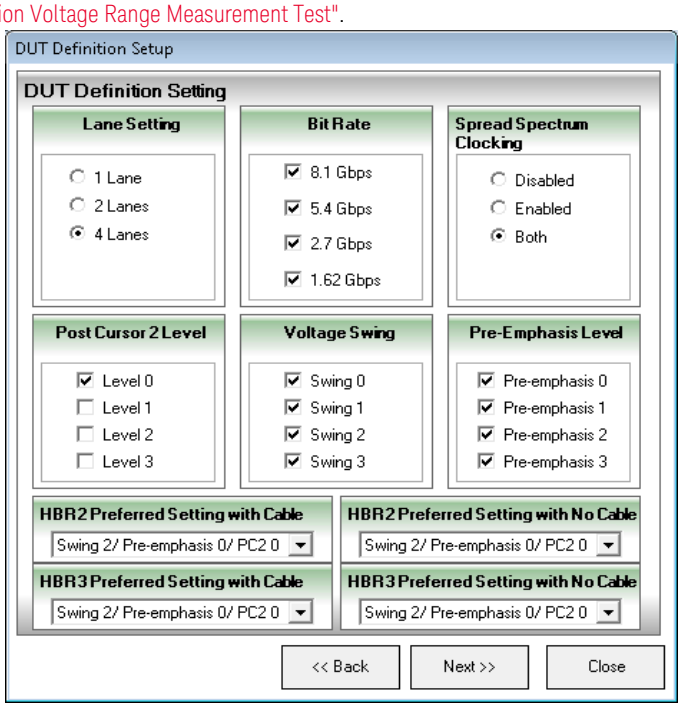
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

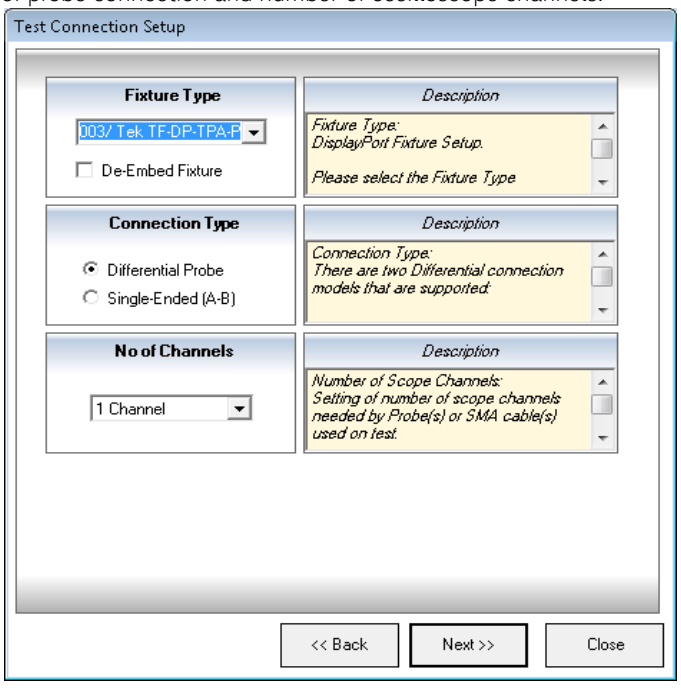
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

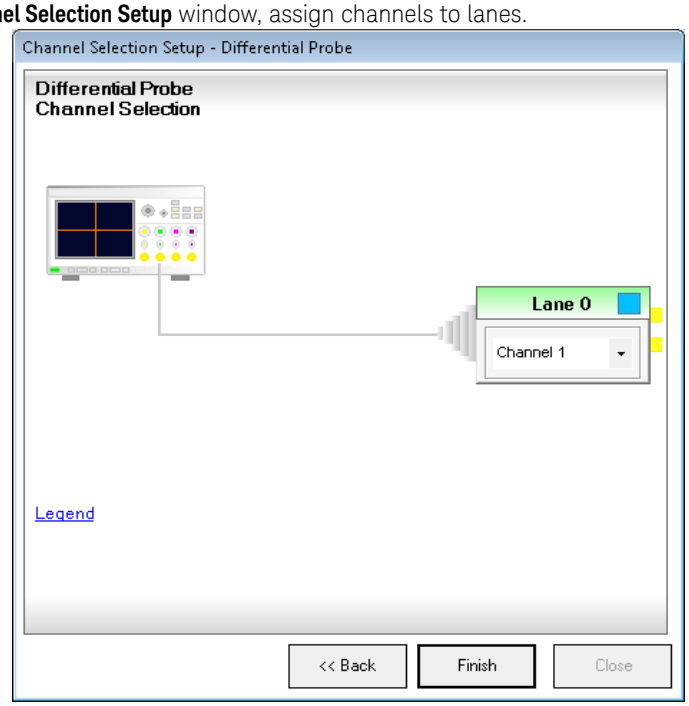
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-Transition Voltage Range Measurement Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

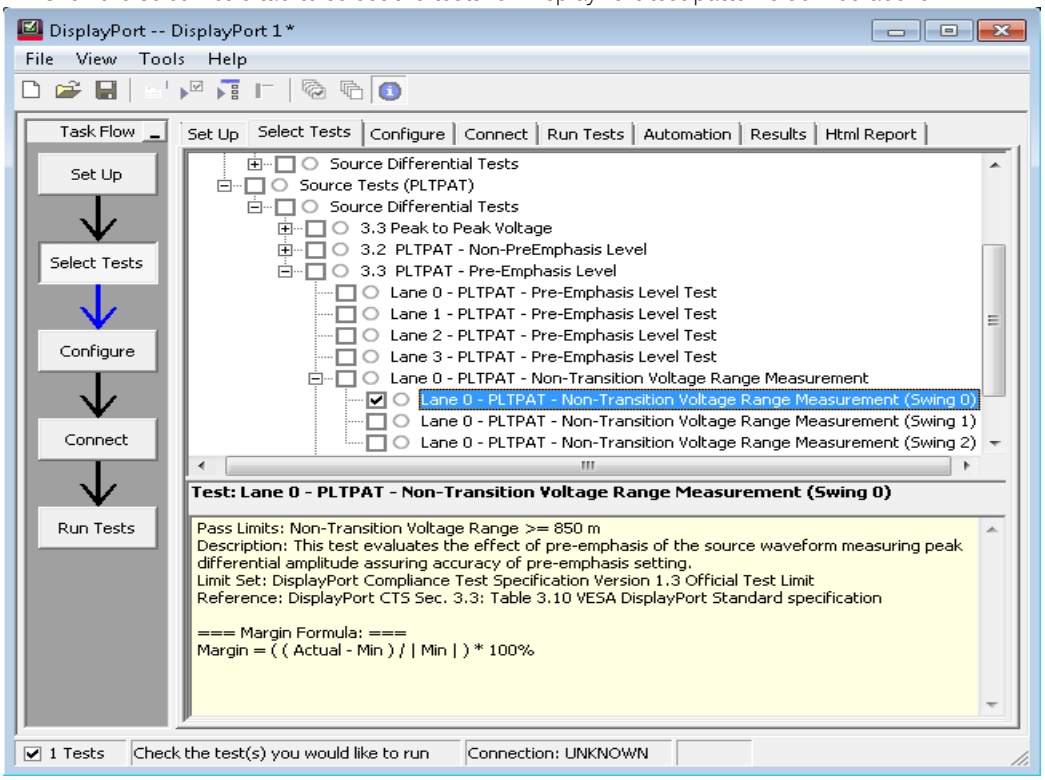


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.3 Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

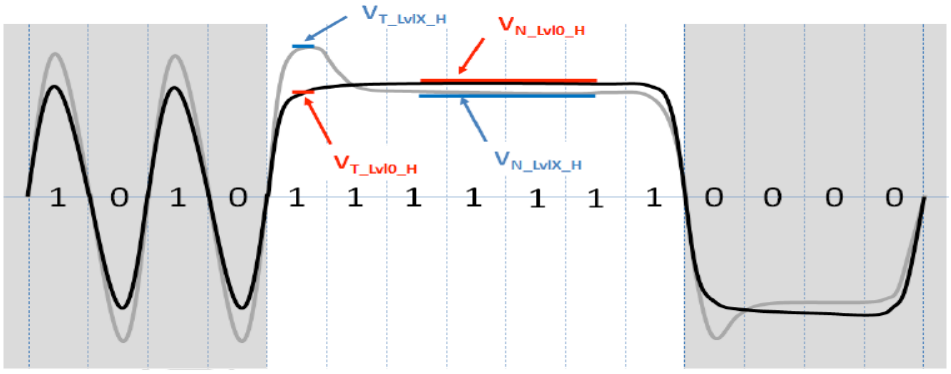


Figure 64 High Voltage measurement for RBR and HBR

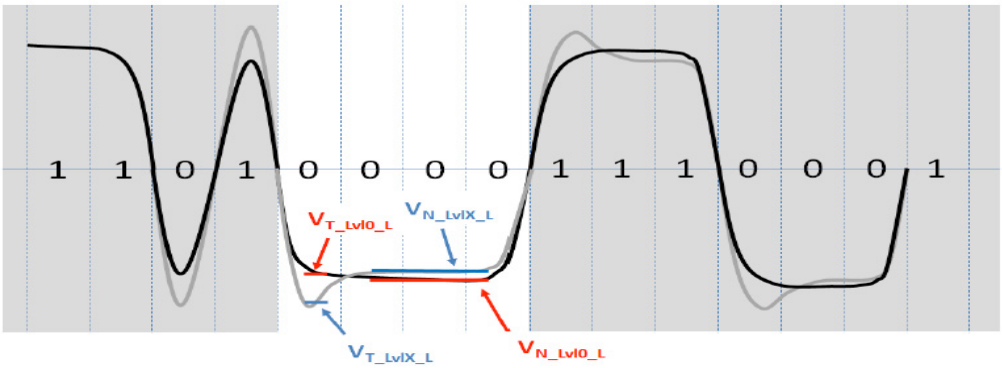


Figure 65 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR3 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5^{th} bit of the five successive transmitted zeros of the pattern.

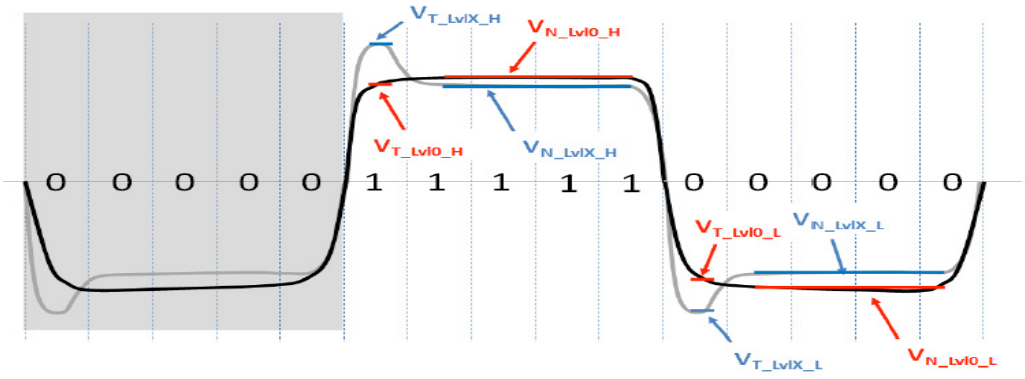


Figure 66 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant > 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant > 0.85 OR 20*log(Resultant) > -1.4dB

Table 57 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX\text{-}DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX\text{-}DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-10*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For Standard DP Pattern (RBR and HBR):

- 1266001, 1266002, 1266003, 1266004 – Peak to Peak Voltage Test

For Standard DP Pattern (HBR2 and HBR3):

- 1266101, 1266102, 1266103, 1266104 – Peak to Peak Voltage Test

For Arbitrary Pattern:

- 1366101, 1366102, 1366103, 1366104 – Peak to Peak Voltage Test

Test Overview

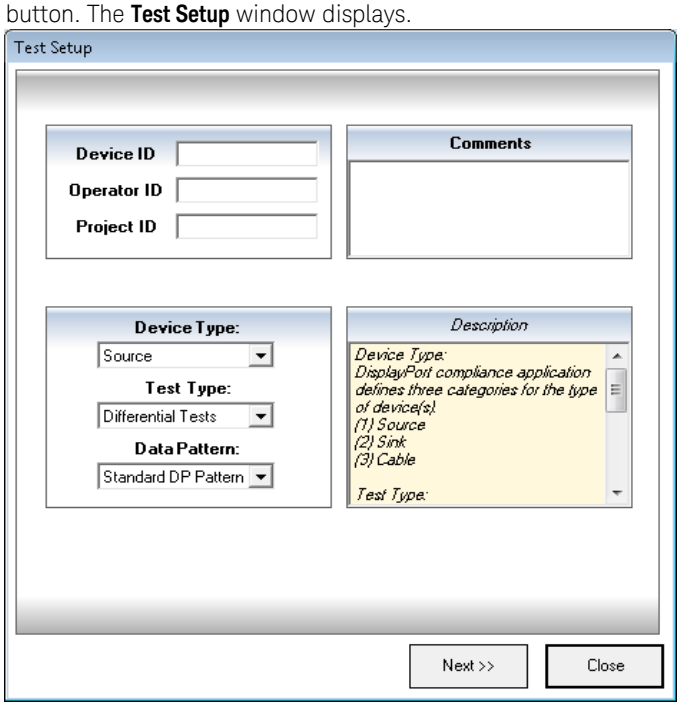
The objective of this test is to evaluate the maximum differential peak to peak voltage.

Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.3 Standard.
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR3 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



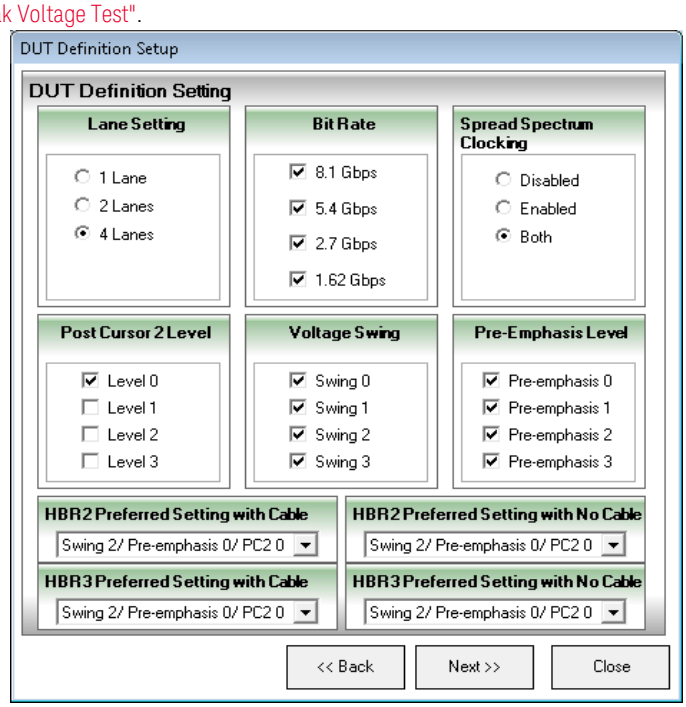
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

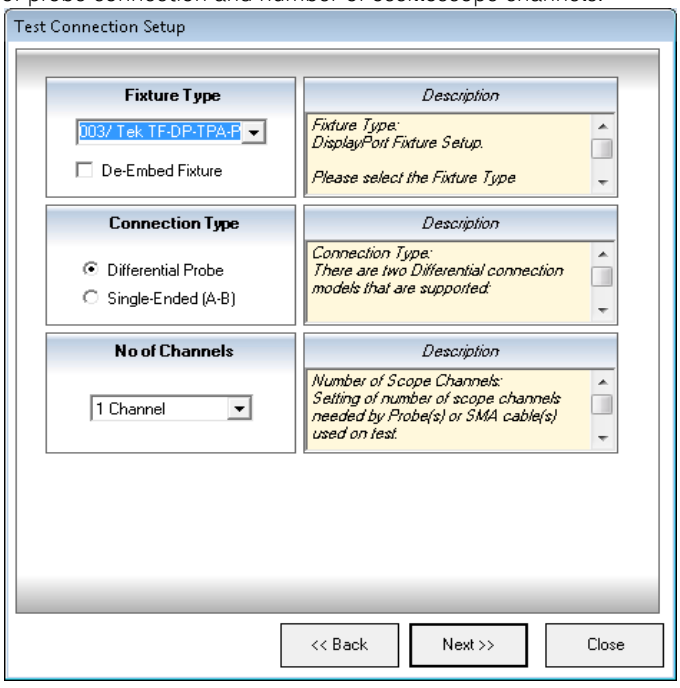
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

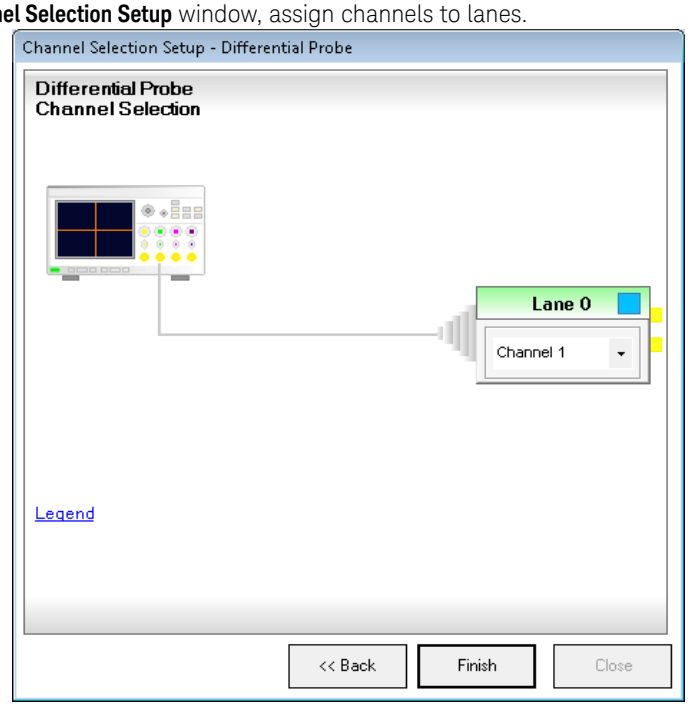
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Peak to Peak Voltage Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

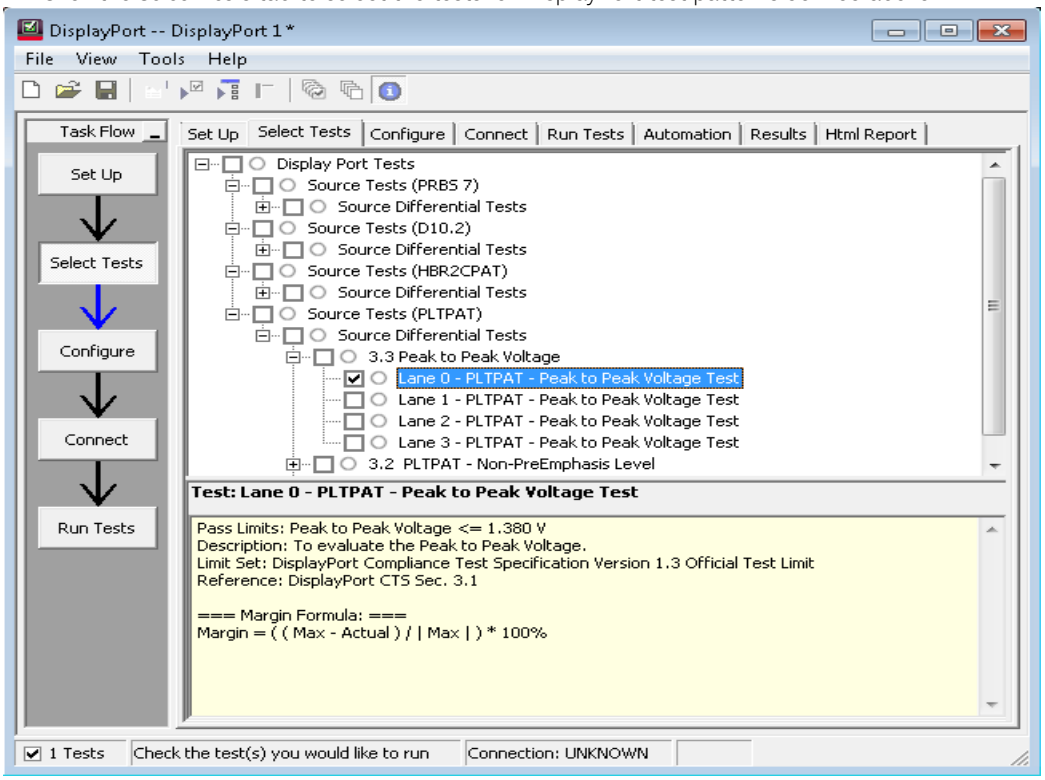


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = \text{Maximum Voltage} - \text{Minimum Voltage}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V.

Table 58 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-10*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Inter-Pair Skew Test

Test ID

For Standard DP Pattern:

- 1290001 – Lane0/Lane1 Inter-Pair Skew Test
- 1290002 – Lane0/Lane2 Inter-Pair Skew Test
- 1290003 – Lane0/Lane3 Inter-Pair Skew Test
- 1290004 – Lane1/Lane2 Inter-Pair Skew Test
- 1290005 – Lane1/Lane3 Inter-Pair Skew Test
- 1290006 – Lane2/Lane3 Inter-Pair Skew Test

For Arbitrary Pattern:

- Not applicable for arbitrary pattern

Test Overview

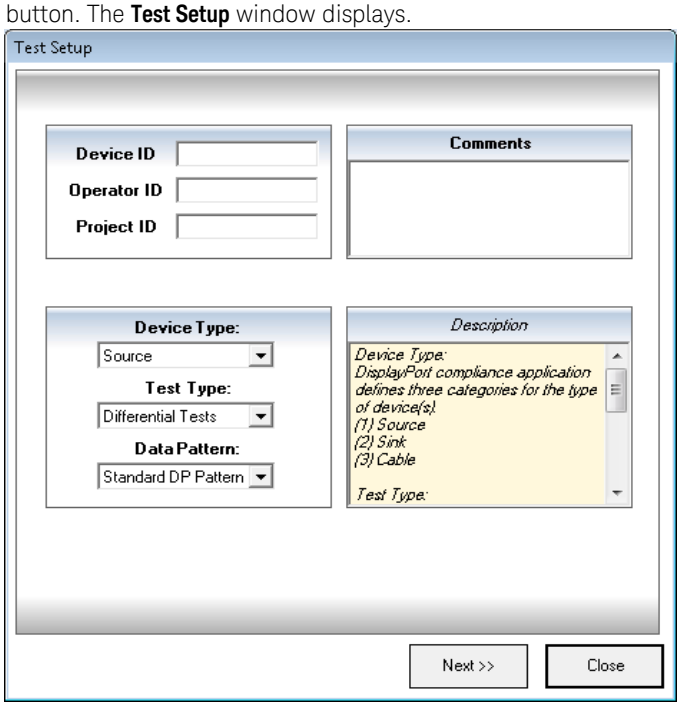
The objective of the test is to evaluate the skew or time delay between differential data lanes in the DisplayPort interface.

Test Conditions for Inter Pair Skew Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest Bit Rate supported (RBR, HBR, HBR2 or HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported For two lane operation: Lane 0 to Lane 1 For four lane operation: Lane 0 to Lane 1 Lane 0 to Lane 2 Lane 0 to Lane 3 Lane 1 to Lane 2 Lane 1 to Lane 3 Lane 2 to Lane 3
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



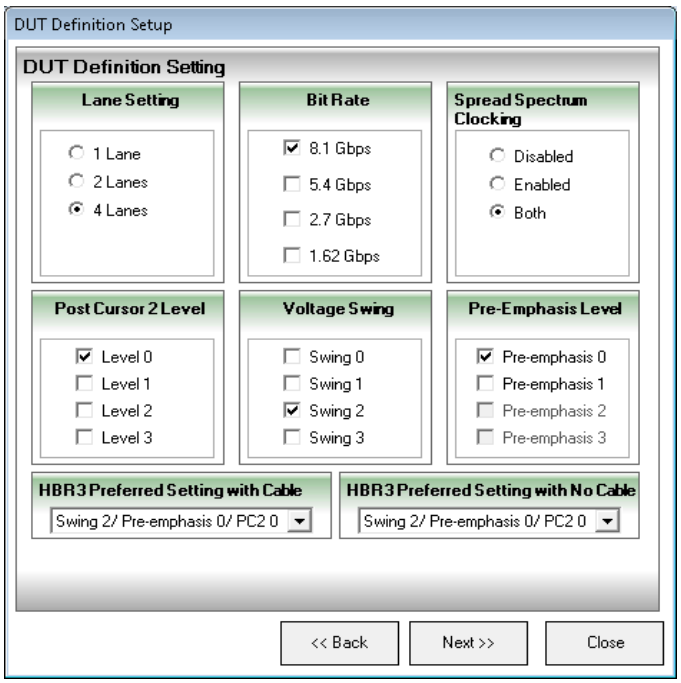
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

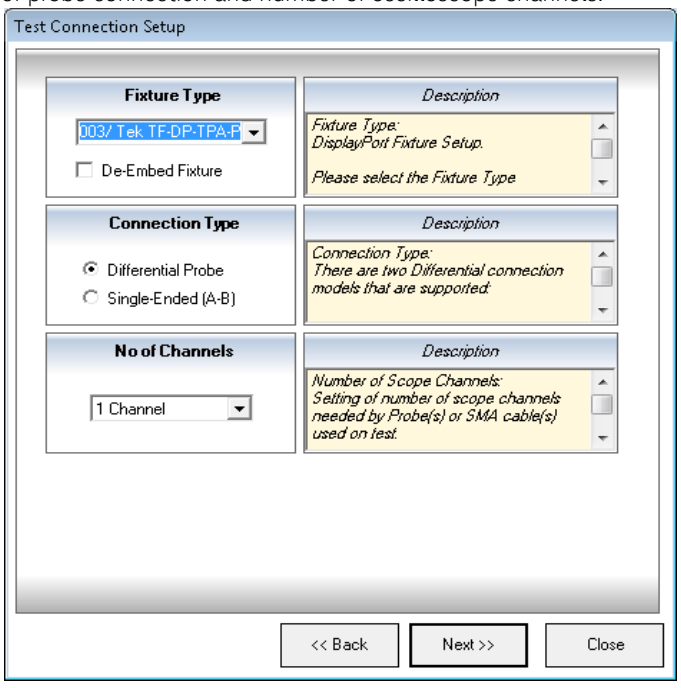
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

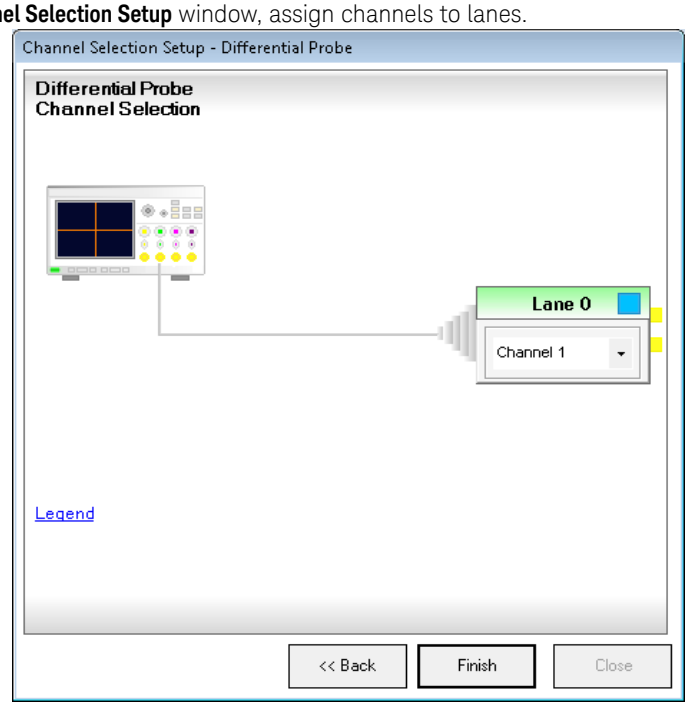
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Inter Pair Skew Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

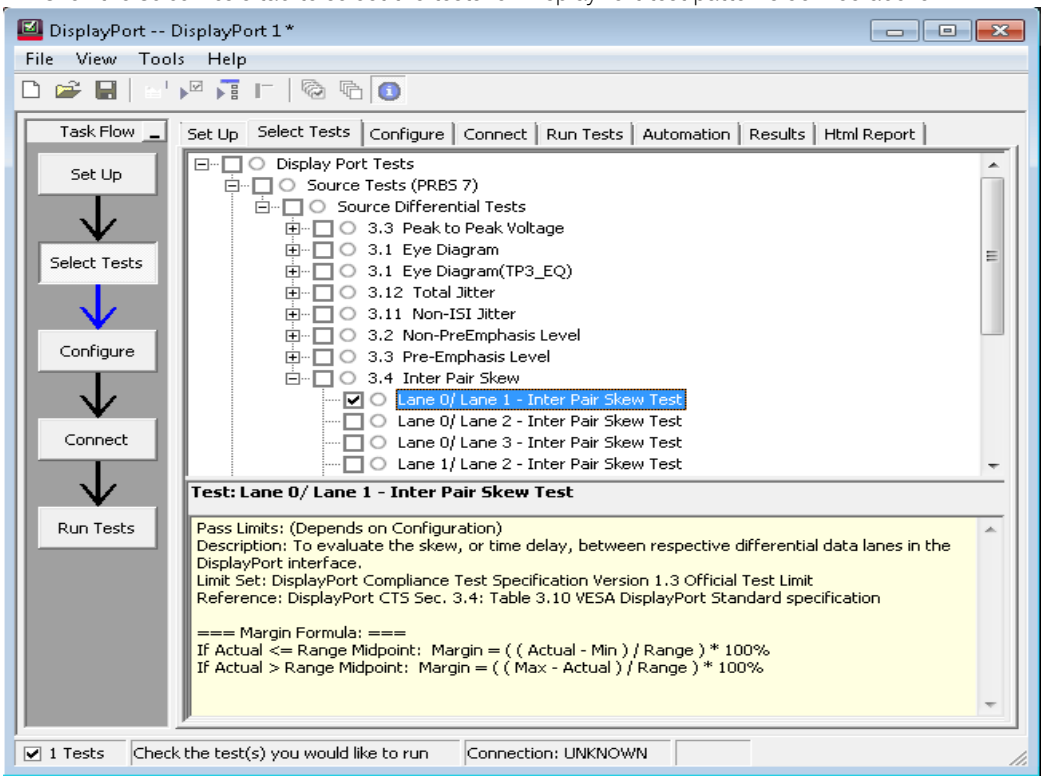


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given inter-pair skew measurement of Lane A to Lane B:
   a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   b Acquire and verify the input signal:
      i Verify the trigger and the amplitude of the Lane A input signal.
      ii Scale the vertical display of the Lane A input signal to optimum value.
      iii Measure V_{TOP} and V_{BASE} of the Lane A input signal.
      iv Verify the trigger and the amplitude of the Lane B input signal.
      v Scale the vertical display of the Lane B input signal to optimum value.
      vi Measure V_{TOP} and V_{BASE} of the Lane B input signal.
      vii Measure the data rate of the Lane A input signal.
      viii Measure the data rate of the Lane B input signal.
   c Set up the parameter of the measurement:
      i Enable measurement of all edges to obtain a statistical value of the measurement.
      ii Set up the measurement threshold.
   d Set up the parameter for the inter-pair skew measurement:
      i Set up two display grids such that each grid displays one test lane data signal.
      ii Set up the measurement threshold for each test lane data signal on the Transition Voltage = 0V.
      iii Decode the data signal for each test lane.
      iv Search the desired pattern from the decoded data signal.
      v Measure the time difference between the corresponding edges of both test lanes:

$$T_{Transition\_LaneA} - T_{Transition\_LaneB}$$

      vi Repeat the previous step until you measure 100 edges.
      vii VESA DisplayPort 1.3 Standard specifies 20 UI offset Lane 0 to Lane 1, Lane 1 to Lane 2 and Lane 2 to Lane 3. The resultant offset is cumulative.
      viii Calculate the inter-pair skew using the equation:

$$\text{Inter-Pair Skew} = \{1/\text{Number of Edges}\} \sum |T_{Transition\_LaneA} - T_{Transition\_LaneB}| - \text{Nominal Skew}$$

   where, Nominal Skew is the expected offset between tested lanes.
2 Report the measurement results.

PASS Condition

-1250ps < Inter-Lane Skew Tolerance < 1250ps

Table 59 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$t_{TX-SKEW-INTER\_PAIR}$	Lane-to-Lane Output Skew	-	-	1250	ps	Applies to transmitters capable of 2- and 4-lane operation. Also, applies to all pairwise combinations of supported lanes for all data rates.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.4*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-10*

Expected/Observable Results

The measured inter-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

For Standard DP Pattern:

- 12193001 12193002 12193003 12193004 – Main Link Frequency Compliance

For Arbitrary Pattern:

- 13193001 13193002 13193003 13193004 – Main Link Frequency Compliance

Test Overview

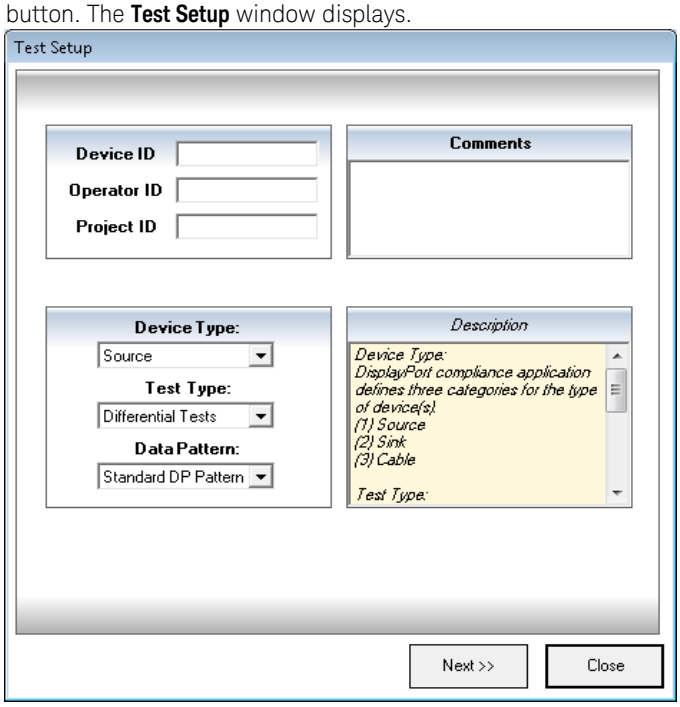
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.3 Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



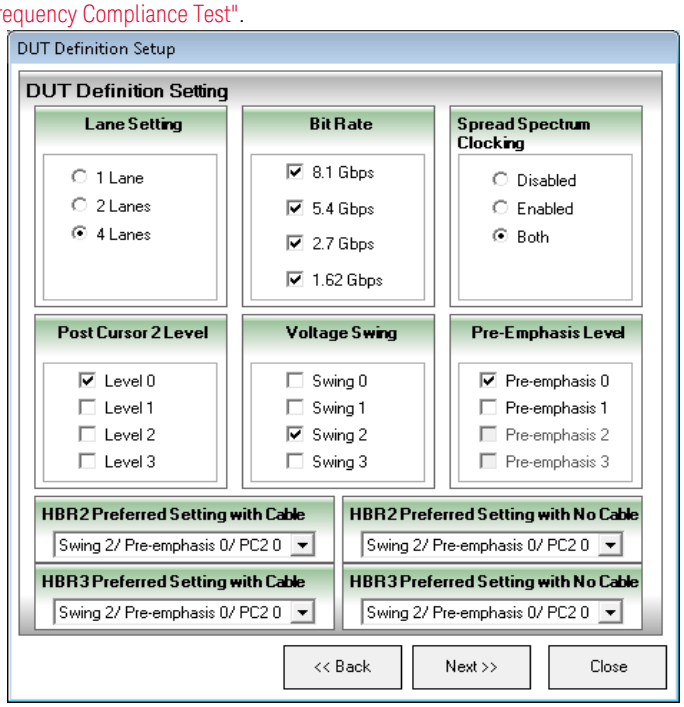
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

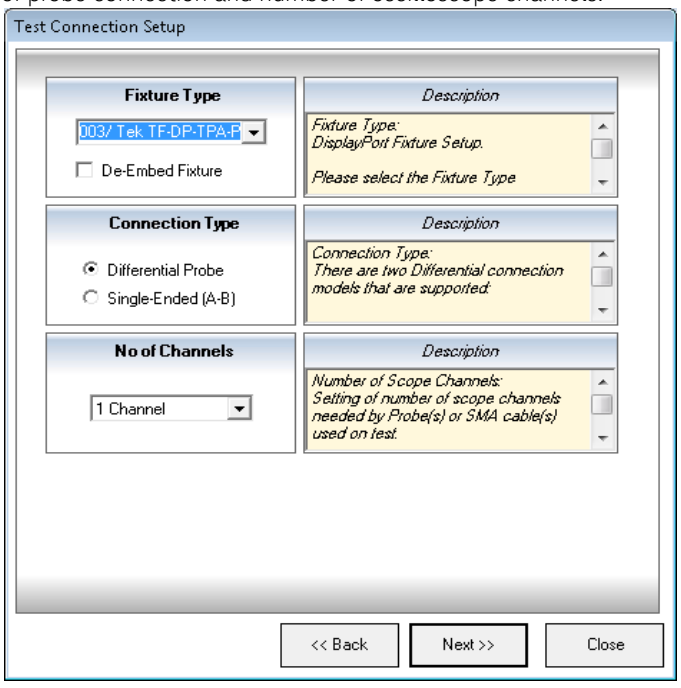
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

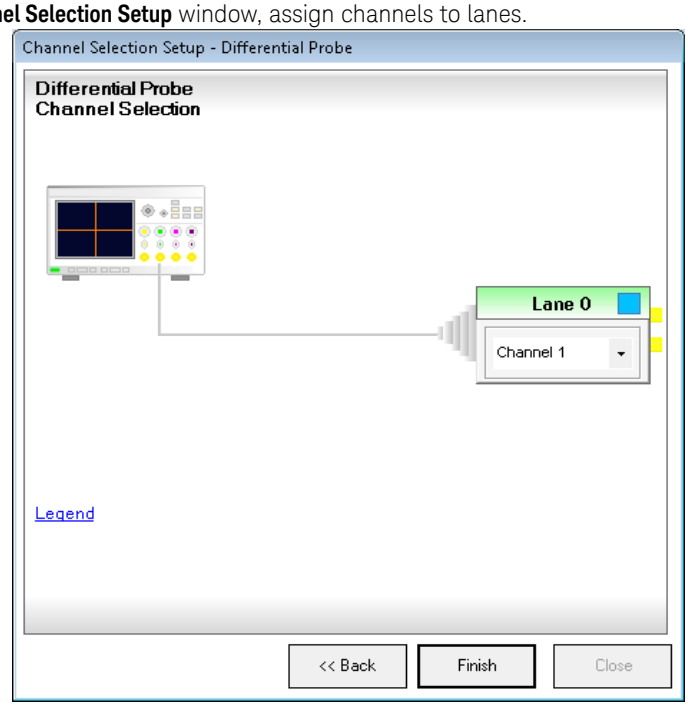
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Main Link Frequency Compliance Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

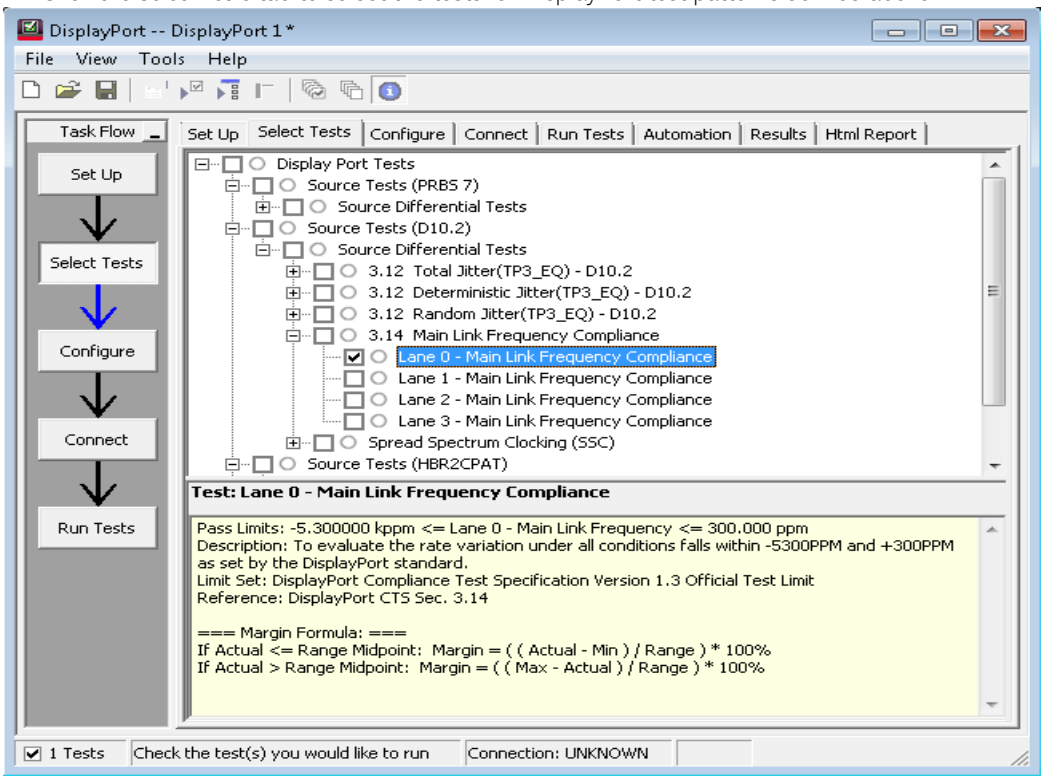


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.
5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.

9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:

a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.

b Acquire the signal with one complete SSC cycle.

c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

Maximum Data Rate = 1 / (Minimum Unit Interval)

d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

Minimum Data Rate = 1 / (Maximum Unit Interval)

e Repeat steps b, c and d until you acquire 10 SSC Cycles.

f Calculate the mean value for the maximum and minimum data rates.

10 Report the measurement results.

PASS Condition

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

Table 60 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR3}	Frequency for High Bit Rate 3	8.05707	8.1	8.10243	Gbps	
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-9*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

For Standard DP Pattern:

- 12170001 12170002 12170003 12170004 – SSC Modulation Frequency Test

For Arbitrary Pattern:

- 13170001 13170002 13170003 13170004 – SSC Modulation Frequency Test

Test Overview

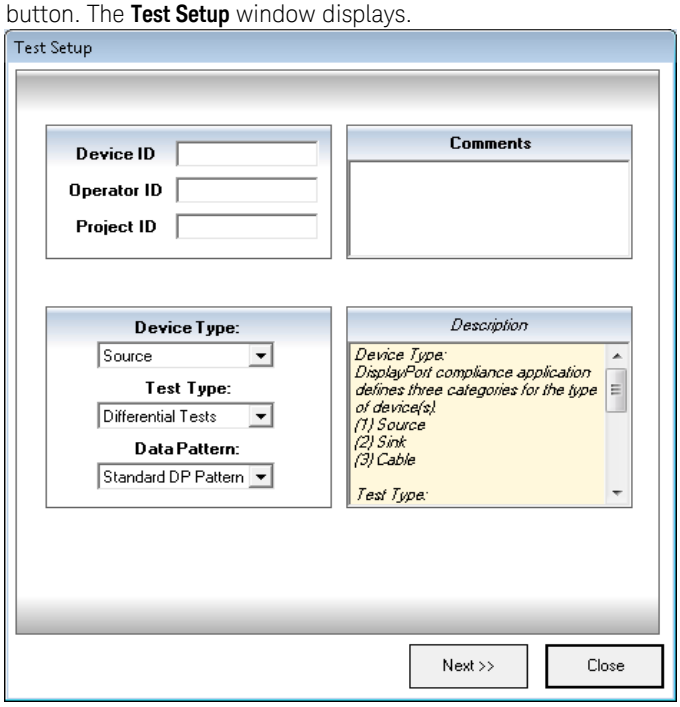
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



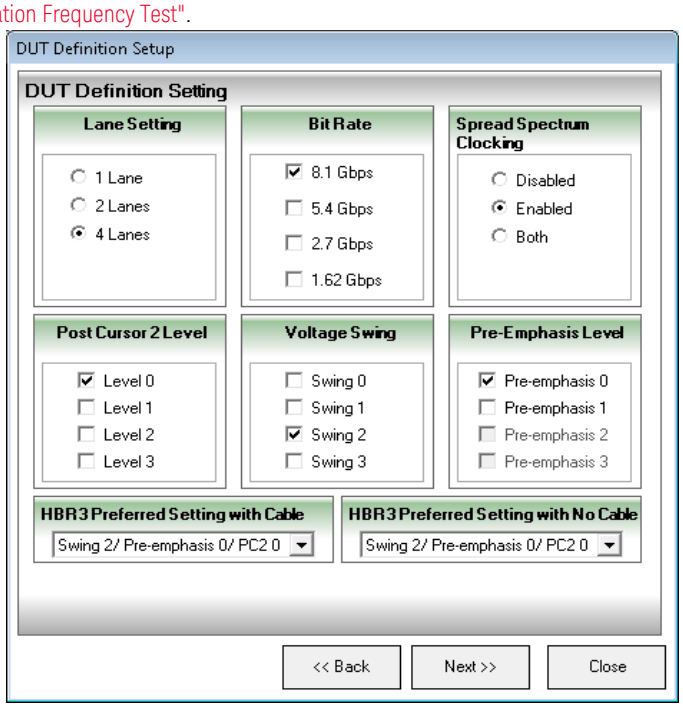
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

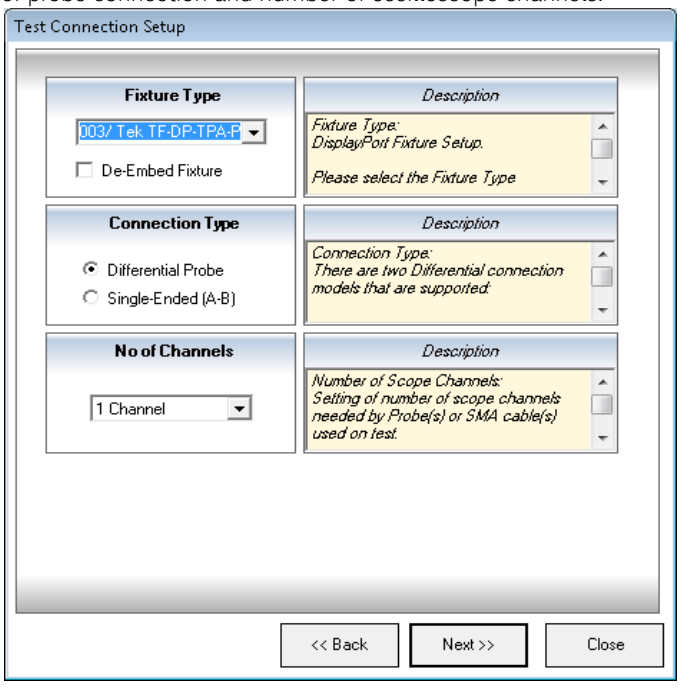
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

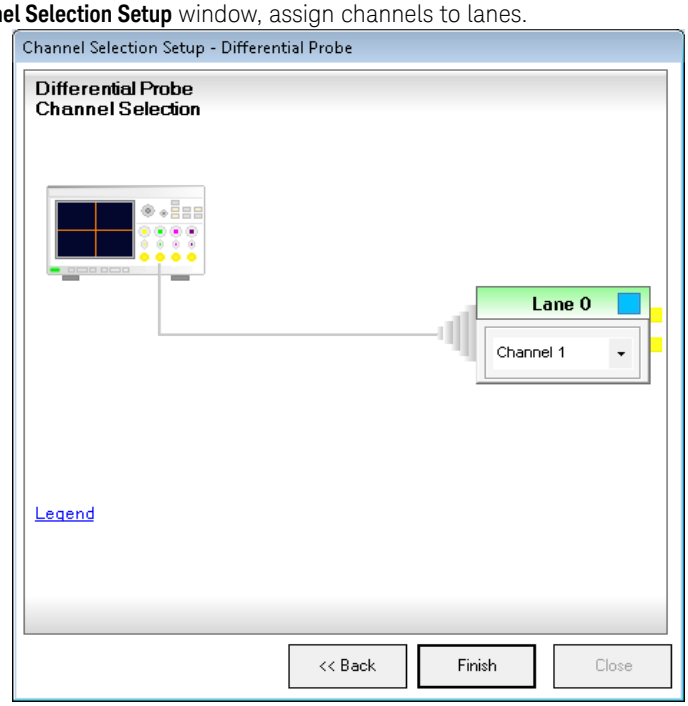
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Modulation Frequency Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

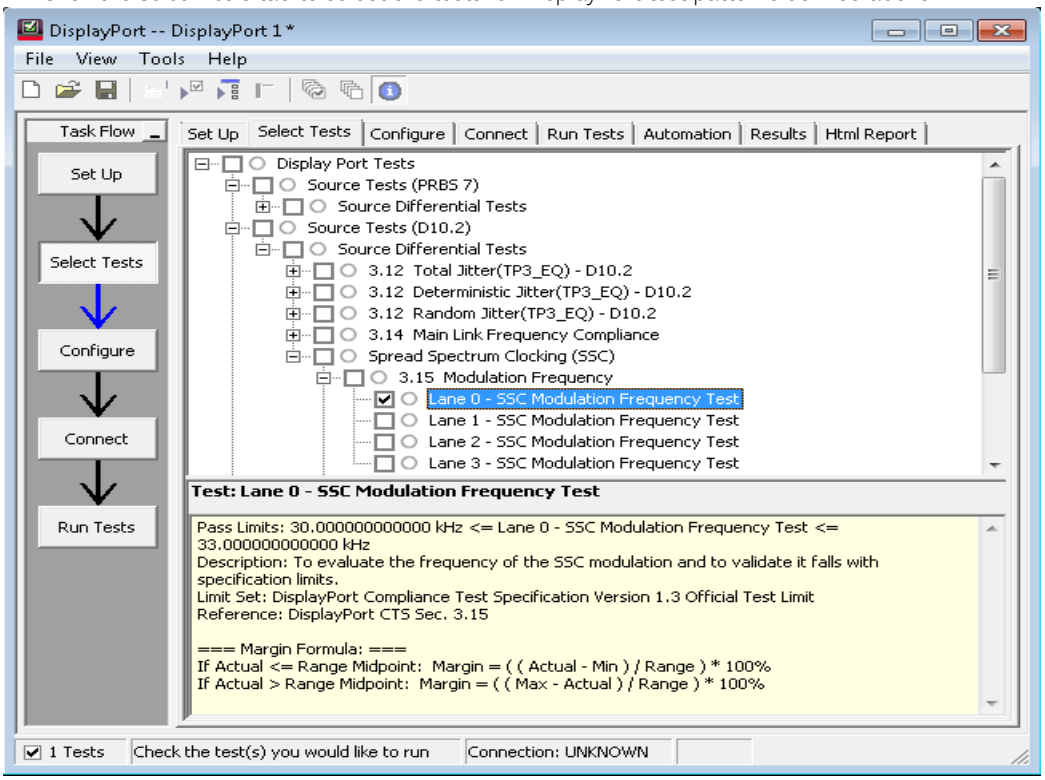


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
   g Acquire the signal for 10 SSC Cycles.
6 Get the mean value for the SSC Modulation frequency.
7 Report the measurement results.

PASS Condition

30kHz ≤ SSC Modulation Frequency (f_{SSC}) ≤ 33kHz

Table 61 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-9*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

For Standard DP Pattern:

- 12180001 12180002 12180003 12180004 – SSC Modulation Deviation Test

For Arbitrary Pattern:

- 13180001 13180002 13180003 13180004 – SSC Modulation Deviation Test

Test Overview

The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

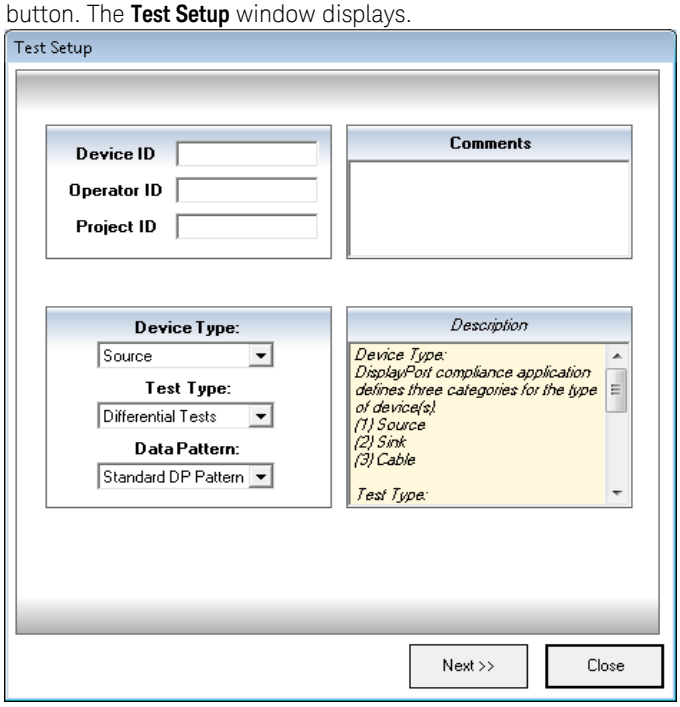
SSC Modulation Deviation = {[Average (Maximum Data Rate) - Average (Minimum Data Rate)] / Nominal Data Rate}*1e6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



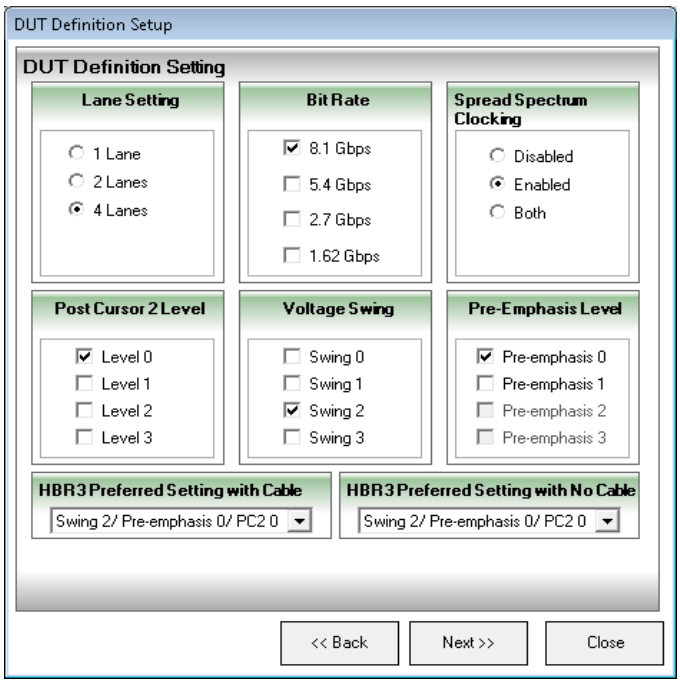
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

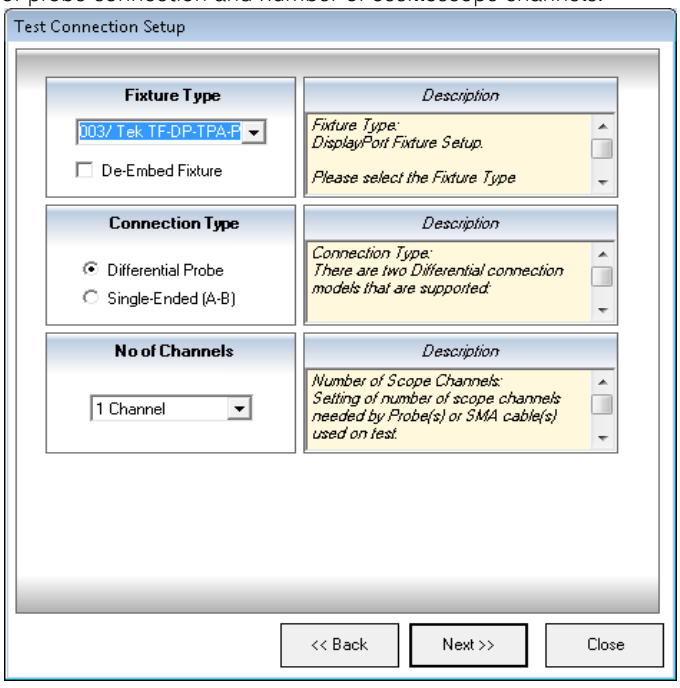
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

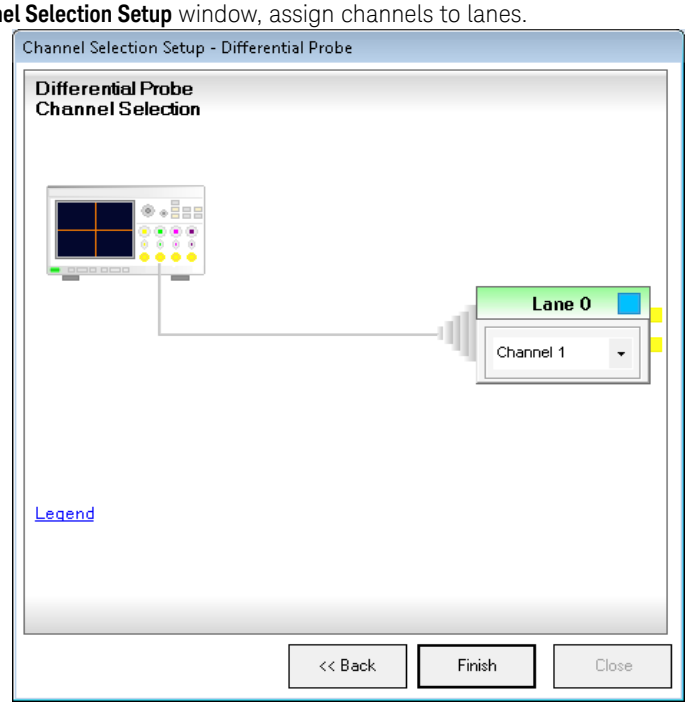
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Modulation Deviation Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

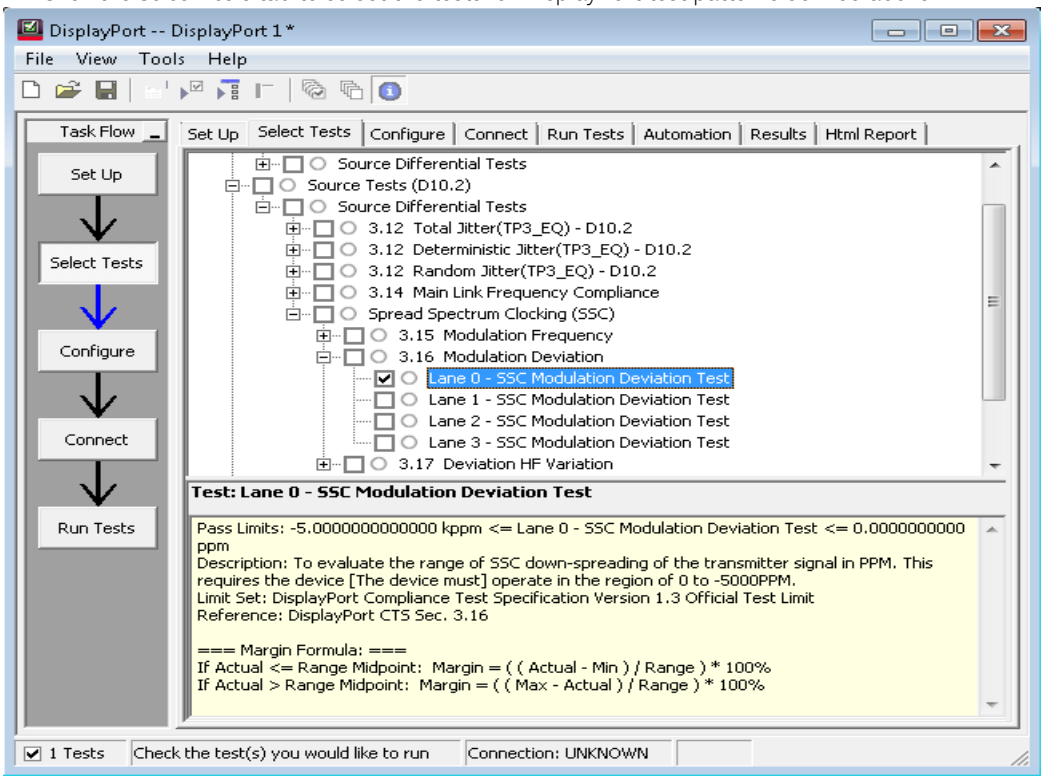


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.
5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.

9 Set up the parameters for SSC measurement.

a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.

b Acquire the signal with one complete SSC Cycle.

c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

Maximum Data Rate = 1/Minimum Unit Interval

d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

Minimum Data Rate = 1/Maximum Unit Interval

e Repeat step b,c and d until you acquire 10 SSC Cycles.

f Calculate the mean value for the maximum and minimum data rate.

10 Calculate the SSC Modulation Deviation using the equation:

SSC Modulation Deviation = (Maximum Data Rate - Minimum Data Rate) / (Nominal Data Rate) * 1E6

11 Report the measurement results.

PASS Condition

-5000ppm ≤ SSC Modulation Deviation ($Resultant_{SSC\ Range}$) ≤ 0ppm

Table 62 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.16*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-9*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

For Standard DP Pattern:

- 12200001 12200002 12200003 12200004 – SSC Deviation HF Variation Test (Informative)

For Arbitrary Pattern:

- 13200001 13200002 13200003 13200004 – SSC Deviation HF Variation Test (Informative)

Test Overview

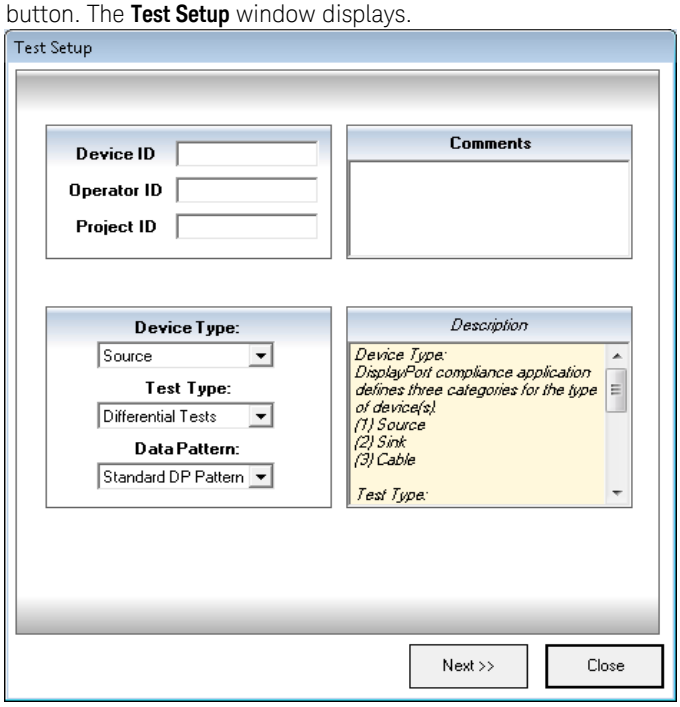
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



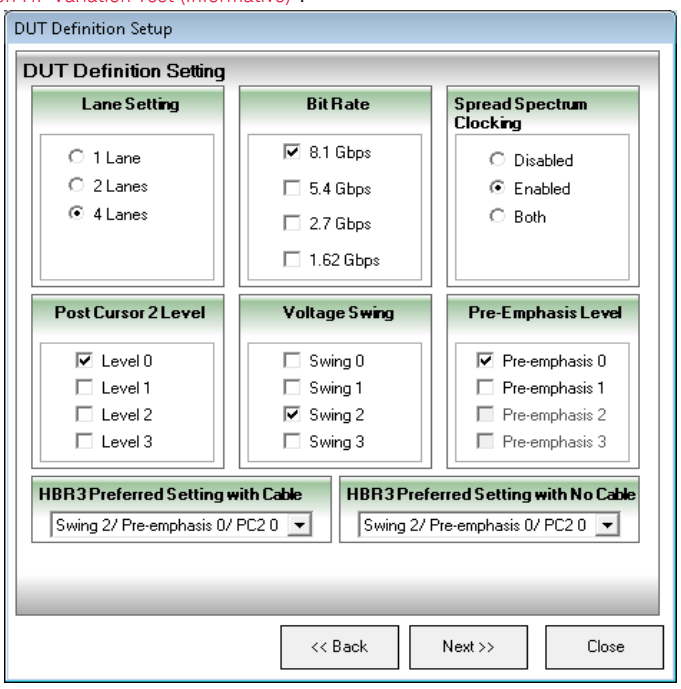
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

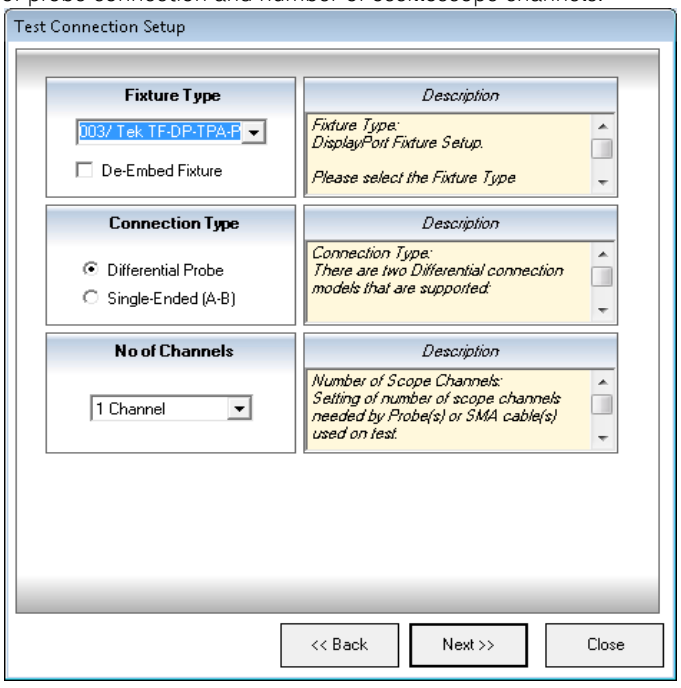
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

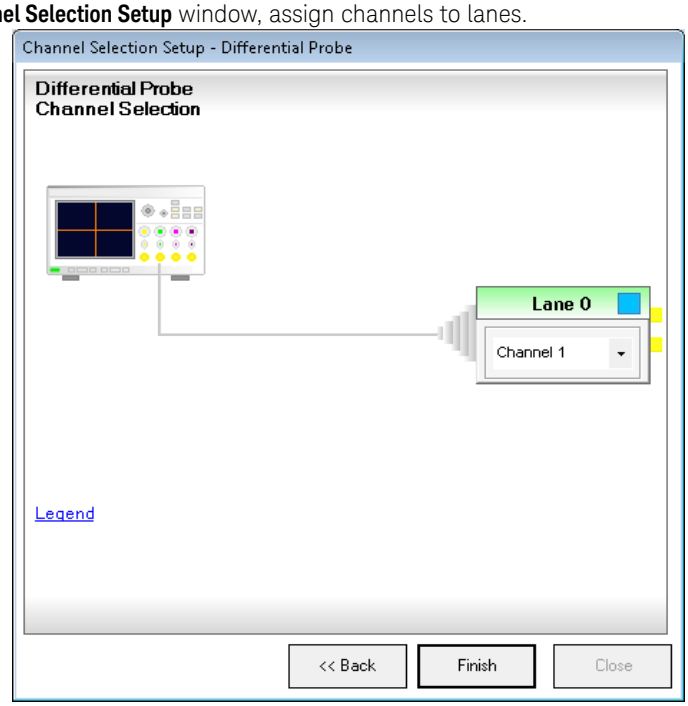
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Deviation HF Variation Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

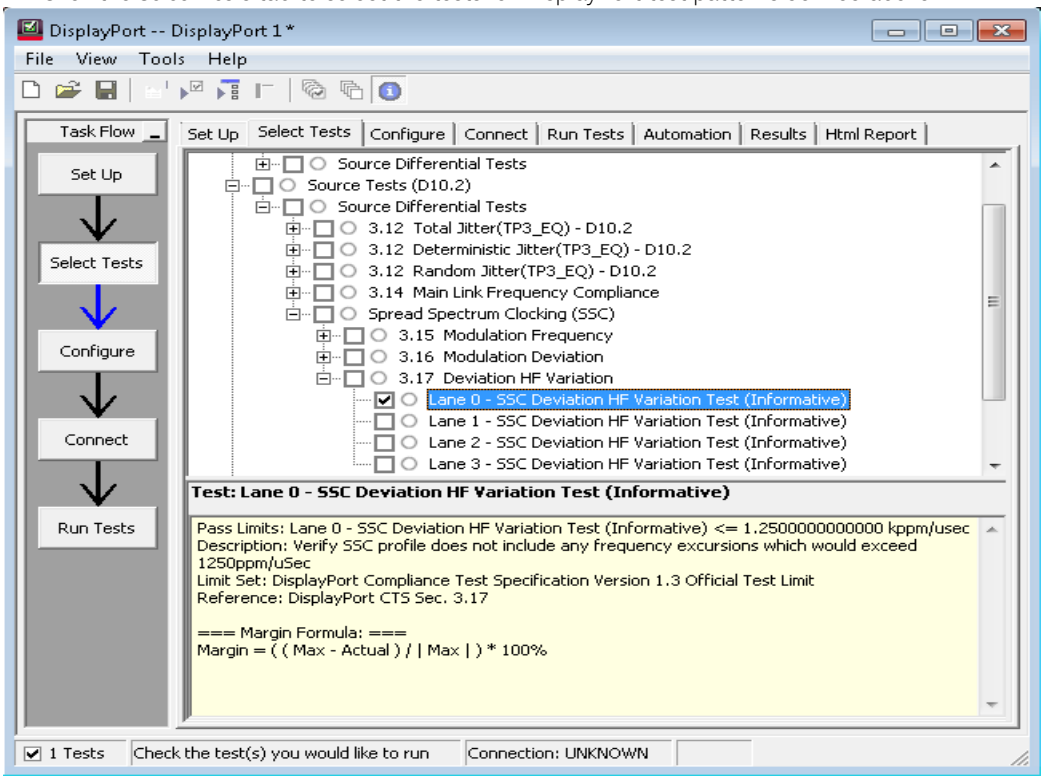


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
6 Set up the parameters for the SSC measurement.
   a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.
   b Acquire the signal with one complete SSC Cycles.
   c Read the FUNC2 filtered unit interval measurement trend.
   d Compute the slope using the “Sliding Window” with 1.00 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t\text{-}1.00\ \mu\text{sec})/1.00\ \mu\text{sec}$$

   e Repeat step b, c and d until you acquire 10 SSC Cycles.
   f Get the maximum value for the computed value of slope.
7 Report the measurement results.

PASS Condition

SSC_t dF/dt ≤ 1250ppm/µsec

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.17*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Eye Diagram Test (TP3_EQ)

Test ID

For Standard DP Pattern (HBR):

- 1211001, 1211002, 1211003, 1211004 – Eye Diagram Test (TP3_EQ) - PRBS7
- 1211011, 1211012, 1211013, 1211014 – Eye Diagram Test with No Cable Model (TP3_EQ) - PRBS7

For Standard DP Pattern (HBR2 and HBR3):

- 1215001, 1215002, 1215003, 1215004 – Eye Diagram Test (TP3_EQ) - HBR2CPAT
- 1215011, 1215012, 1215013, 1215014 – Eye Diagram Test with No Cable Model (TP3_EQ) - HBR2CPAT

For Arbitrary Pattern:

- 1315001, 1315002, 1315003, 1315004 – Eye Diagram Test (TP3_EQ)
- 1315011, 1315012, 1315013, 1315014 – Eye Diagram Test with No Cable Model (TP3_EQ)

Test Overview

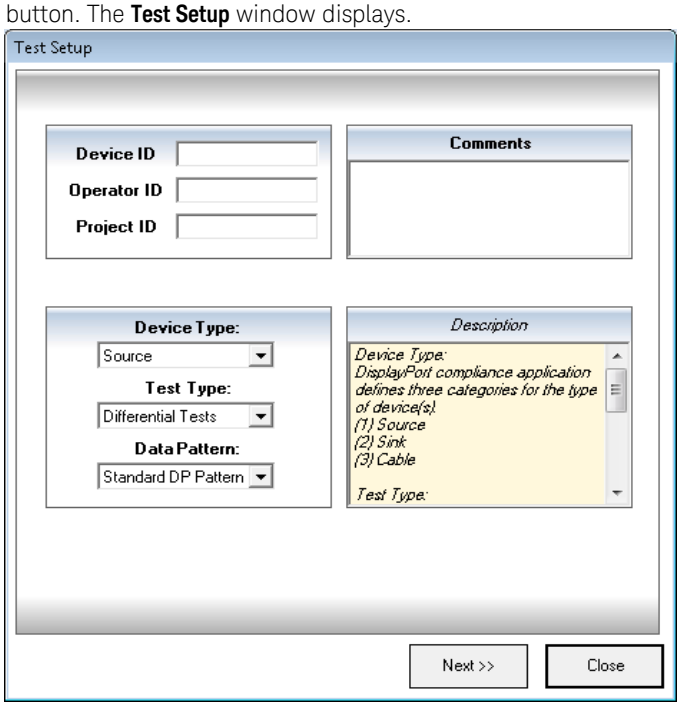
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative), HBR2 and HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	HBR – Level 2 HBR2, HBR3 – Any Voltage Level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2, HBR3 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2, HBR3 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR – PRBS7 HBR2, HBR3 – HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



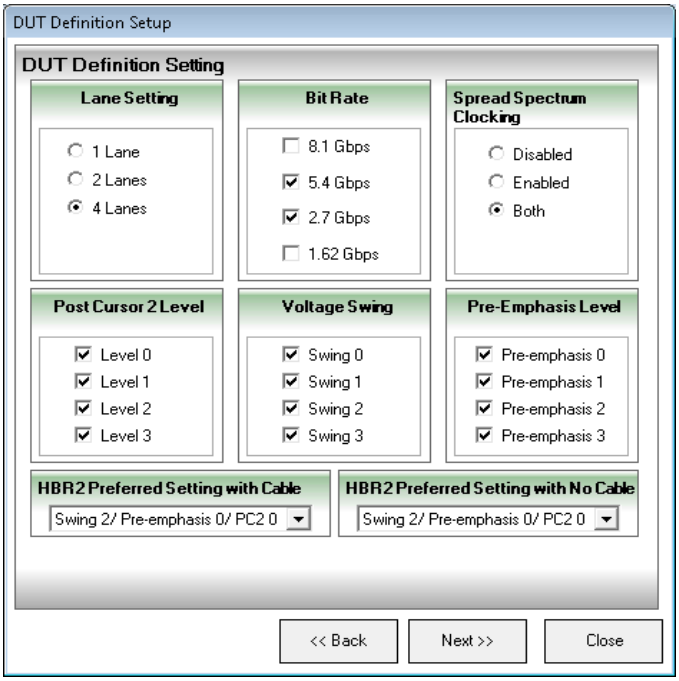
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

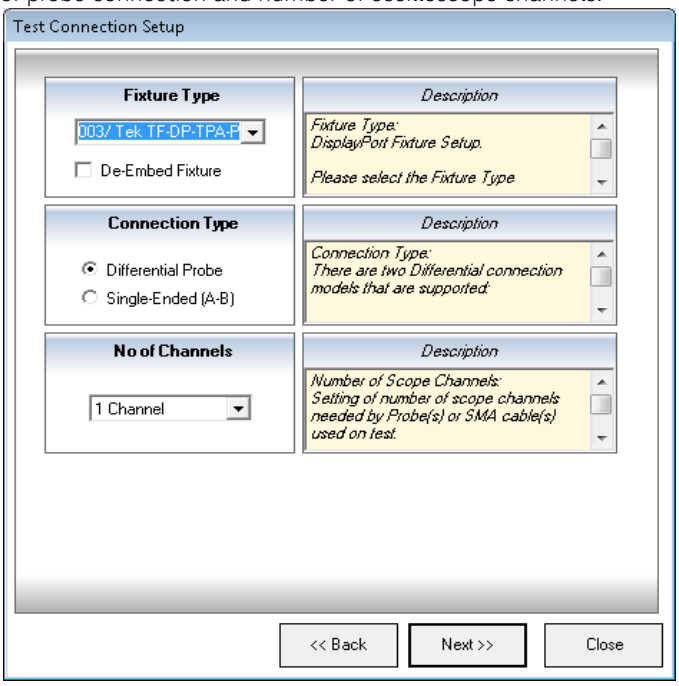
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

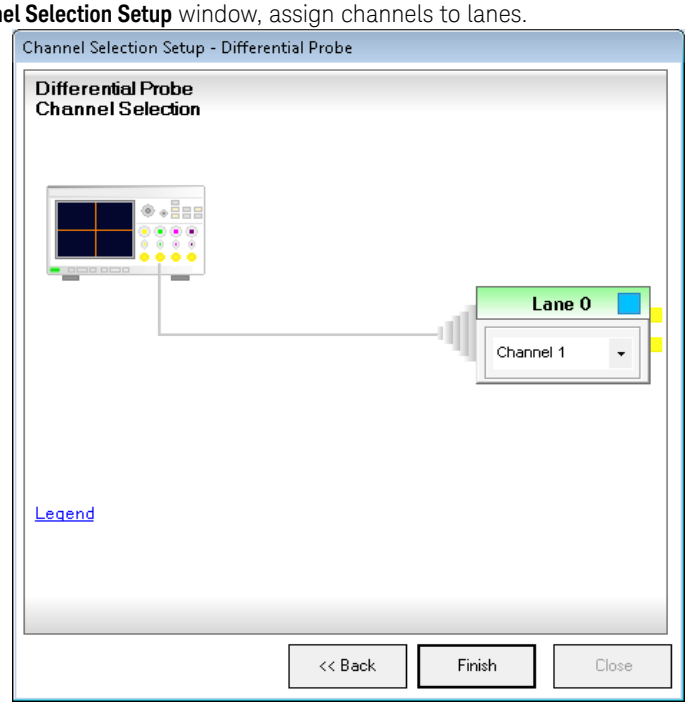
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

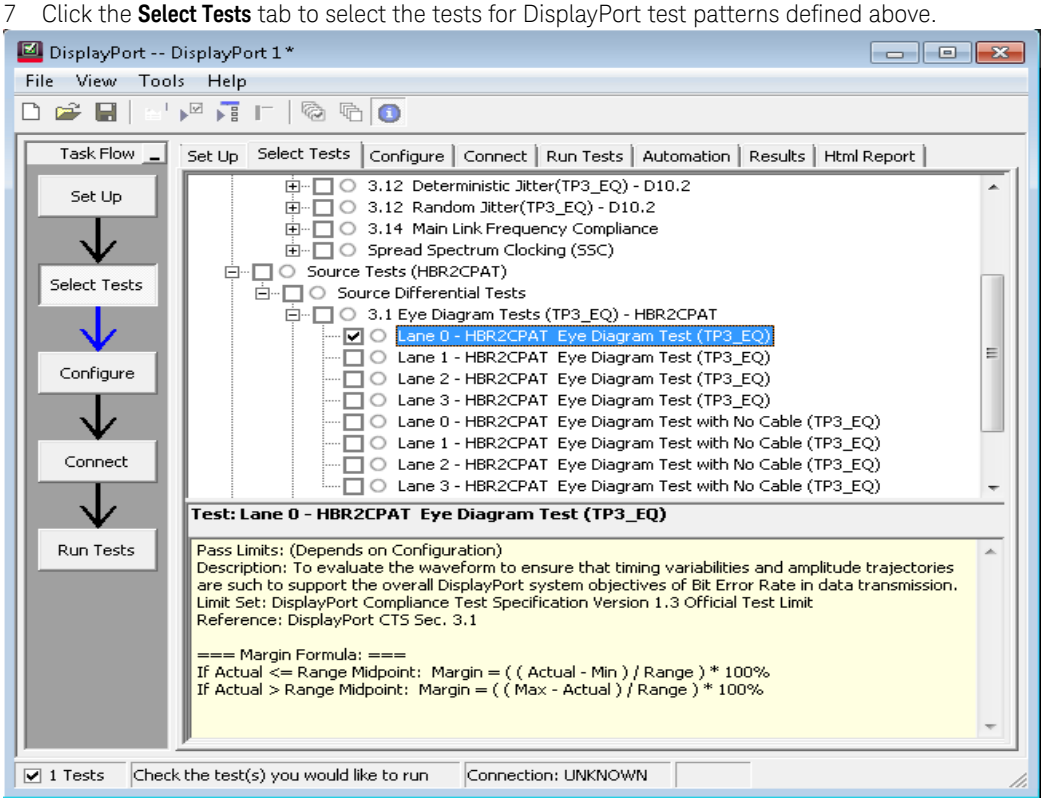


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure for HBR

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2 and HBR3

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.

4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 1,000,000 edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If you select more than one lane (2 lanes or 4 lanes DUT configuration), the eye mask height and width is derate in the following manner, to include crosstalk as defined in DisplayPort 1.3 Compliance Test Specification:
      i Eye Mask Width Derate (Crosstalk) = 0.04 UI
      ii Eye Mask Height Derate (Crosstalk) = 0.014V
   b If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification (0.38 UI) + Eye Mask Width Derate (Crosstalk) + 2 * Eye Mask Width Derate (Random Jitter)

e Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification (0.09 UI) + Eye Mask Height Derate (Crosstalk)}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification (0.09 UI) + Eye Mask Height Derate (Crosstalk)}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 1,000,000 UI are folded.

13 Measure the eye height of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 63 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 63 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

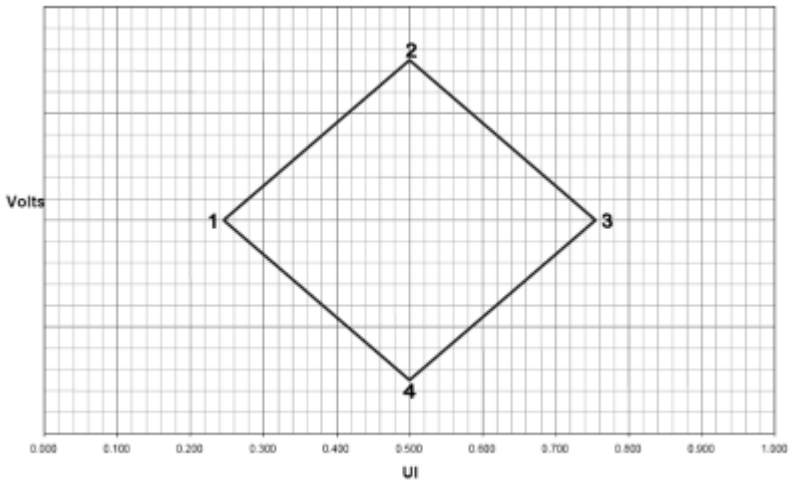


Figure 67 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 64 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045

Table 65 Eye Diagram Mask Coordinates for TP3_EQ (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.35UI	0.00000
2	Any passing UI location between 0.375 and 0.625UI	0.00375
3	Point 1 + 0.35UI	0.00000
4	Same as Point 2	-0.00375

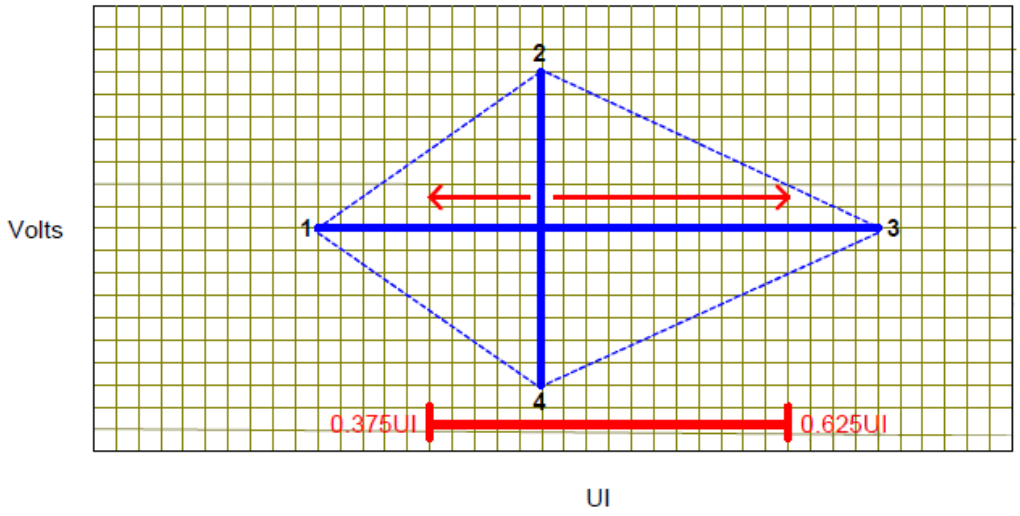


Figure 68 The Eye Mask at TP3_EQ (HBR2 and HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2.8, Table 3-21 for HBR, Table 3-17 for HBR2 and Table 3-16 for HBR3*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1222001, 1222002, 1222003, 1222004 – Total Jitter Test (TP3_EQ) - HBR2CPAT
- 1222011, 1222012, 1222013, 1222014 – Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1221001, 1221002, 1221003, 1221004 – Total Jitter Test (TP3_EQ) - D10.2
- 1221011, 1221012, 1221013, 1221014 – Total Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1322001, 1322002, 1322003, 1322004 – Total Jitter Test (TP3_EQ)
- 1322011, 1322012, 1322013, 1322014 – Total Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

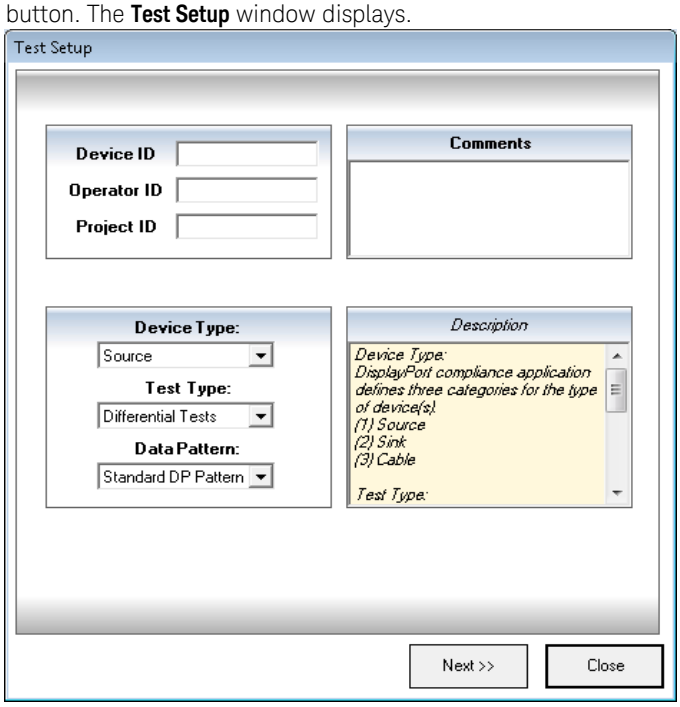
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2, HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



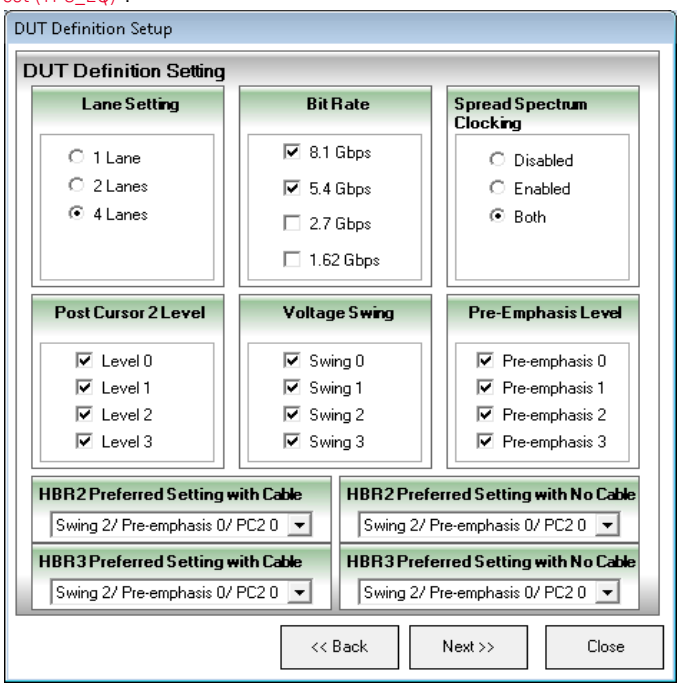
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

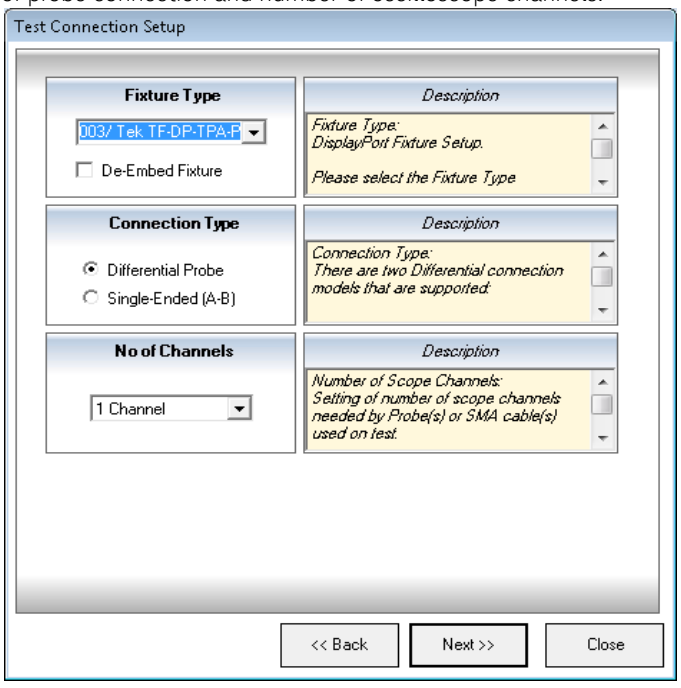
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

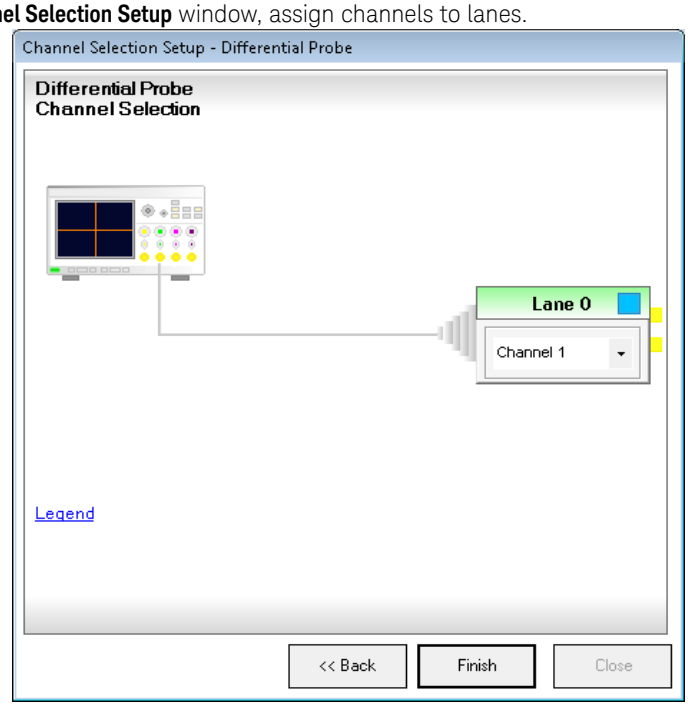
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

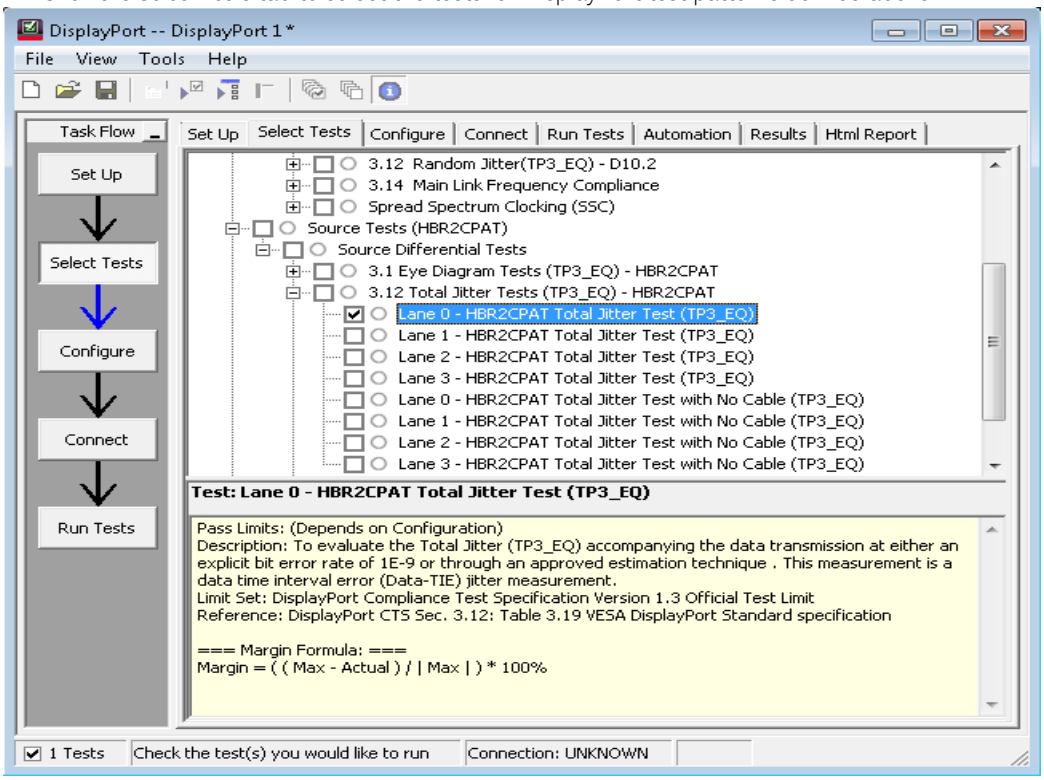


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 66 Total Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	0.65 UI
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.580 UI*

* The HBR2 limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 67 Total Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) and High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	0.40 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2.7.2, Table 3-15*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-11*

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Deterministic Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1236001, 1236002, 1236003, 1236004 – Deterministic Jitter Test (TP3_EQ) - HBR2CPAT
- 1236011, 1236012, 1236013, 1236014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1235001, 1235002, 1235003, 1235004 – Deterministic Jitter Test (TP3_EQ) - D10.2
- 1235011, 1235012, 1235013, 1235014 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1336001, 1336002, 1336003, 1336004 – Deterministic Jitter Test (TP3_EQ)
- 1336011, 1336012, 1336013, 1336014 – Deterministic Jitter Test with No Cable Model (TP3_EQ)

Test Overview

The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

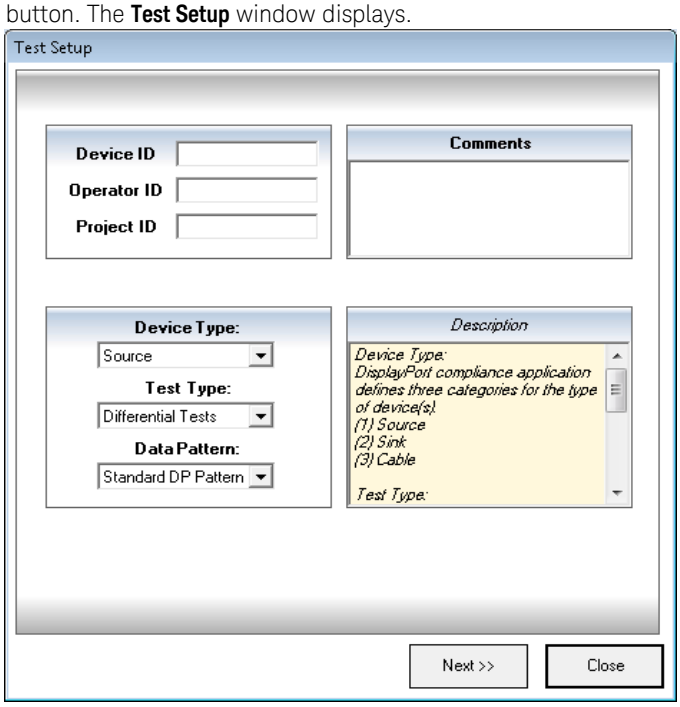
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2, HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



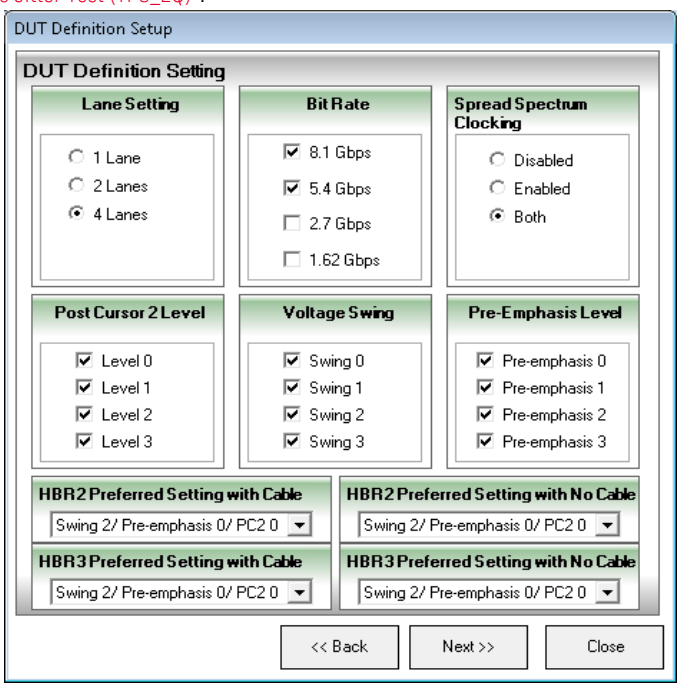
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

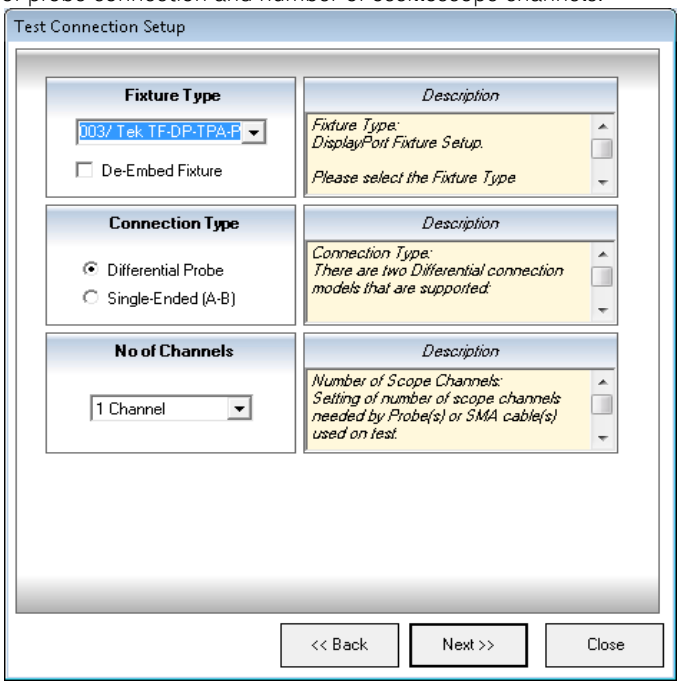
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

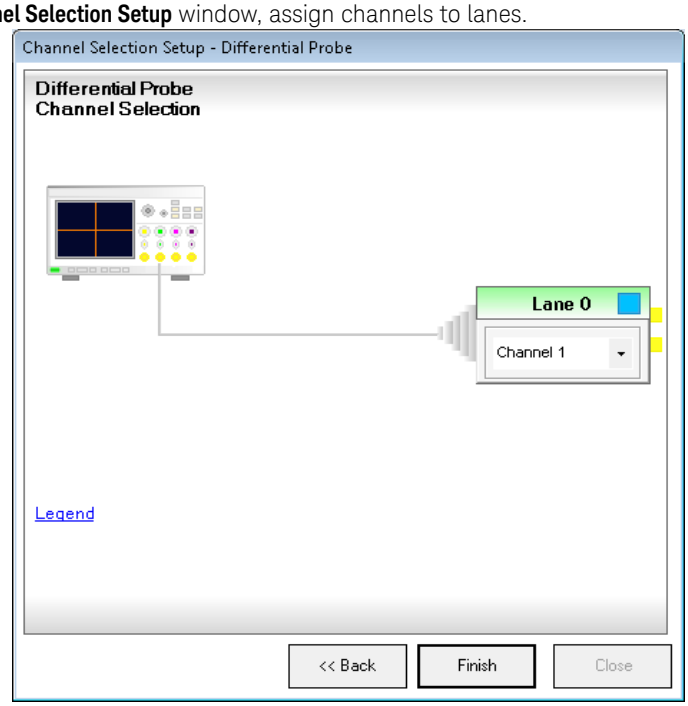
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Deterministic Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

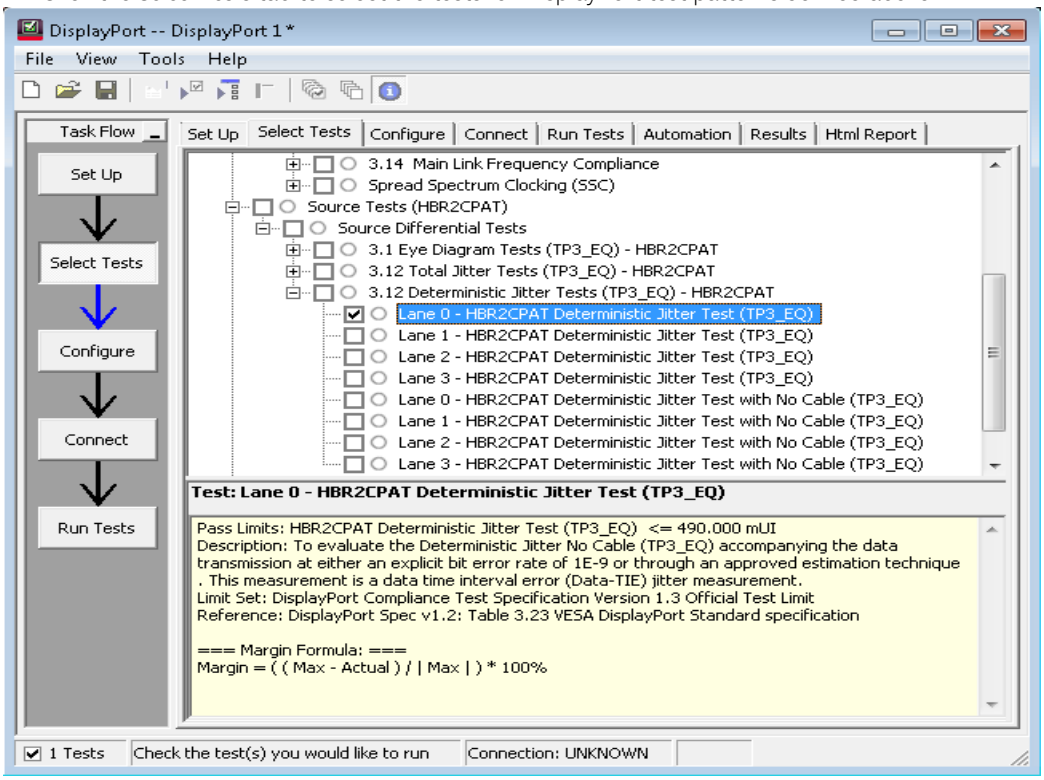


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 68 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) and High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 69 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) and High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	0.27 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2.7.2, Table 3-15*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-11*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Random Jitter Test (TP3_EQ)

Test ID

For Standard DP Pattern:

- 1238001, 1238002, 1238003, 1238004 – Random Jitter Test (TP3_EQ) - D10.2
- 1238011, 1238012, 1238013, 1238014 – Random Jitter Test with No Cable Model (TP3_EQ) - D10.2

For Arbitrary Pattern:

- 1338001, 1338002, 1338003, 1338004 – Random Jitter Test (TP3_EQ) - D10.2
- 1338011, 1338012, 1338013, 1338014 – Random Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

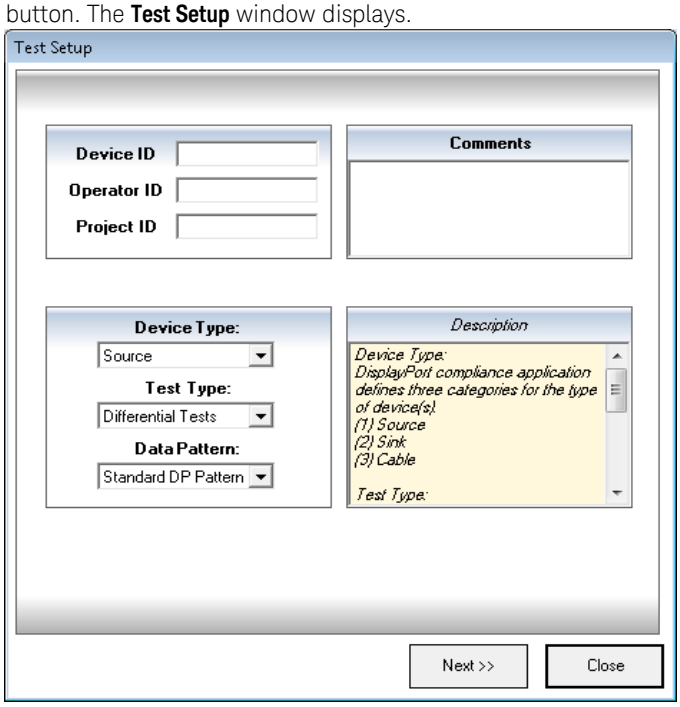
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2, HBR3
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	All test lanes supported
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



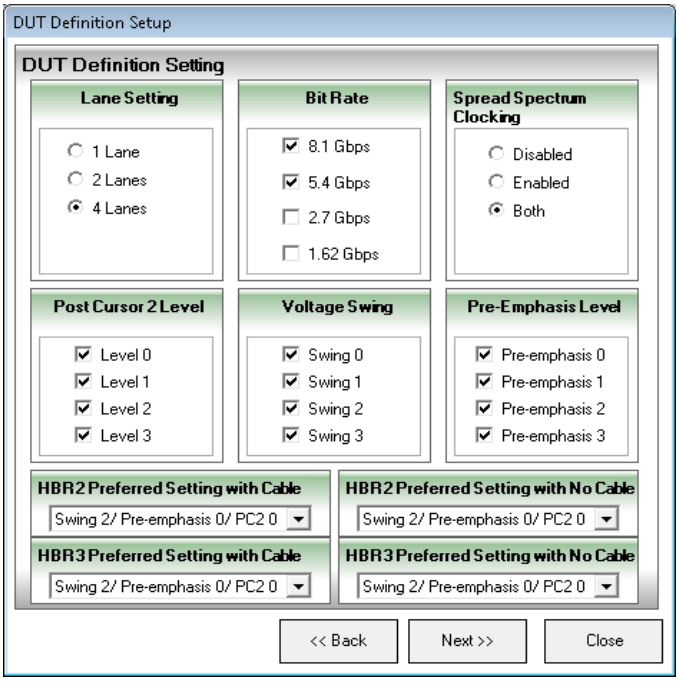
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

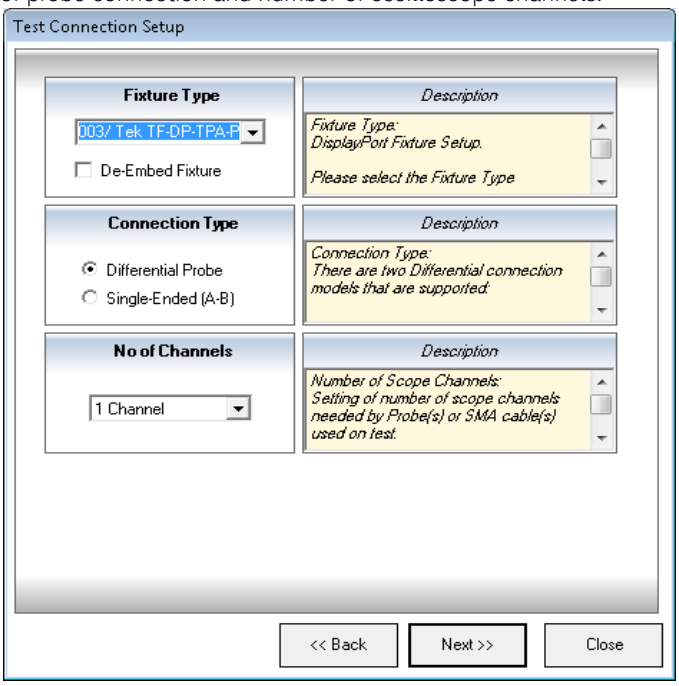
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

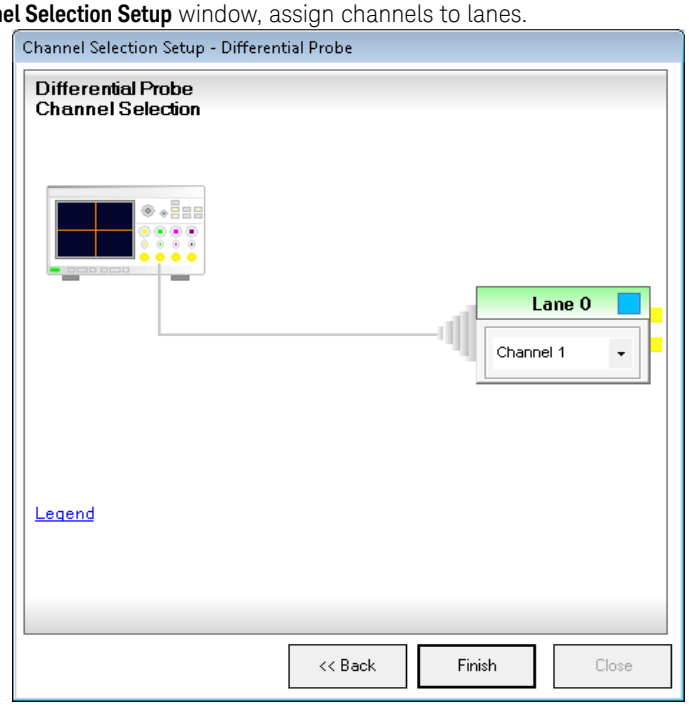
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Random Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

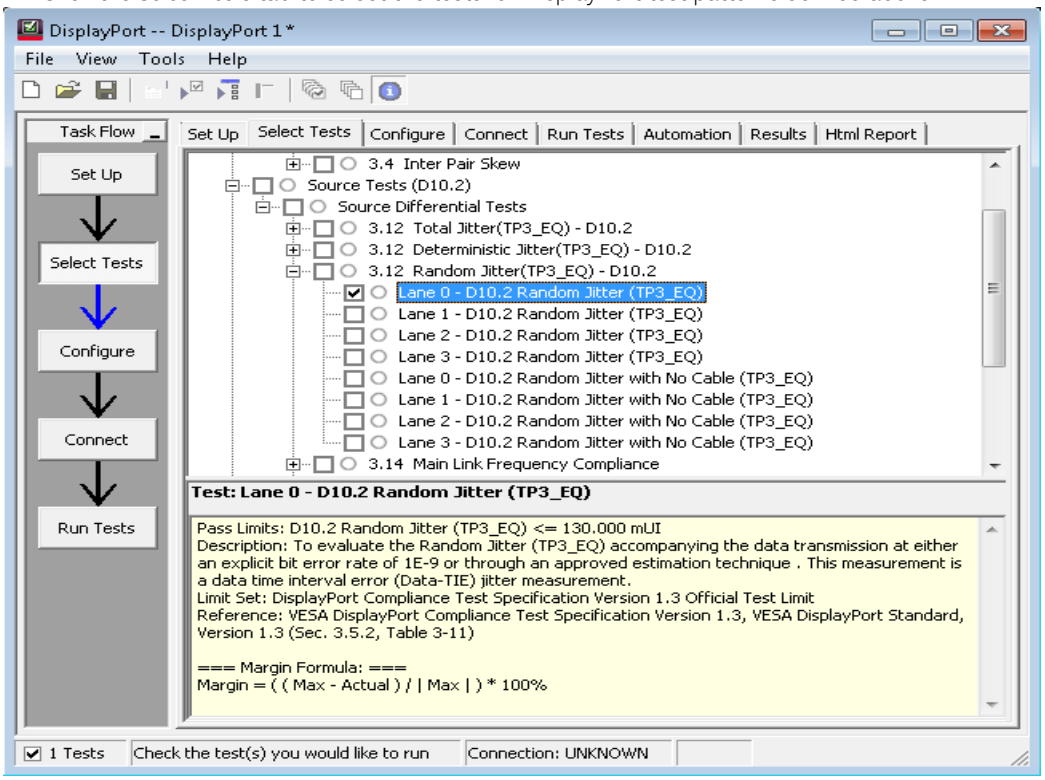


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 70 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) and High-Bit Rate 3 (8.1 Gb/s per lane)	
A_{p-p}	0.13 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-11*

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source AC Common Mode Test (Informative)

Test ID

For Standard DP Pattern:

- 12110001, 12110002, 12110003, 12110004 – AC Common Mode Test (Informative)

For Arbitrary Pattern:

- 13110001, 13110002, 13110003, 13110004 – AC Common Mode Test (Informative)

Test Overview

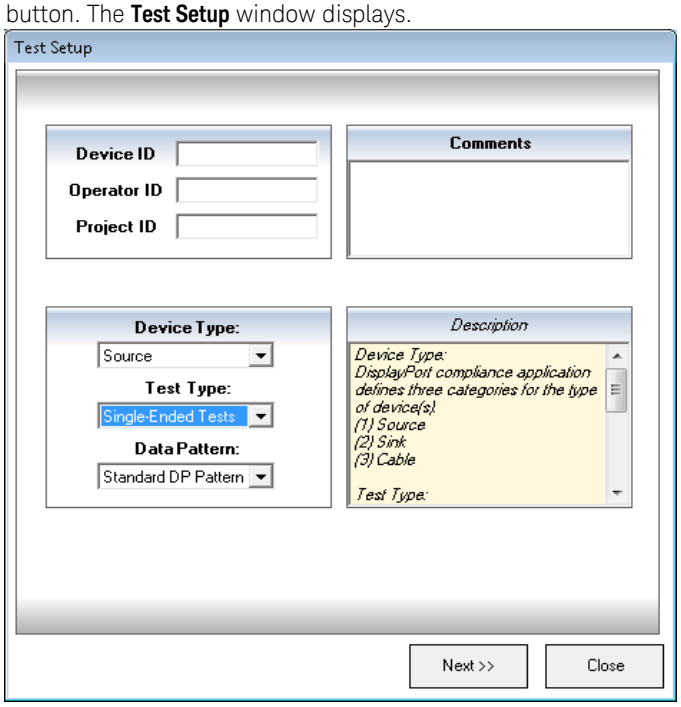
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR3)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.3 Standard
Post-Cursor2 Level	Level 0
Test Lane	All test lanes are supported
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



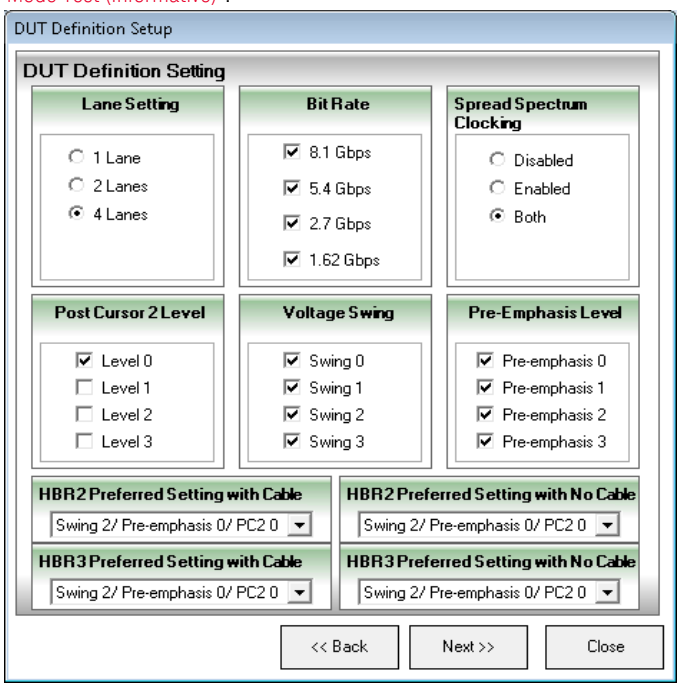
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

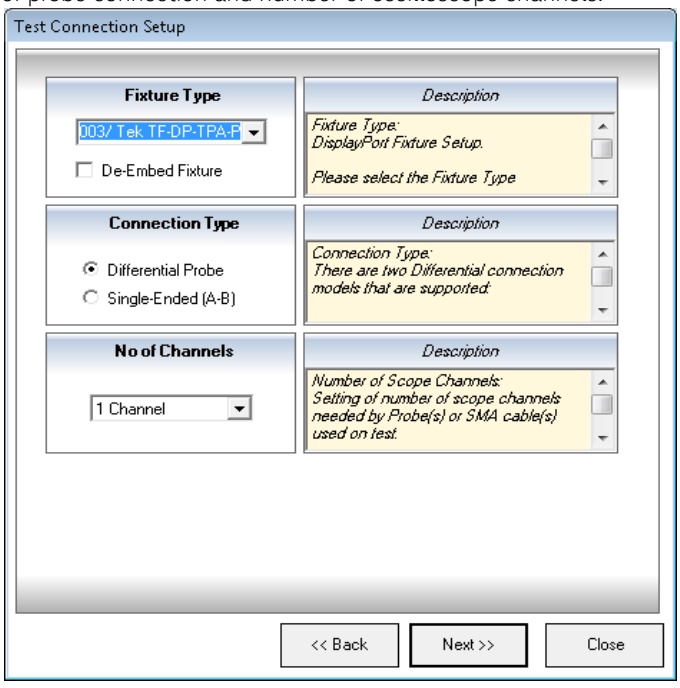
b Select **Device Type:** as **Source**, **Test Type:** as **Single-Ended Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

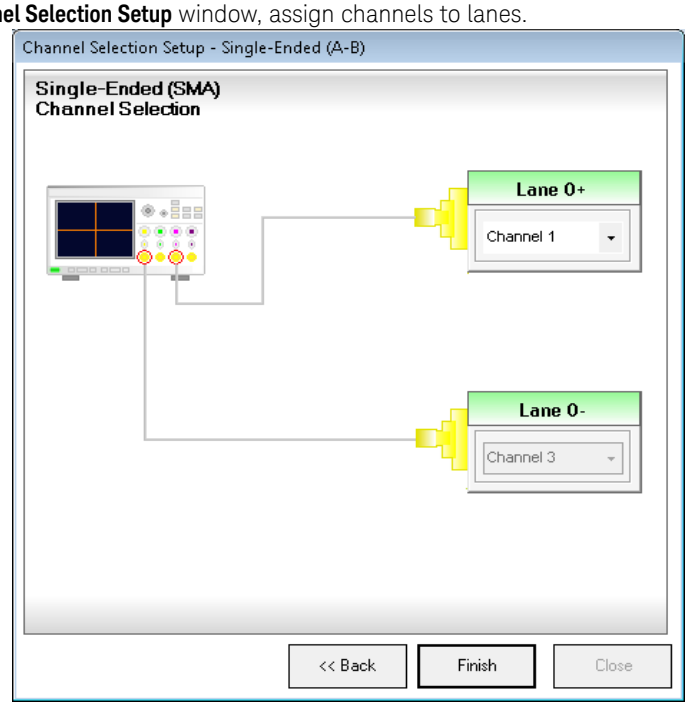
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for AC Common Mode Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

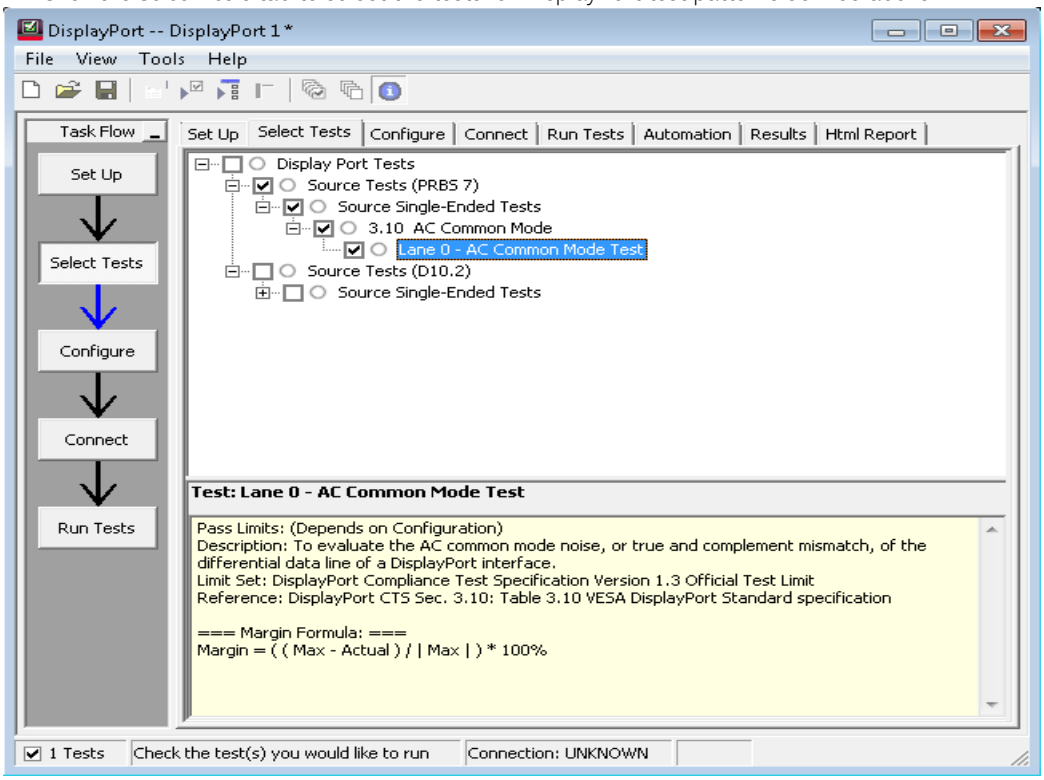


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled ["Filter" configuration variable set to "High Pass Filter", "Low Pass Filter" or "None" (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.
8 Get the mean for the V_{rms} measurement.
9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2 and HBR3:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.10*
- *VESA DisplayPort (DP) Standard Version 1.3, Section D.2, Table D-3*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

Source Intra-Pair Skew Test (Informative)

Test ID

For Standard DP Pattern:

- 12100001, 12100002, 12100003, 12100004 – Intra-Pair Skew Test (Informative)

For Arbitrary Pattern:

- 13100001, 13100002, 13100003, 13100004 – Intra-Pair Skew Test (Informative)

Test Overview

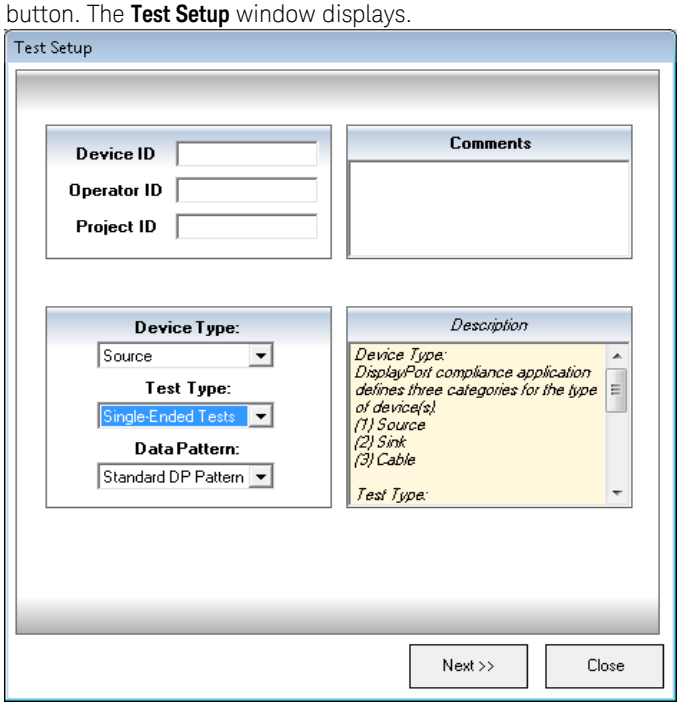
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR3)
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported For one lane operation: Lane 0+ to Lane 0- For two lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- For four lane operation: Lane 0+ to Lane 0- Lane 1+ to Lane 1- Lane 2+ to Lane 2- Lane 3+ to Lane 3-
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



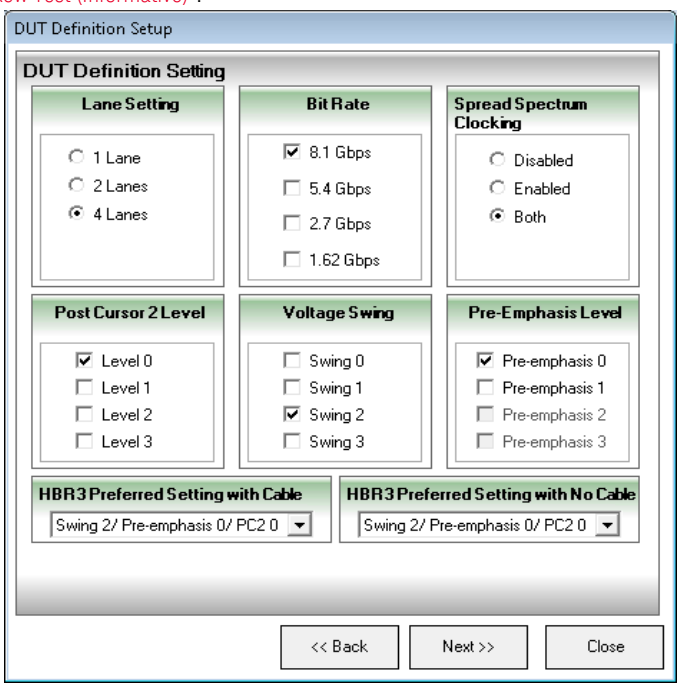
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

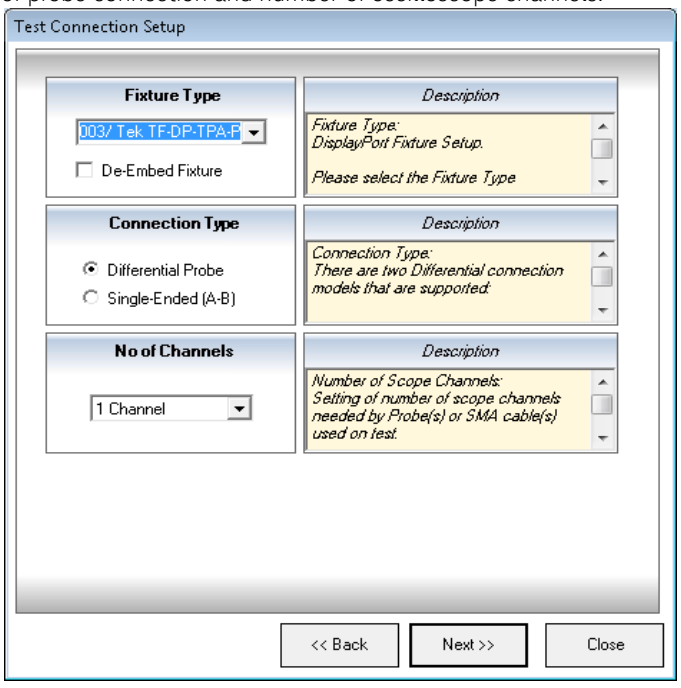
b Select **Device Type:** as **Source**, **Test Type:** as **Single-Ended Tests** and **Data Pattern:** as either **Standard DP Pattern** (selected by default) or **Arbitrary Pattern** (if you have a DisplayPort Test Pattern with specifications different from the standards).

c Click **Next**.

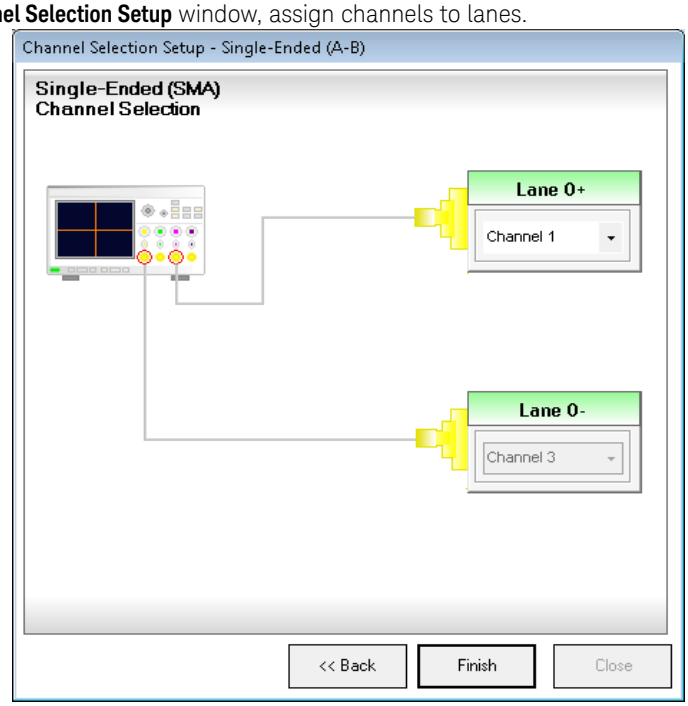
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Intra-Pair Skew Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

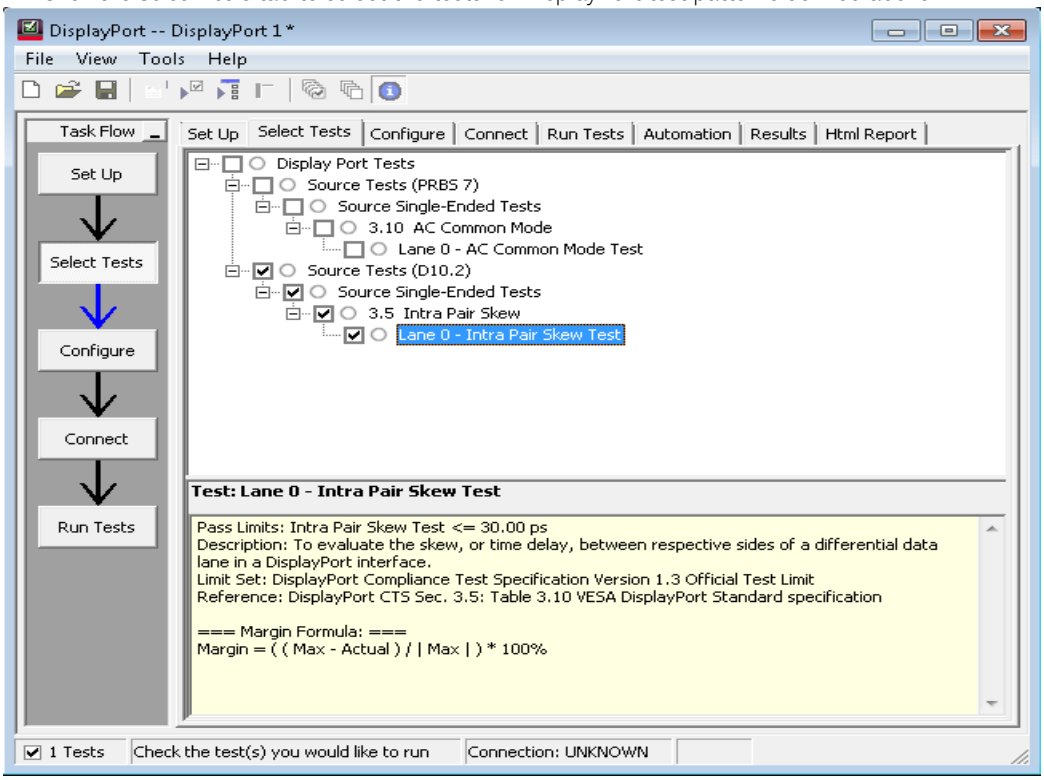


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Source Tests" on page 291 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find V_{HIGH} by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find V_{LOW} by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:
   a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.
   b Set up InfiniiScan to trigger on the desired pattern.
   c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

   d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

   e Acquire the signal until you measure 100 edges.
   f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra-Pair skew ≤ 30 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.5*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.5.2, Table 3-10*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

10 DisplayPort 1.3 Sink Tests

Overview

Test Point Definition for DisplayPort 1.3 Sink Tests

NOTE Sink Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Sink DUT at Test Point 3(TP3) as shown in Figure 69. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

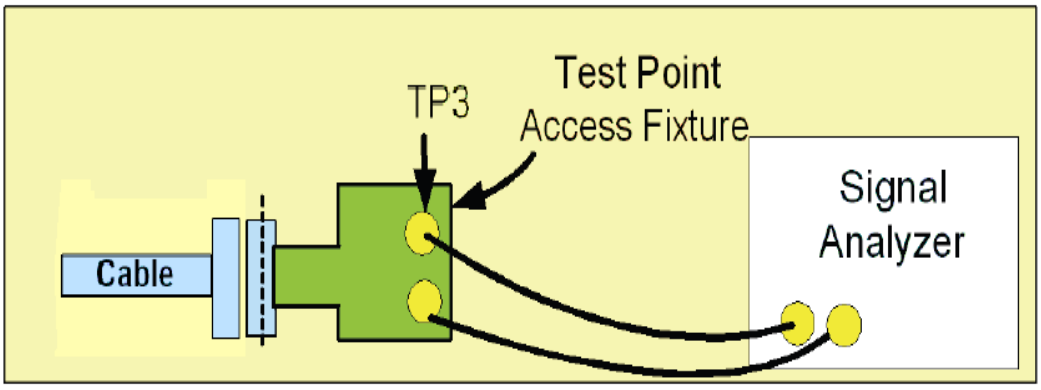


Figure 69 Test Point 3 Connection for DisplayPort 1.3 Sink Tests

Table 71 defines the test point fixtures and instruments used for DisplayPort 1.3 Sink Tests:

Table 71 Test Point Fixtures and Instruments for DisplayPort 1.3 Sink Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Calibration of Stress Signal

For the calibration of the stress signal, you must test the stress signal in the manner shown in the Figure 70 for RBR and Figure 71 for HBR and HBR2.

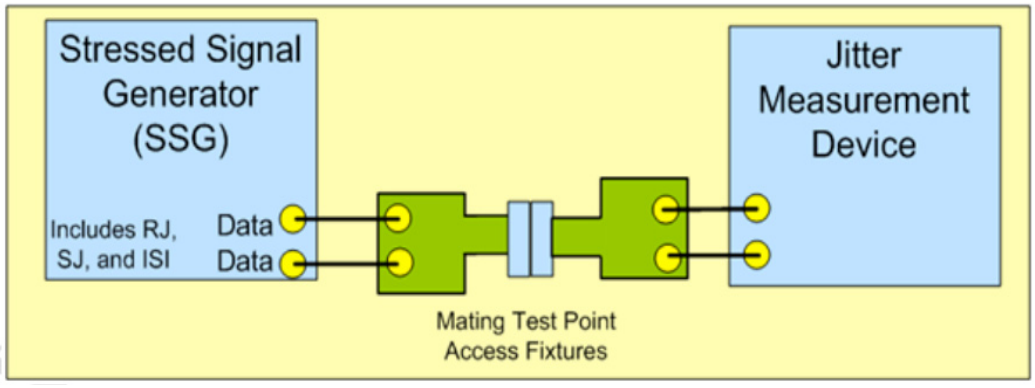


Figure 70 Test Point 3 Connection for Stress Signal Calibration of RBR

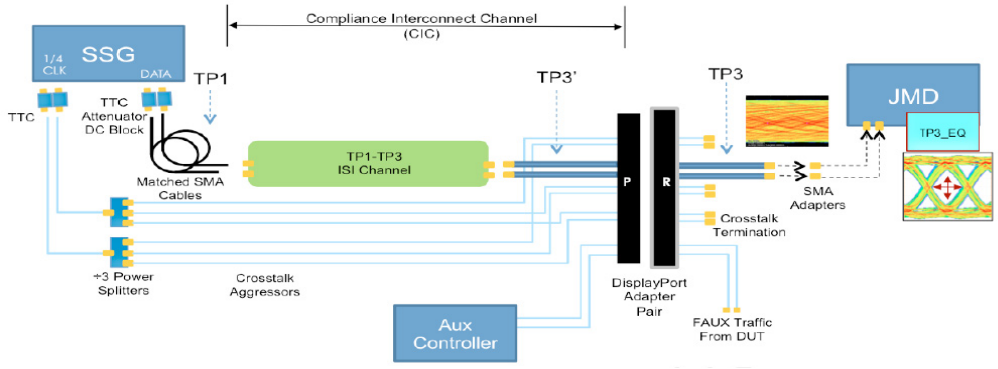


Figure 71 Test Point 3 Connection for Stress Signal Calibration of HBR and HBR2

Table 72 defines the Test Point 3 Connections for Stress Signal Calibration:

Table 72 Test Point Connections for Stress Signal Calibration

Test Requirement	Device Used
Stress Signal Generator (SSG)	Bit Error Rate Tester ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Jitter Measurement Device (JMD)	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Sink Tests

Perform the following steps before you run the compliance tests on the sink device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 72).

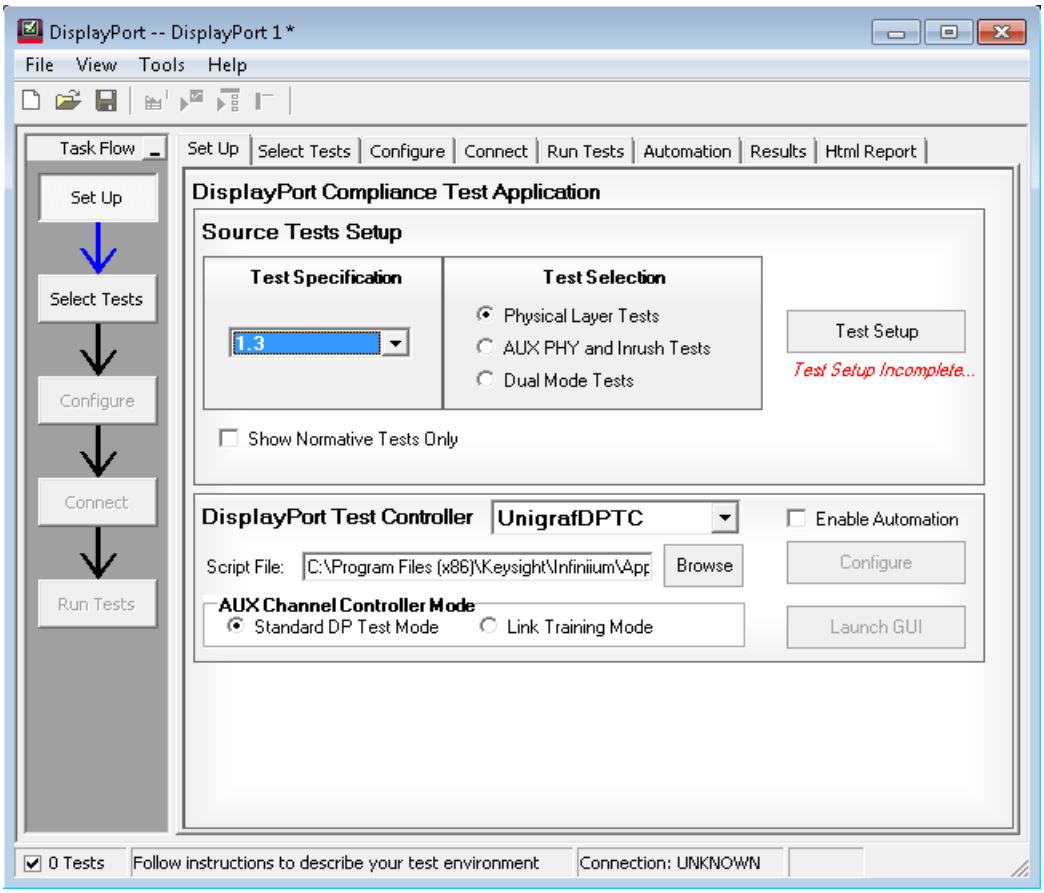


Figure 72 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.3 Standards, select **1.3** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.3 Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

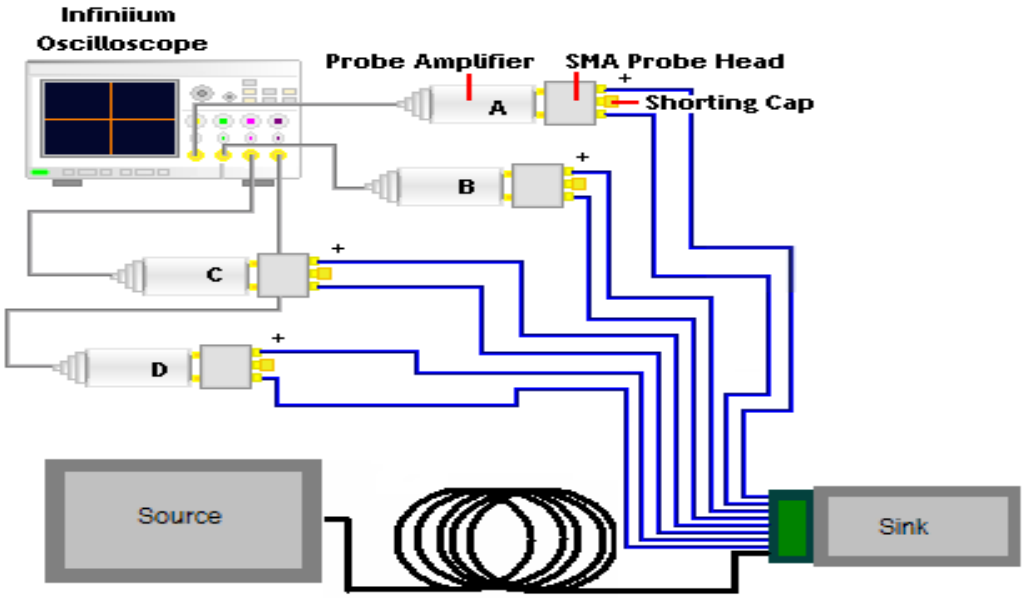


Figure 73 Sample connection diagram for DisplayPort 1.3 Sink Tests

Sink Eye Diagram Test

Test ID

12140001, 12140002, 12140003, 12140004 – Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a

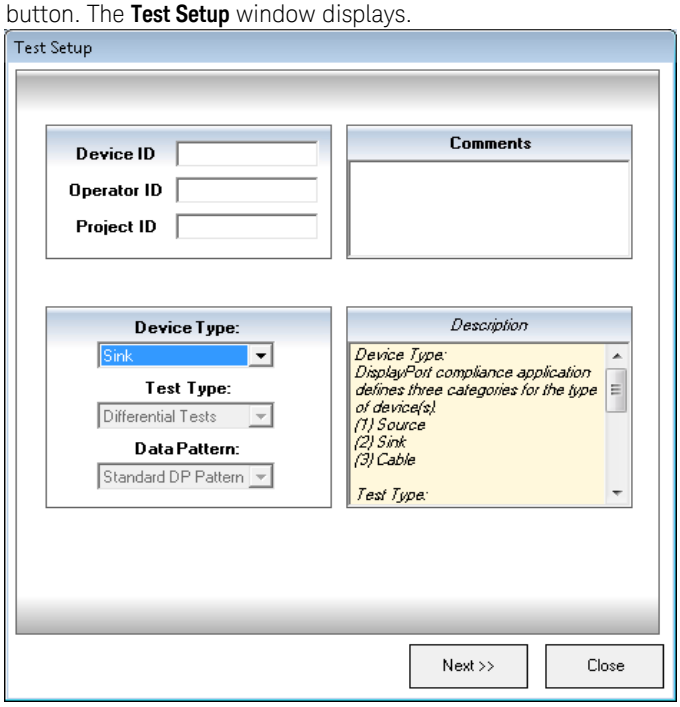
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



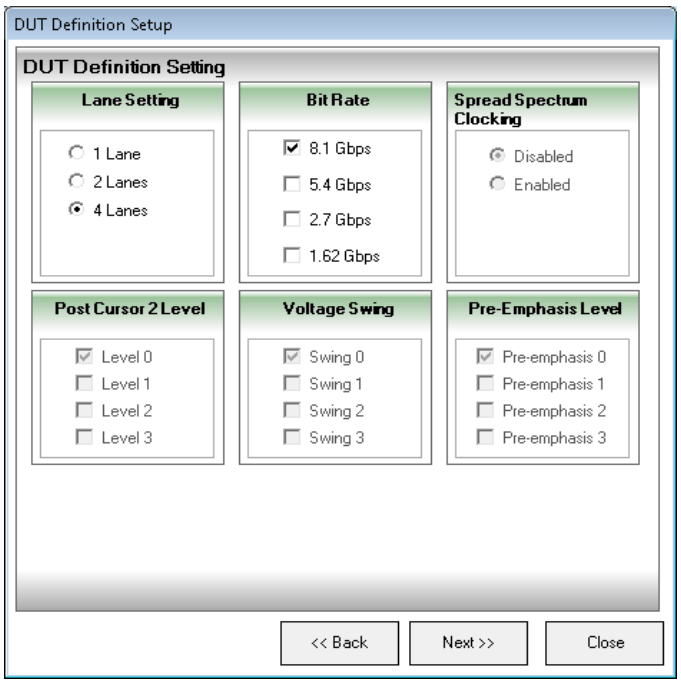
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

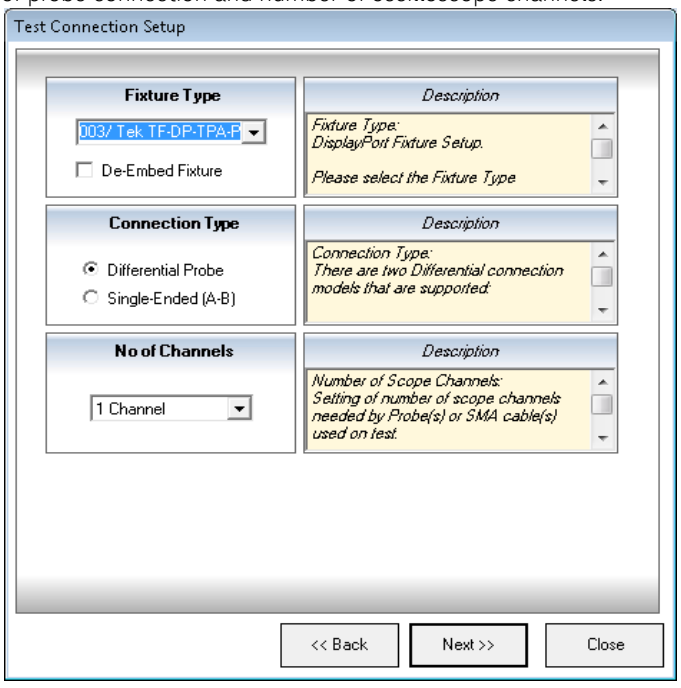
b Select **Device Type:** as **Sink**, **Test Type:** and **Data Pattern:** automatically gray out.

c Click **Next**.

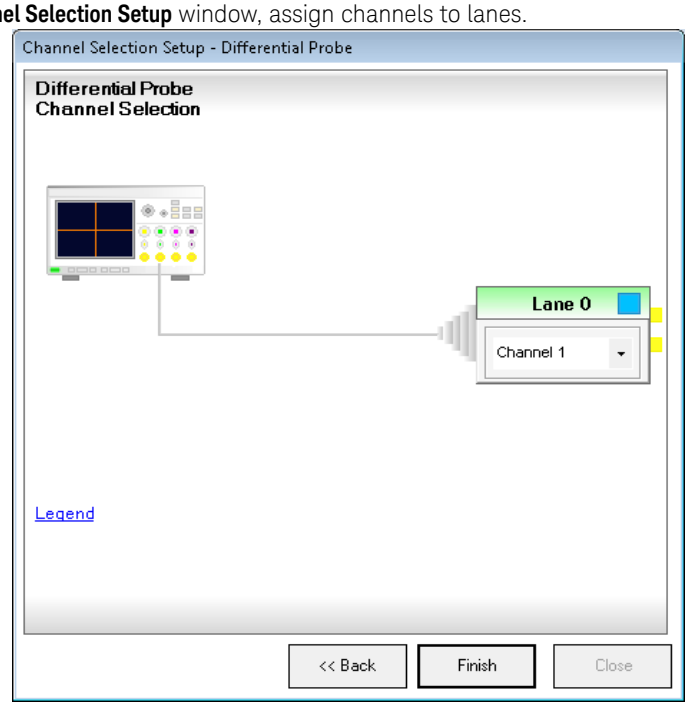
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

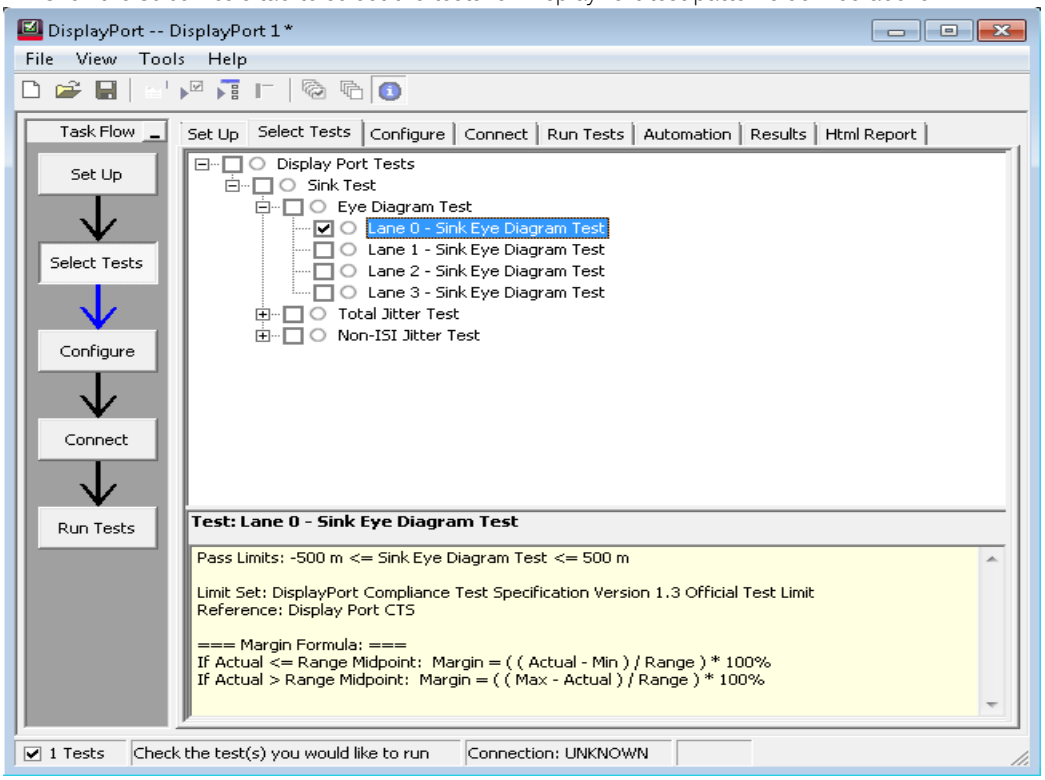


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Sink Tests" on page 410 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 73 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 73 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

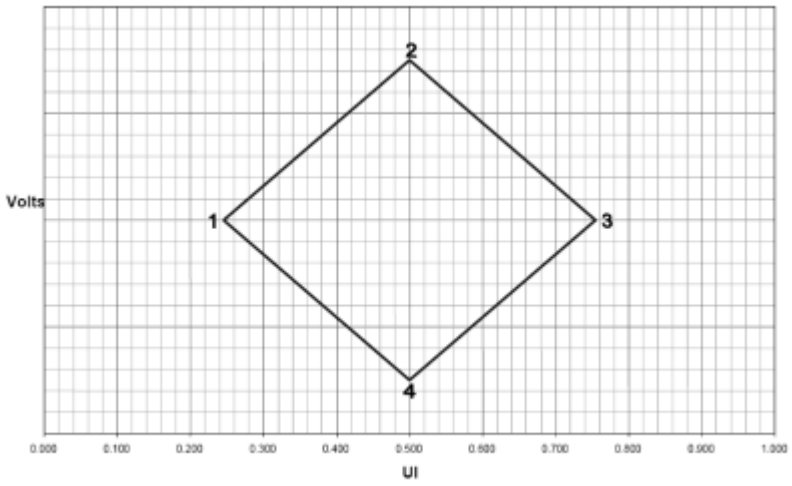


Figure 74 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 74 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045

Table 75 Eye Diagram Mask Coordinates for TP3_EQ (HBR3)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.35UI	0.00000
2	Any passing UI location between 0.375 and 0.625UI	0.00375
3	Point 1 + 0.35UI	0.00000
4	Same as Point 2	-0.00375

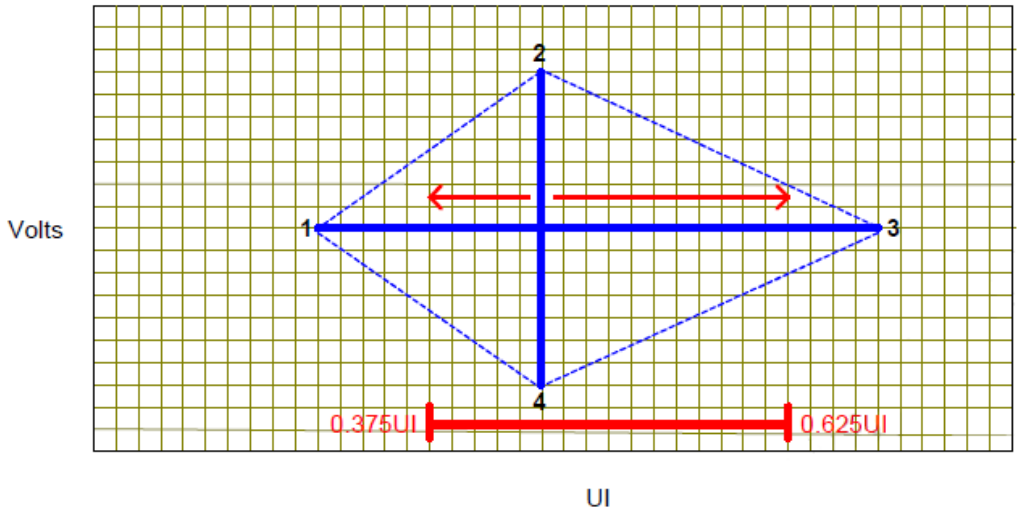


Figure 75 The Eye Mask at TP3_EQ (HBR2 and HBR3)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001, 12210002, 12210003, 12210004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

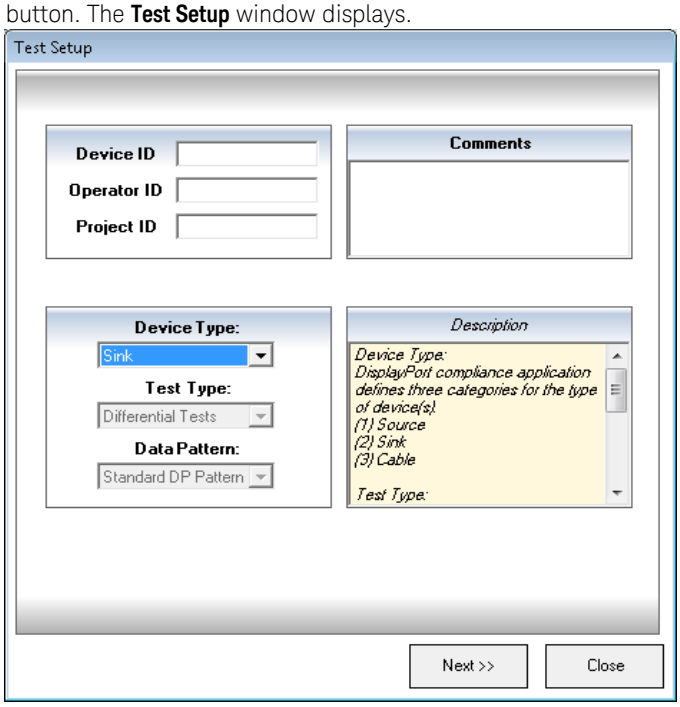
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



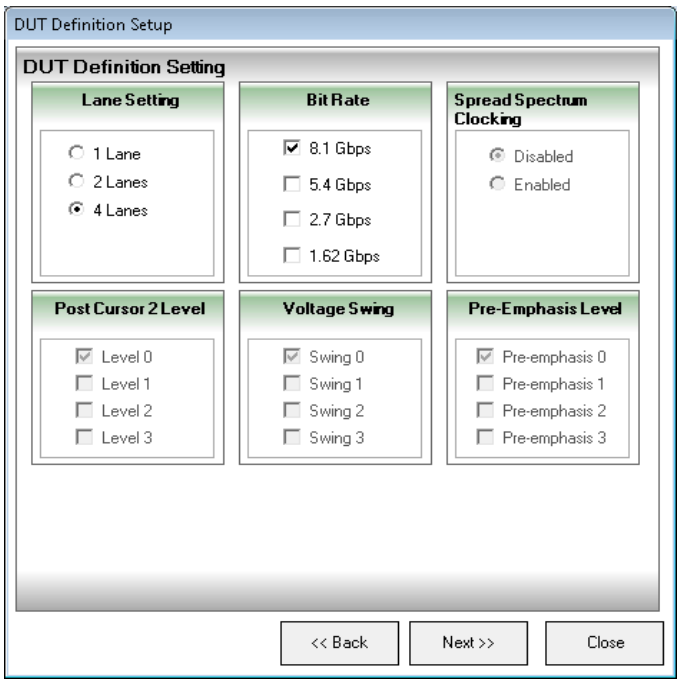
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

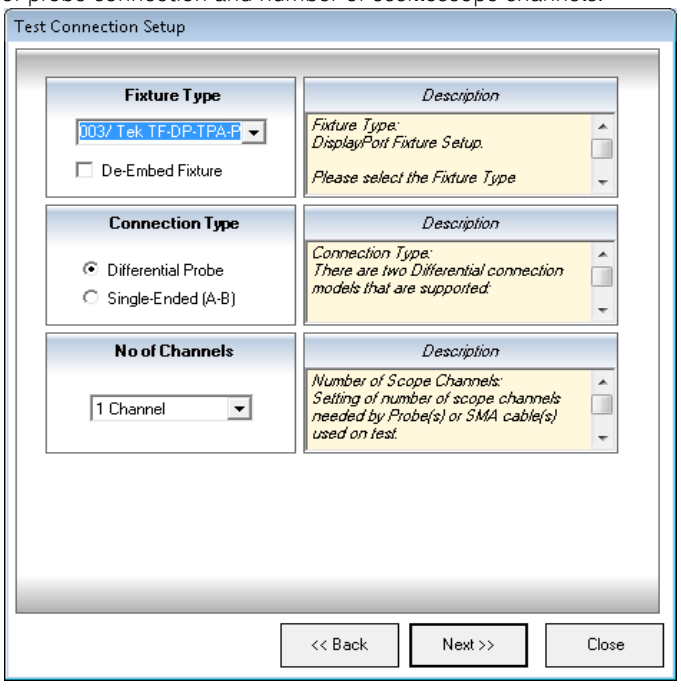
b Select **Device Type:** as **Sink**, **Test Type:** and **Data Pattern:** automatically gray out.

c Click **Next**.

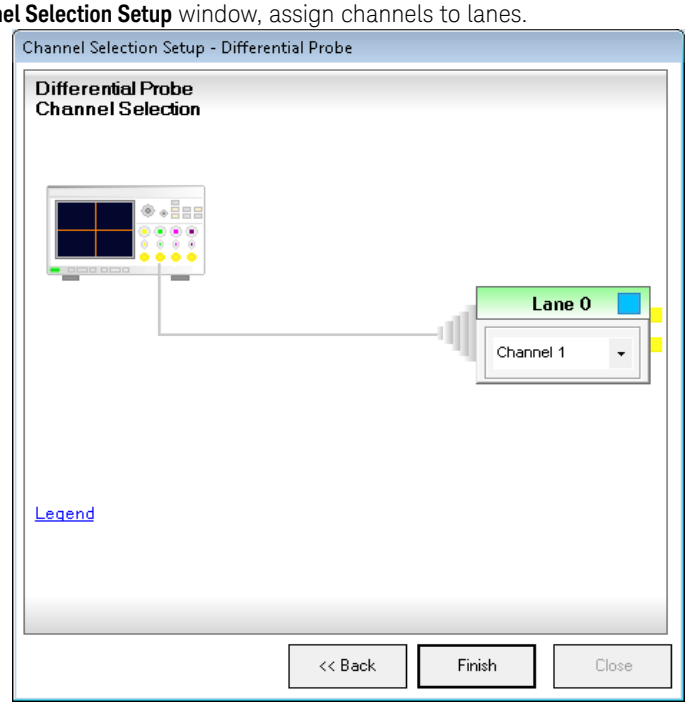
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

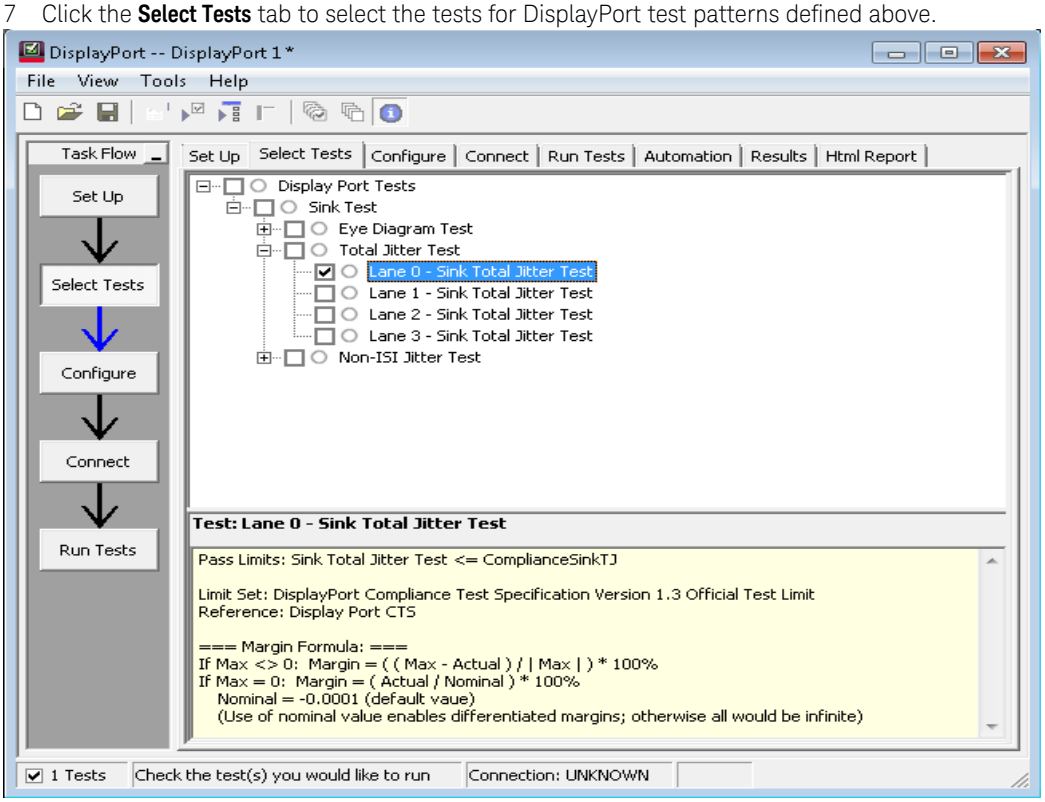


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Sink Tests" on page 410 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 76 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI limit in DisplayPort 1.2a Standard.

Table 77 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Test

Test ID

12220001, 12220002, 12220003, 12220004 – Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Calculate Non-ISI Jitter using the following equation:

$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

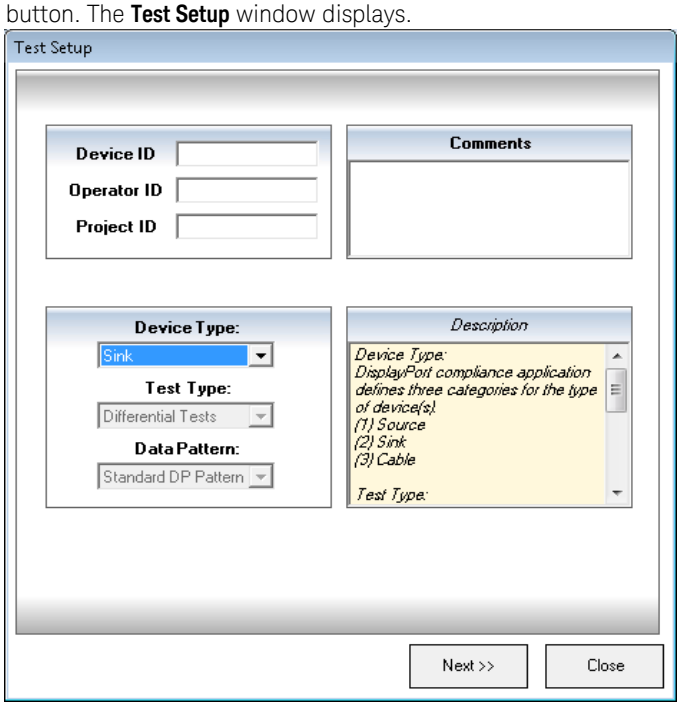
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR3–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR3)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR3–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



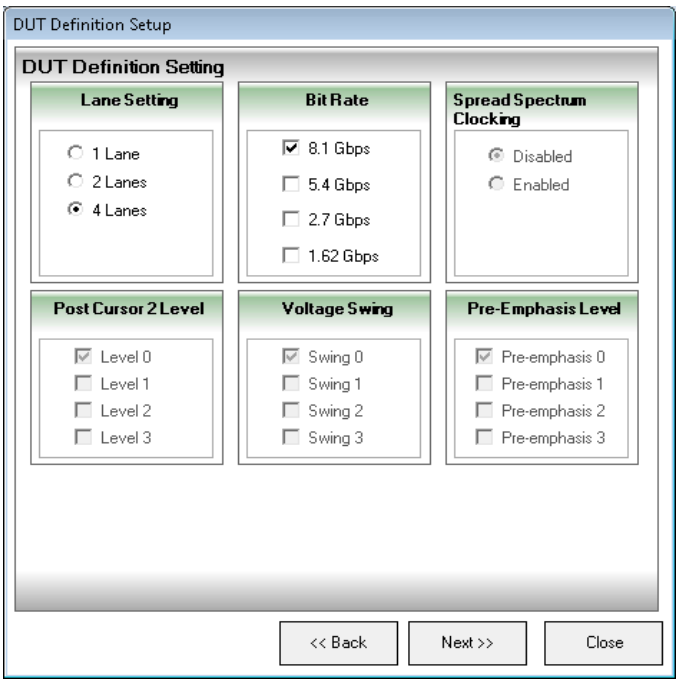
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

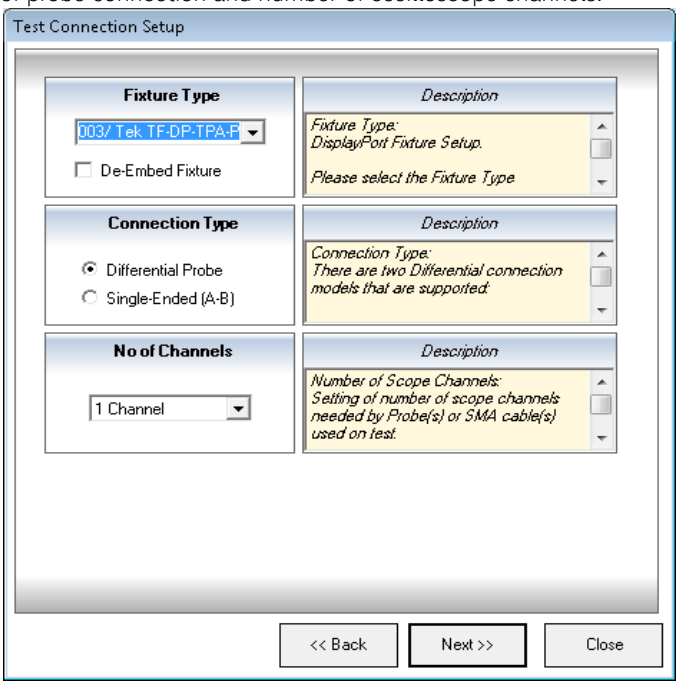
b Select **Device Type:** as **Sink**, **Test Type:** and **Data Pattern:** automatically gray out.

c Click **Next**.

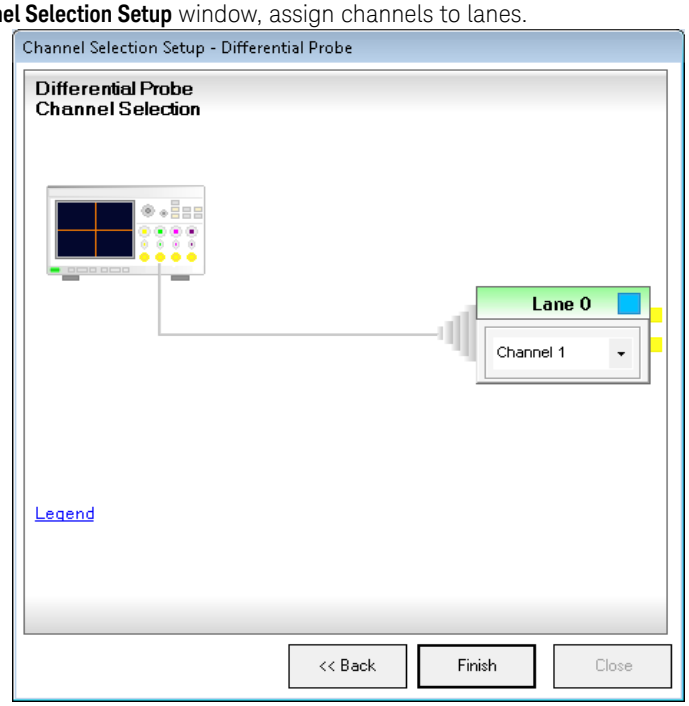
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

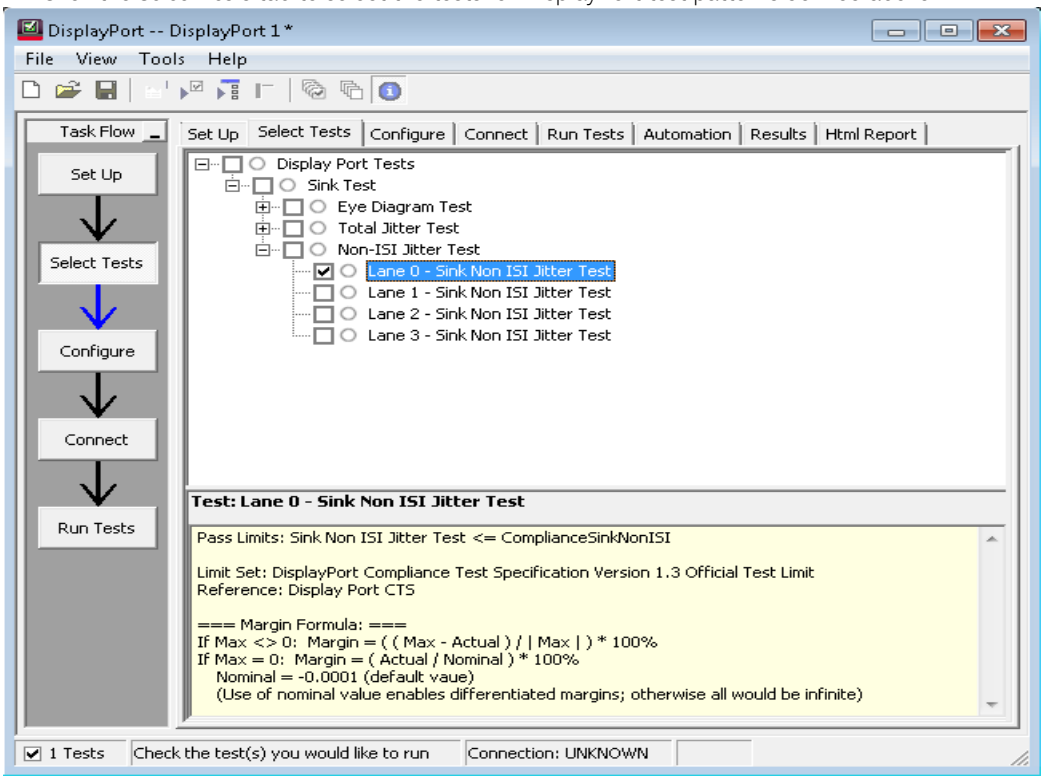


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Sink Tests" on page 410 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 78 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 79 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

11 DisplayPort 1.3 Cable Tests

Overview

Test Point Definition for DisplayPort 1.3 Cable Tests

NOTE Cable Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Cable DUT at Test Point 3 (TP3) as shown in Figure 76. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

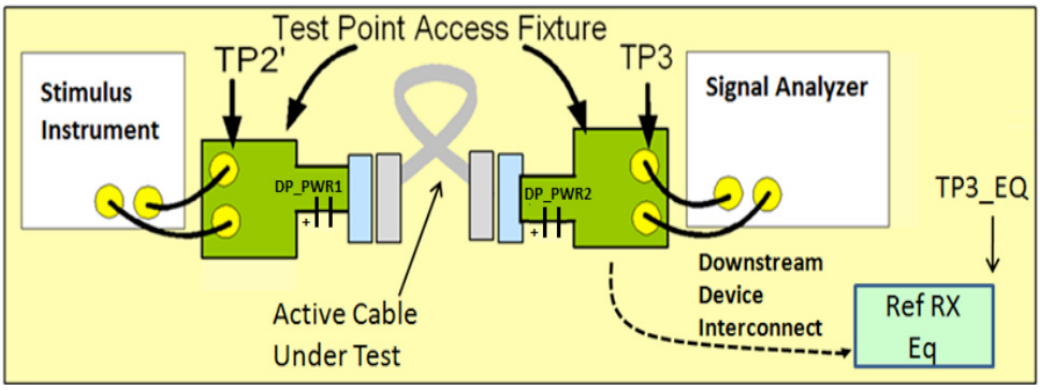


Figure 76 Test Point 3 Connection for DisplayPort 1.3 Cable Tests

Table 80 defines the test point fixtures and instruments used for DisplayPort 1.3 Cable Tests:

Table 80 Test Point Fixtures and Instruments for DisplayPort 1.3 Cable Tests

Test Requirement	Device Used
Stimulus Instrument	Pulse Pattern Generator ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Table 81 defines the input signal parameters applied by the stimulus instrument at TP2:

Table 81 Input Signal Parameters by Stimulus Instrument

RBR	▪ Reference Table 3-22 and Table 3-24, DP 1.2a ▪ Edge Rate (20-80): 155-165ps (260mUI) ▪ Eye Height: 400mV ▪ Total Jitter: 270mUI ▪ ISI: 100mUI ▪ Random Jitter (rms): 7.9mUI ▪ Sinusoidal Jitter: ~75mUI at 20MHz (Adjust to achieve Total Jitter)
HBR	▪ Reference Table 3-22 and Table 3-23, DP 1.2a ▪ Edge Rate (20-80): 90-100ps (260mUI) ▪ Eye Height: 350mV ▪ Total Jitter: 420mUI ▪ ISI: 144mUI ▪ Random Jitter (rms): 13.2mUI ▪ Sinusoidal Jitter: ~117mUI at 20MHz (Adjust to achieve Total Jitter)

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Cable Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 77).

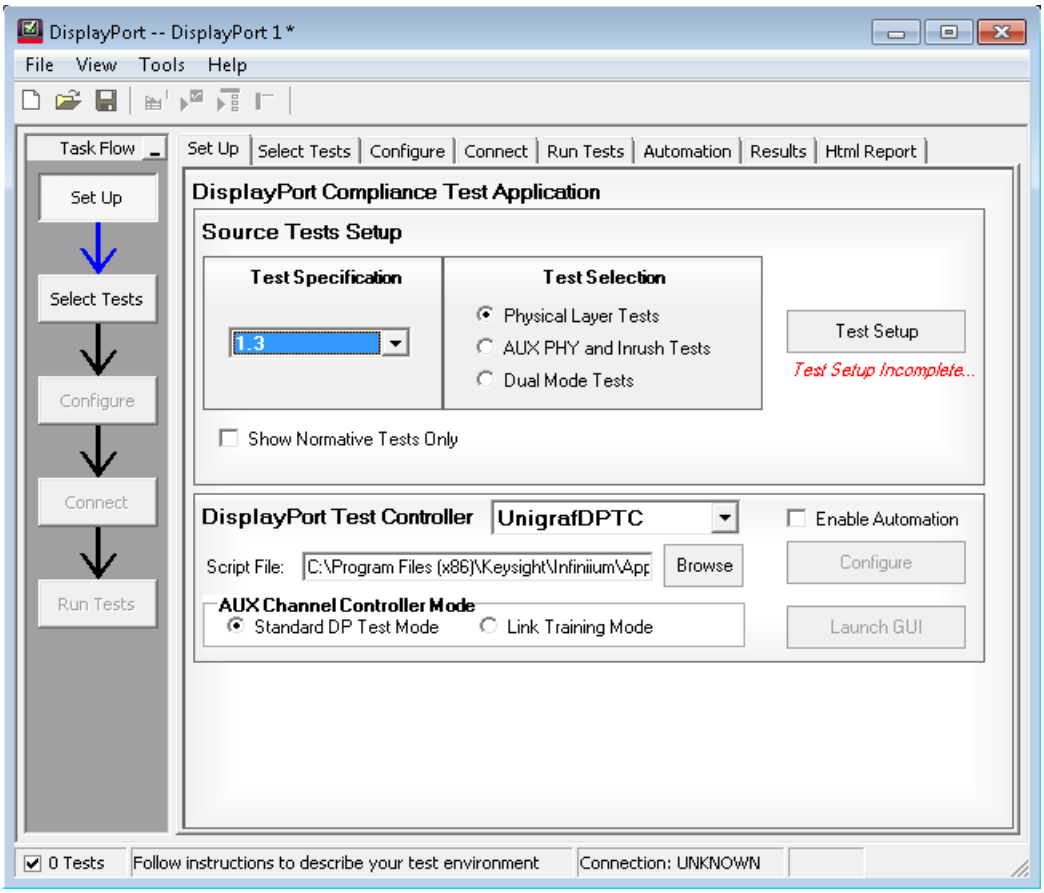


Figure 77 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.3 Standards, select **1.3** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for DisplayPort 1.3 Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

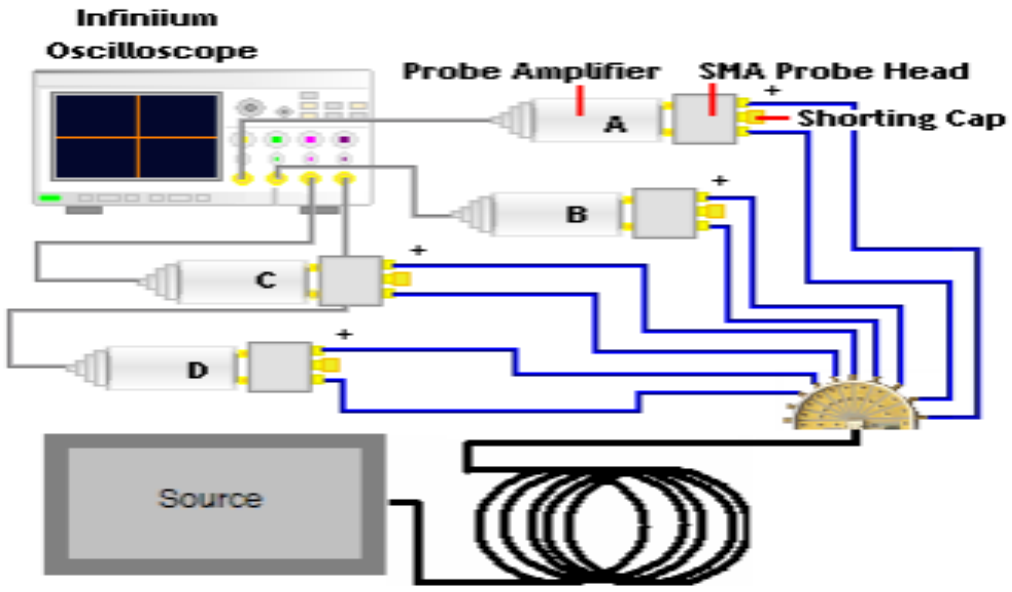


Figure 78 Sample connection diagram for DisplayPort 1.3 Cable Tests

Cable Eye Diagram Test

Test ID

12150001, 12150002, 12150003, 12150004 – Eye Diagram Test

Test Overview

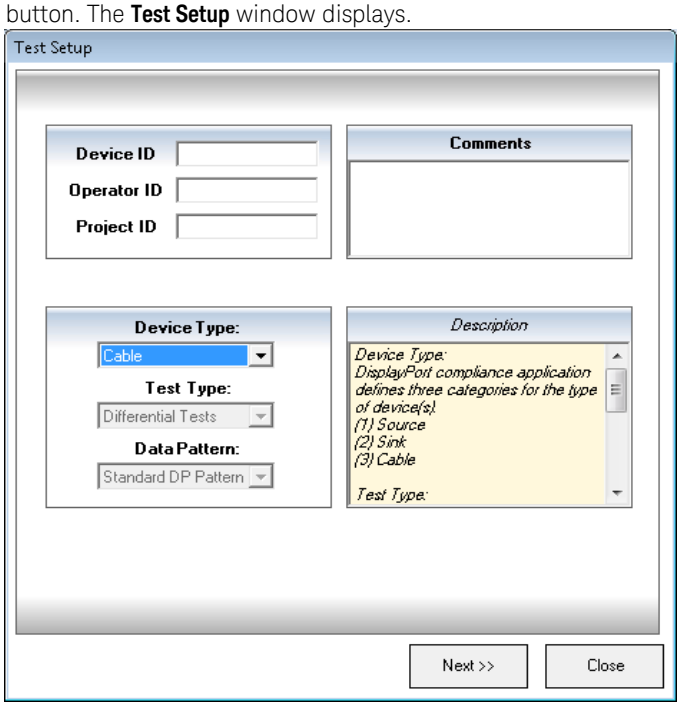
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 81
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



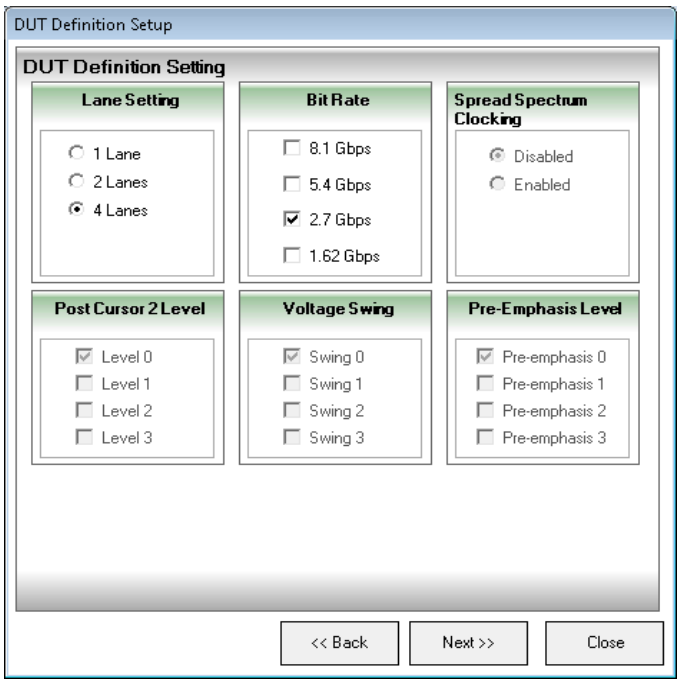
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

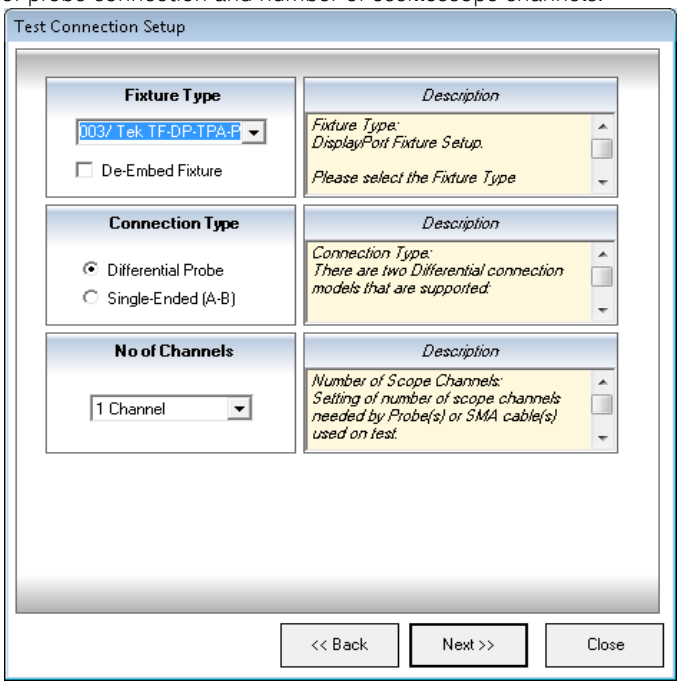
b Select **Device Type:** as **Cable**, **Test Type:** and **Data Pattern:** automatically gray out.

c Click **Next**.

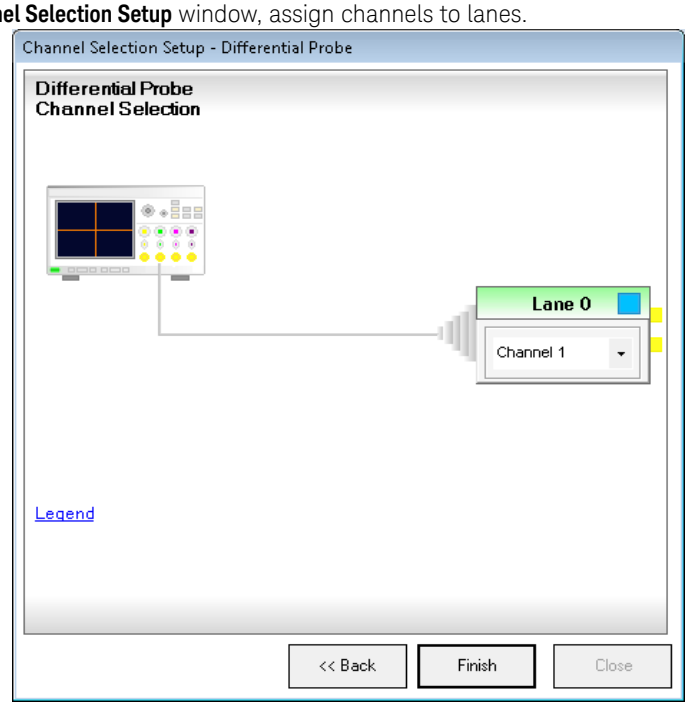
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Cable Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

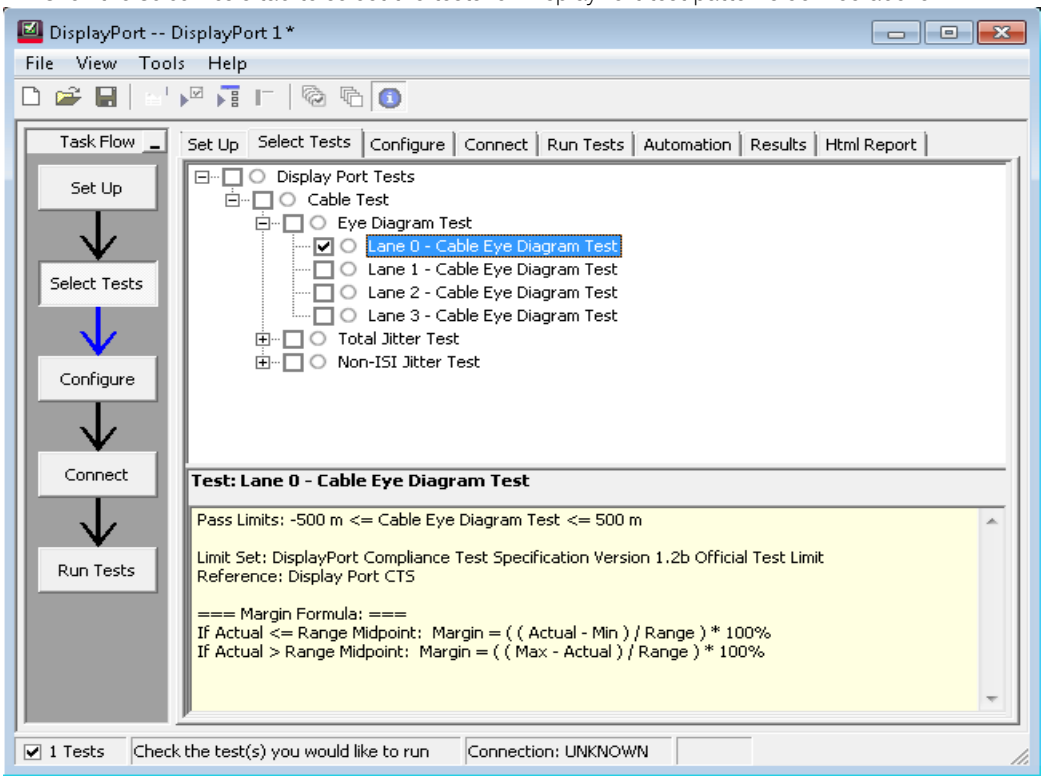


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Cable Tests" on page 436 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1. Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2. Acquire and verify the input signal.
   a. Verify the trigger and the amplitude of the input signal.
   b. Scale the vertical display of the input signal to the optimum value.
   c. Measure V_{TOP} and V_{BASE} of the input signal.
3. Create FUNC3 signal, which is the magnify signal of the input signal.
4. Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a. Scale the vertical display of the equalized signal to the optimum value.
   b. Measure V_{TOP} and V_{BASE} of the equalized signal.
   c. Measure the data rate of the equalized signal.
5. Set up the parameter of the measurement:
   a. Enable measurement of all edges to obtain a statistical value of the measurement.
   b. Set up the measurement threshold.
   c. Set up the Clock Recovery as described in the section “Clock Recovery”.
6. Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7. Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8. Set up the parameter for the Mask Test.
   a. Load the eye mask based on the settings in the Configuration Variable.
   b. Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c. Run the eye mask until 1,000,000 UI are folded.
9. Measure the jitter of the eye diagram using the Histogram.
10. Check for any signal trajectories that may have entered into the mask.
11. Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 82 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 82 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

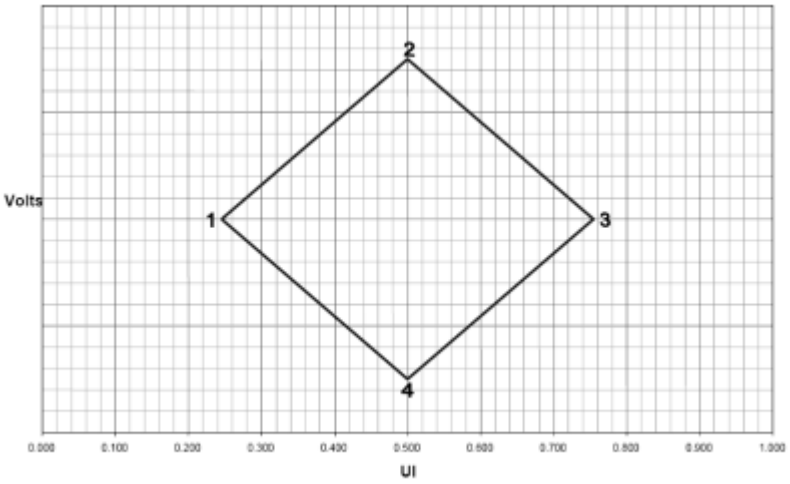


Figure 79 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001, 12230002, 12230003, 12230004 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

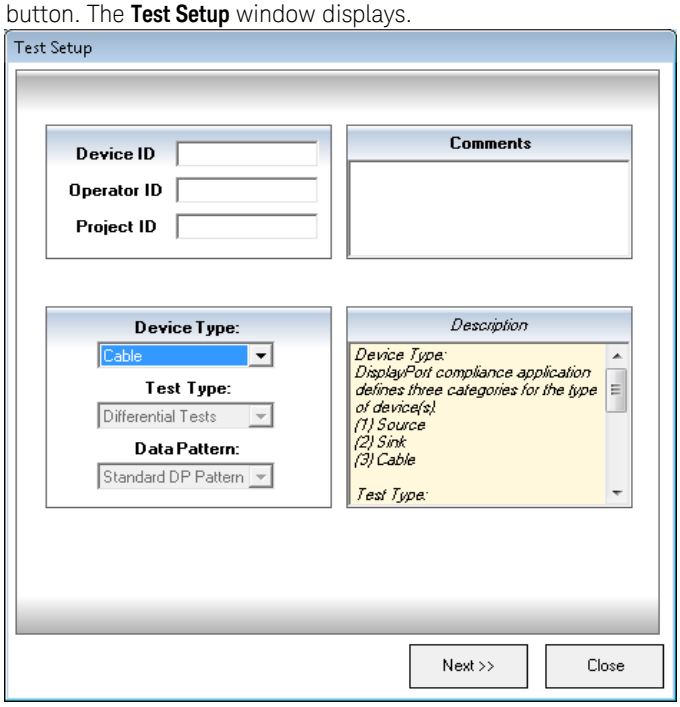
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 81

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



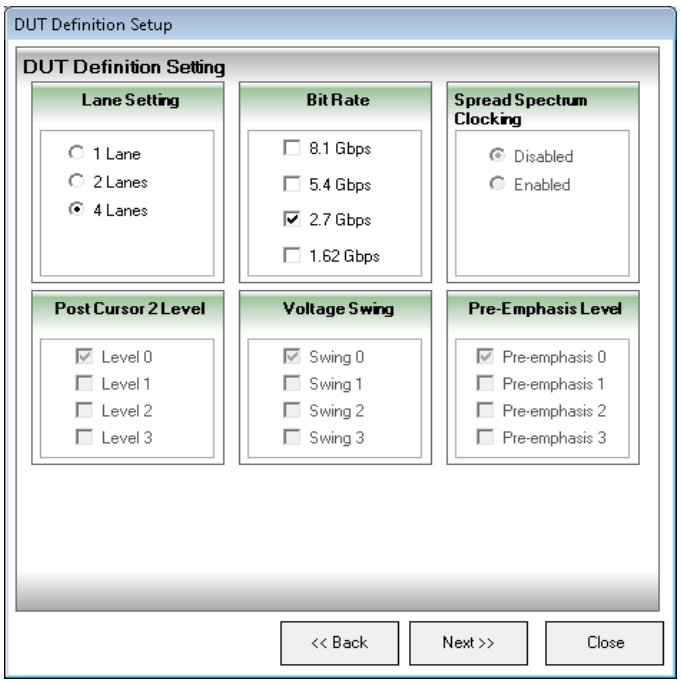
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

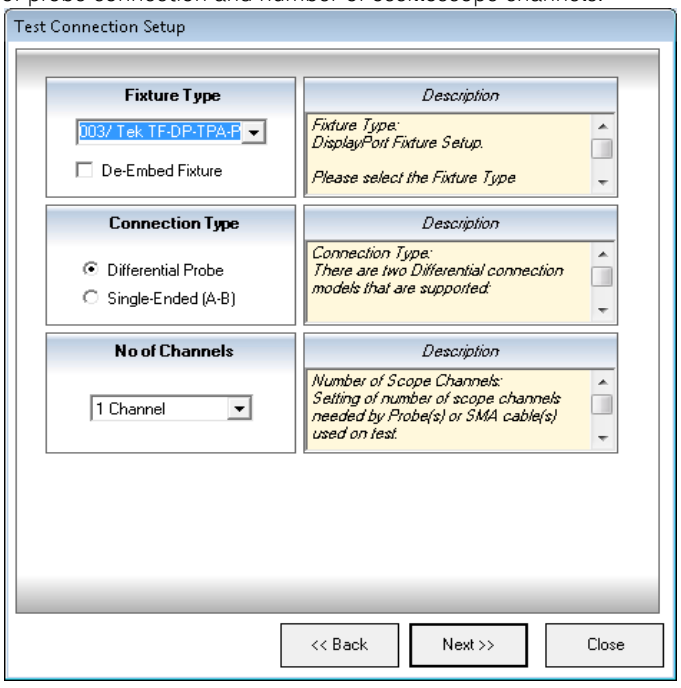
b Select **Device Type:** as **Cable**, **Test Type:** and **Data Pattern:** automatically gray out.

c Click **Next**.

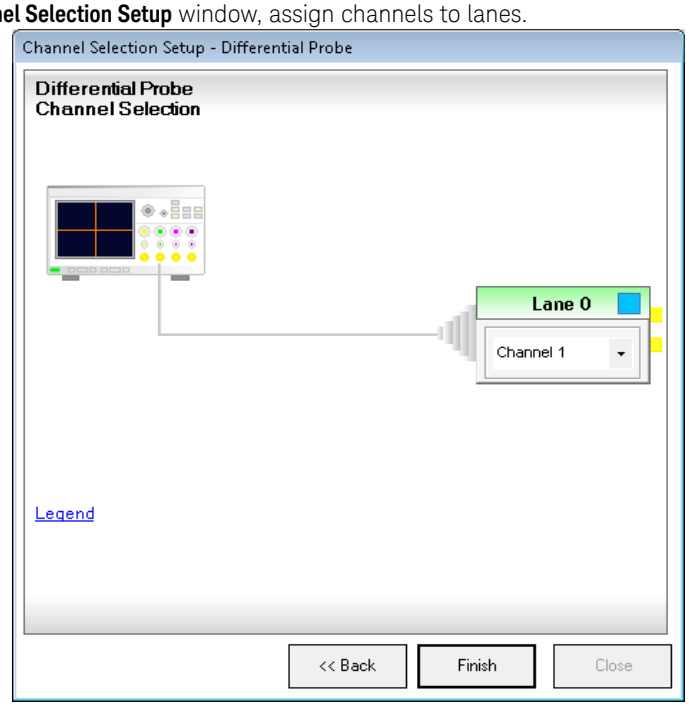
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Cable Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

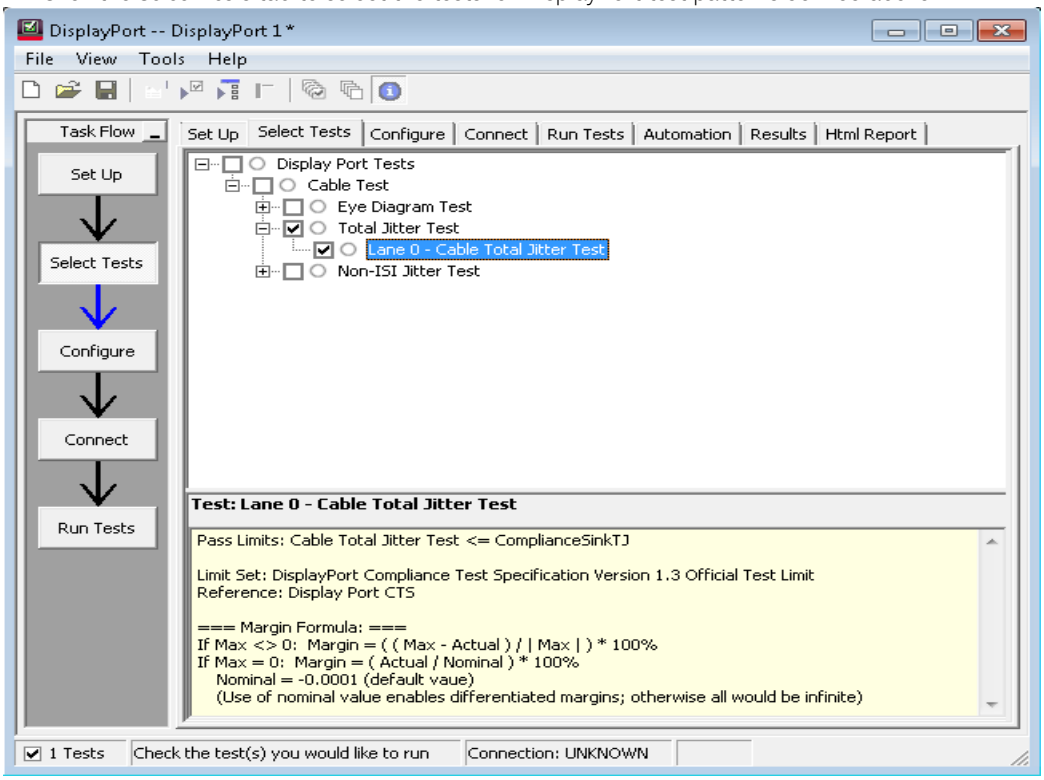


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Cable Tests" on page 436 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 83 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001, 12240002, 12240003, 12240004 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Calculate Non-ISI Jitter using the following equation:

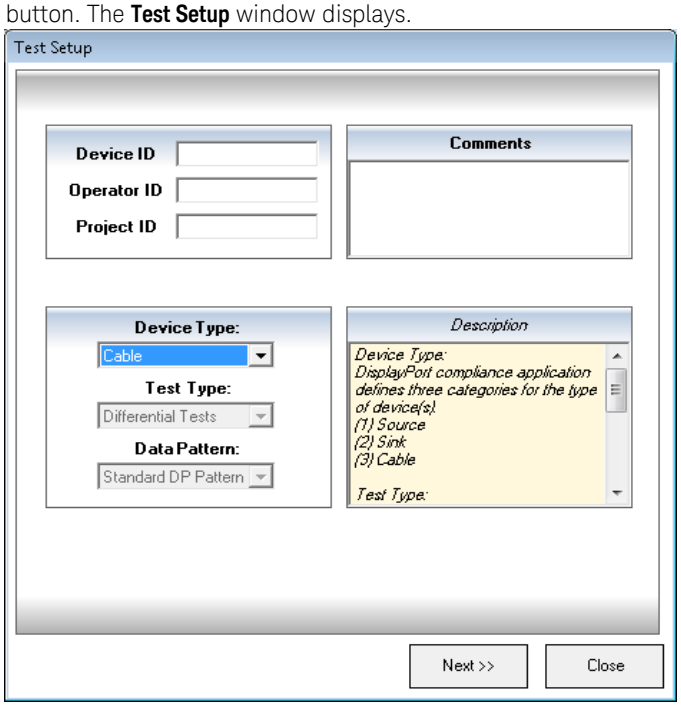
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	All test lanes supported
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 81

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



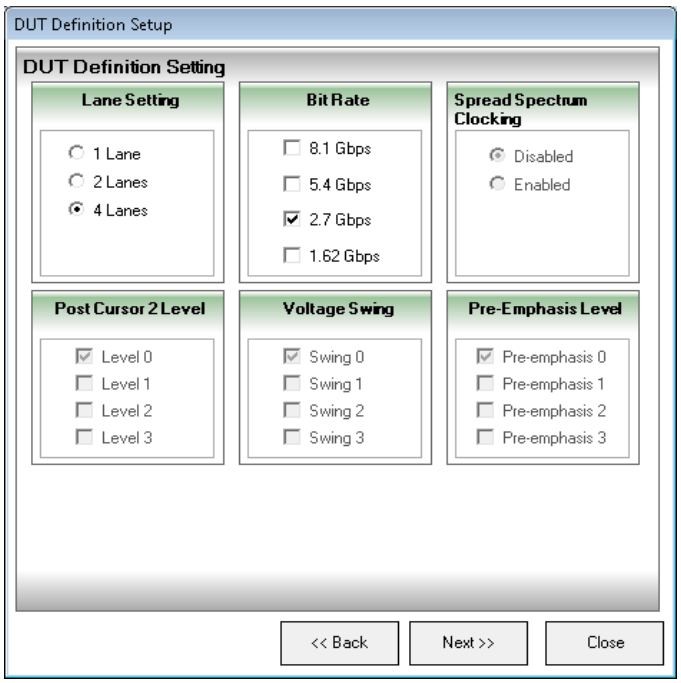
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

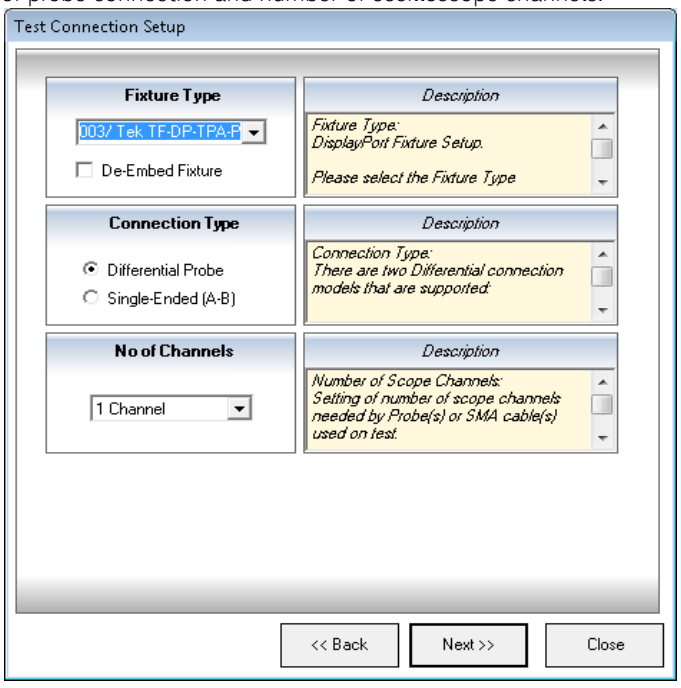
b Select **Device Type:** as **Cable**, **Test Type:** and **Data Pattern:** automatically gray out.

c Click **Next**.

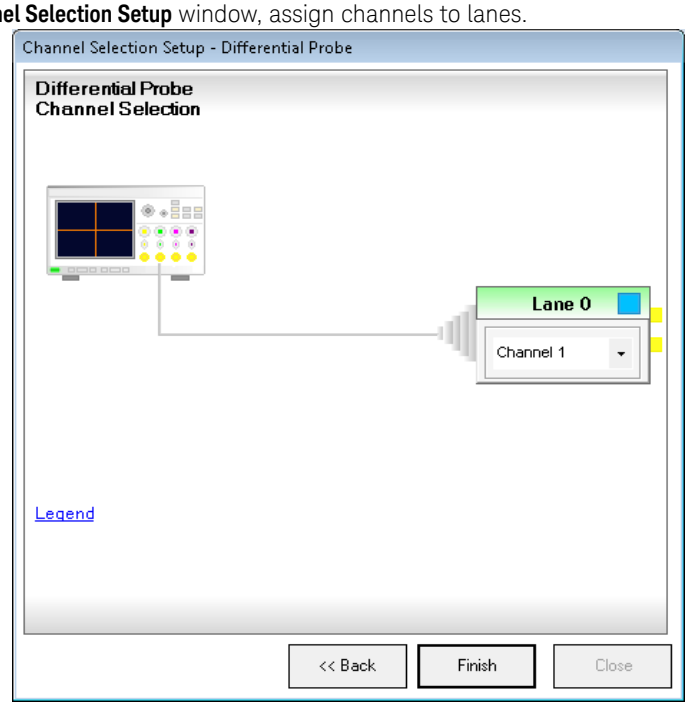
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Cable Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

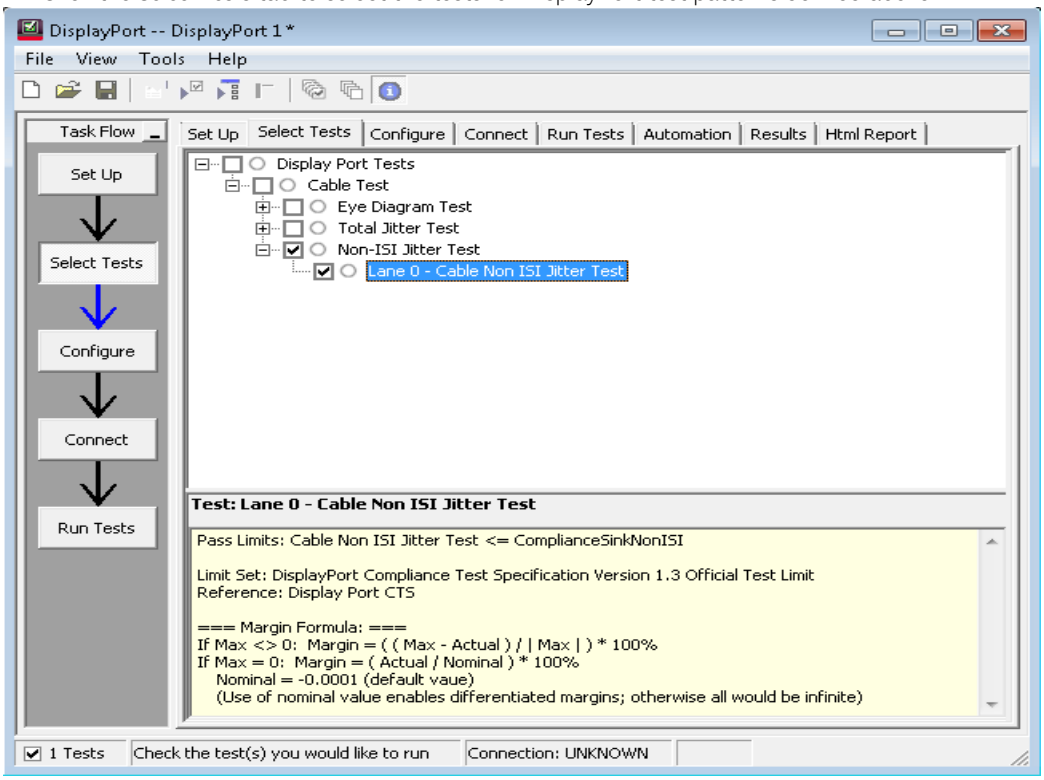


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Cable Tests" on page 436 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 84 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

12 DisplayPort 1.3 AUX Channel Tests

Overview

This section describes the normative and informative AUX Channel physical layer tests and inrush tests for compliance verification of DisplayPort1.3 source and sink.

Test Point for AUX Channel Tests

You must test the Source devices at Test Point 2 (TP2) while the Sink devices must be tested at Test Point 3 (TP3). See Figure 80.

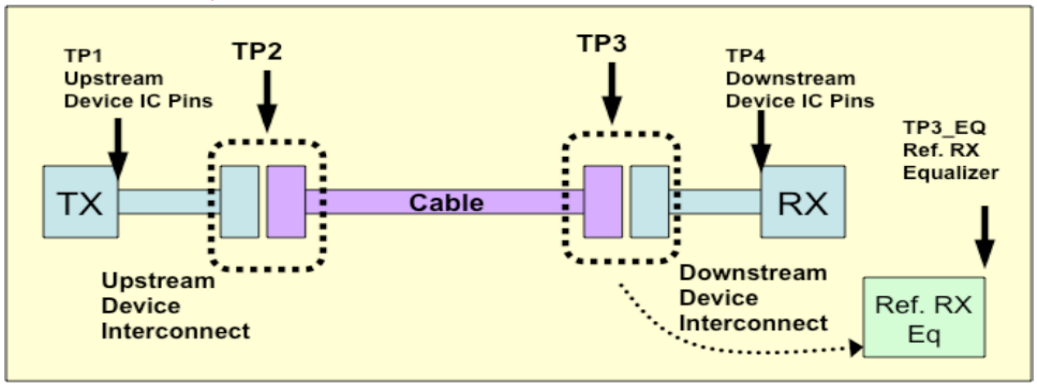


Figure 80 Test Points for DisplayPort 1.3 AUX Channel Tests

Table 85 defines the test point fixtures and instruments used for DisplayPort 1.3 AUX Channel Tests:

Table 85 Test Point Fixtures and Instruments for DisplayPort 1.3 AUX Channel Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope
Stimulus	Stimulus must be applied to the DUT to cause AUX Channel transactions to occur. This stimulus shall not be included in or affect the measurements. Reference Sink needed as stimulus for the Source DUT: ▪ Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Reference Source needed as stimulus for the Sink DUT: ▪ Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 AUX Channel Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 81).

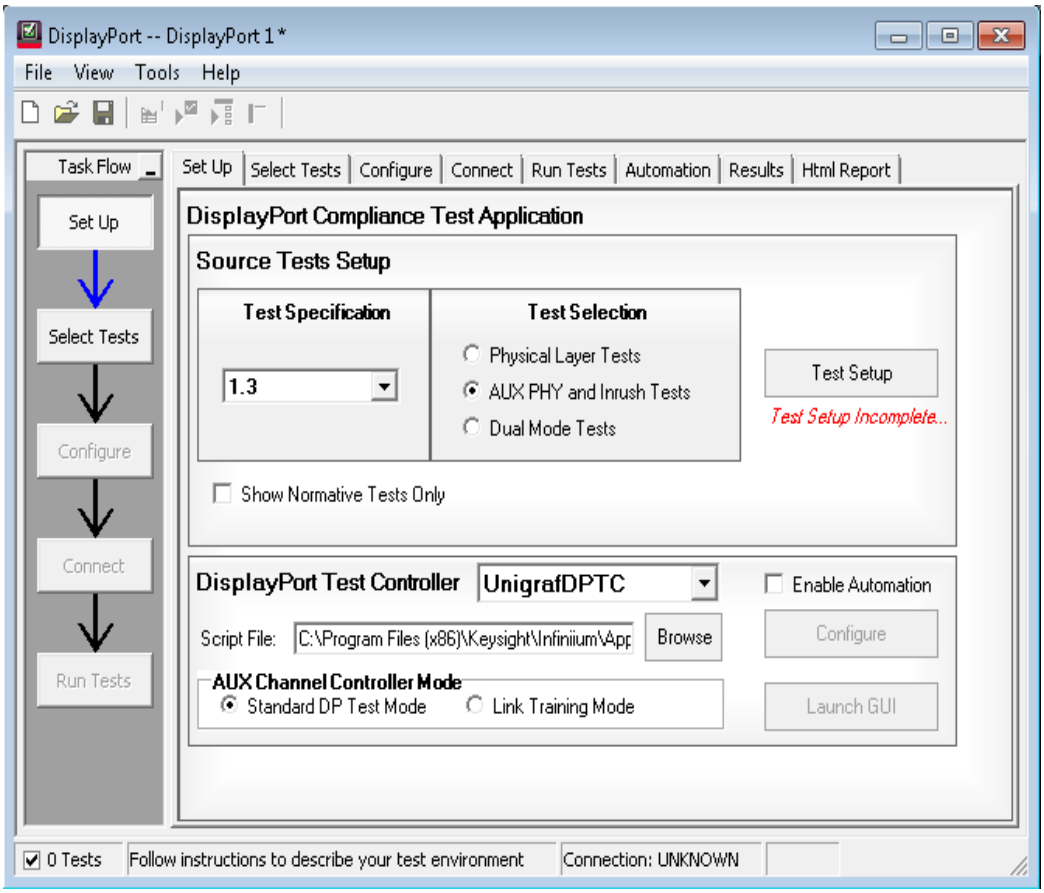


Figure 81 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.3 Standards, select **1.3** from the drop-down options in the **Test Specification** area and select **AUX PHY and Inrush Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

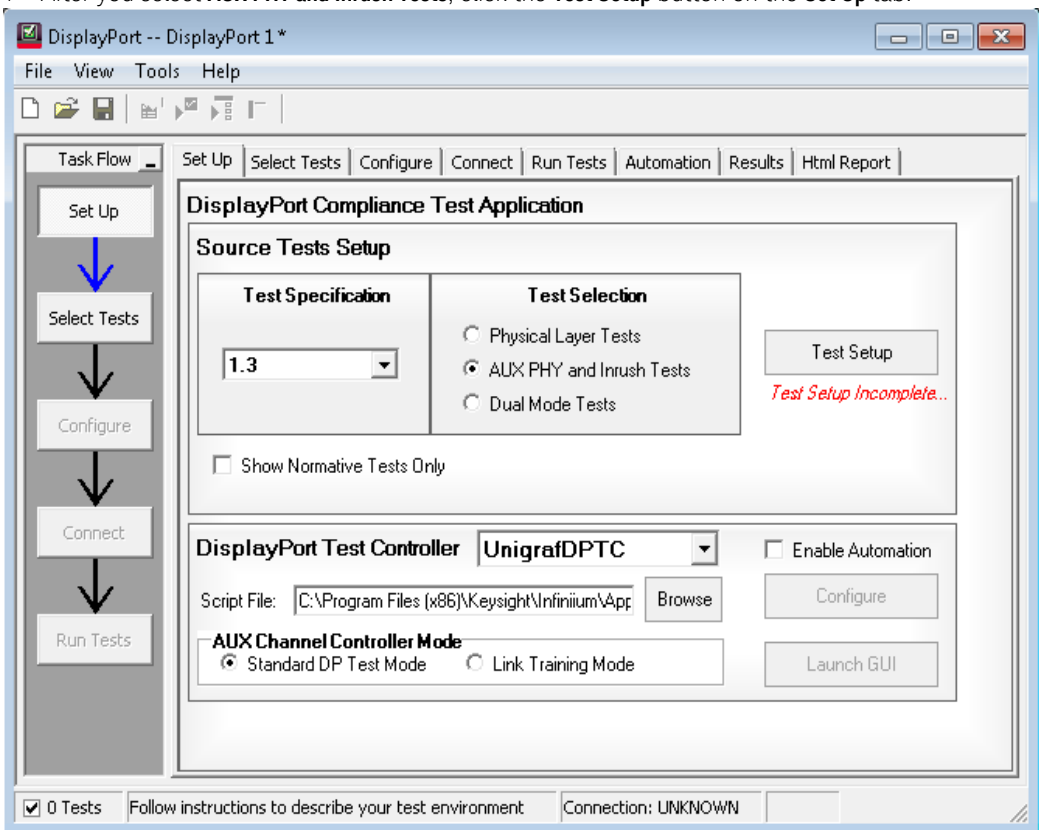
10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

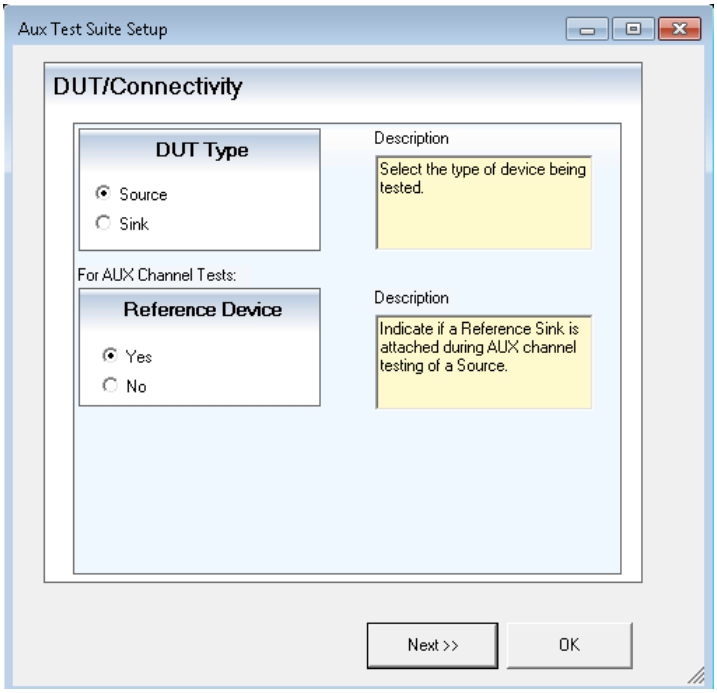
Setting Up for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

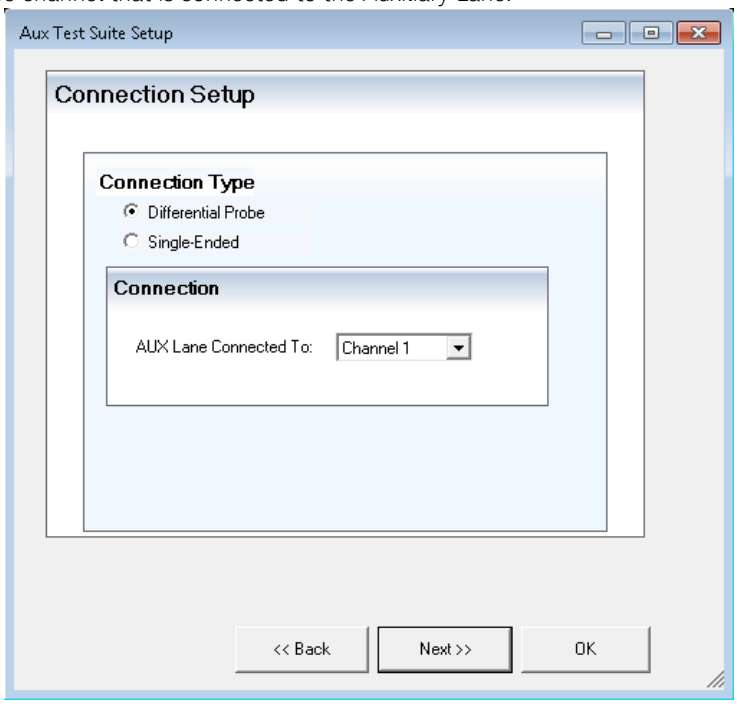
1 After you select **AUX PHY and Inrush Tests**, click the **Test Setup** button on the **Set Up** tab.



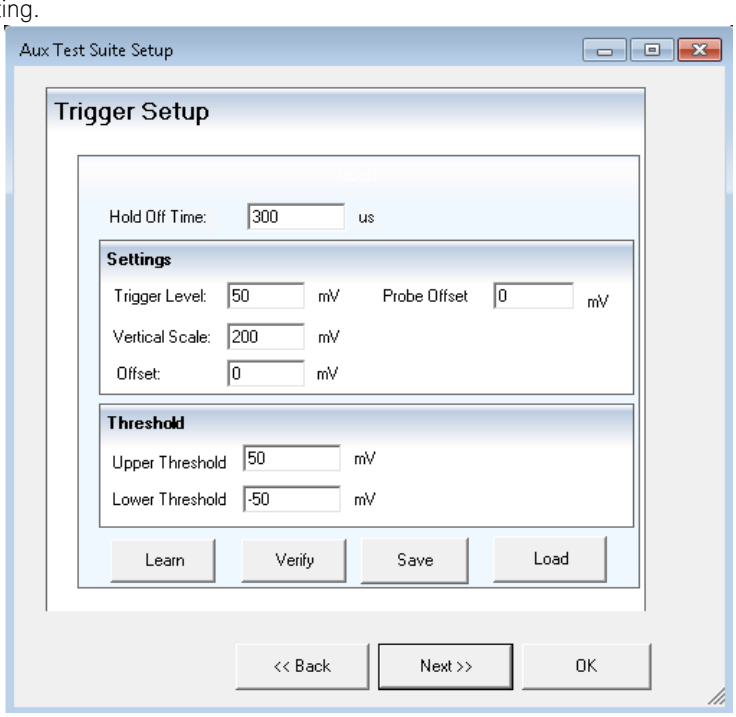
2 On the **DUT/Connectivity** page, select **Source** or **Sink** in the **DUT Type** area. In the **Reference Device** area, select **Yes** if a reference sink/source is attached to device under test during testing. Click **Next**.



3 On the **Connection Setup** page, depending on the probe connection you are using, select either **Differential Probe** or **Single-Ended** in the **Connection Type** area and in the **Connection** area, select the oscilloscope channel that is connected to the Auxiliary Lane.



4 On the **Trigger Setup** page, define the oscilloscope parameters to trigger on an Auxiliary signal during testing.



Hold Off Time – The oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each Aux transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.

Trigger Level – The AUX Channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure shows correct and incorrect trigger levels.

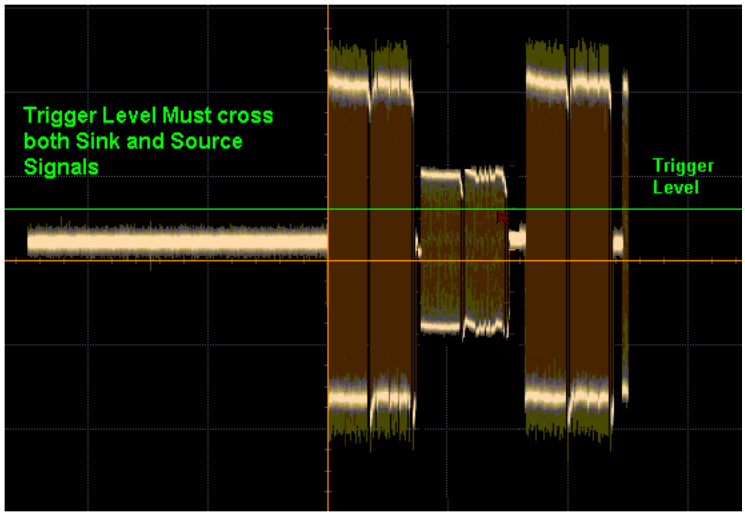


Figure 82 Correct Trigger Level

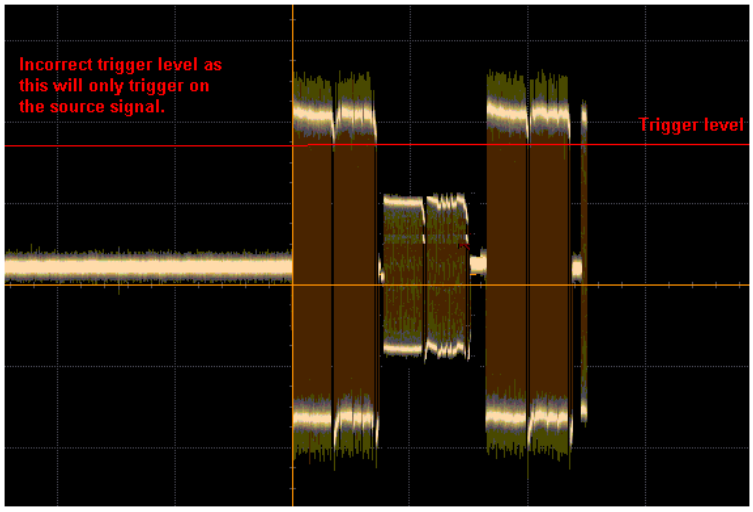


Figure 83 Incorrect Trigger Level

Vertical Scale – The oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.

Offset – Set the offset so that the center point is aligned with the center of the oscilloscope display.

Upper Threshold/Lower Threshold – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply.

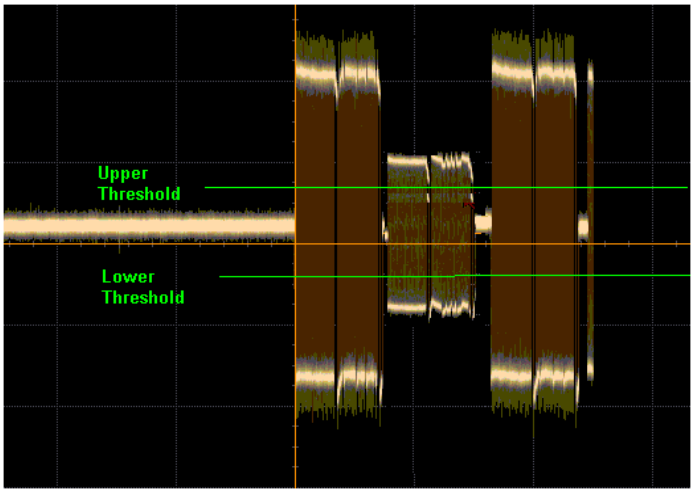


Figure 84 Correct Threshold set

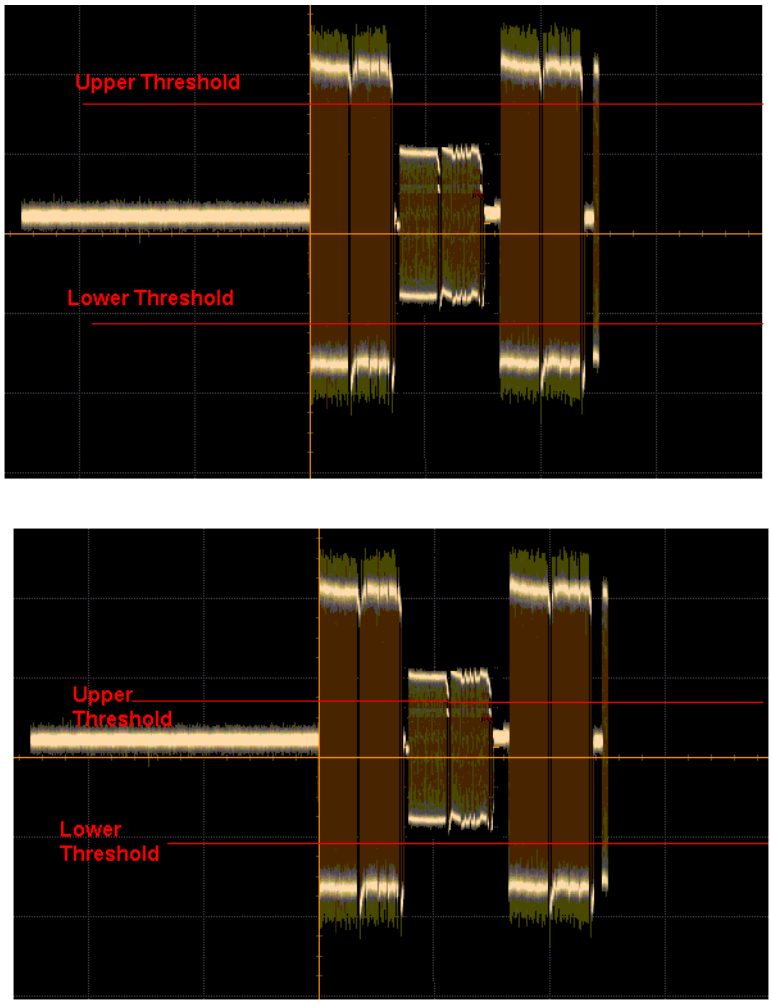


Figure 85 Wrong Thresholds set

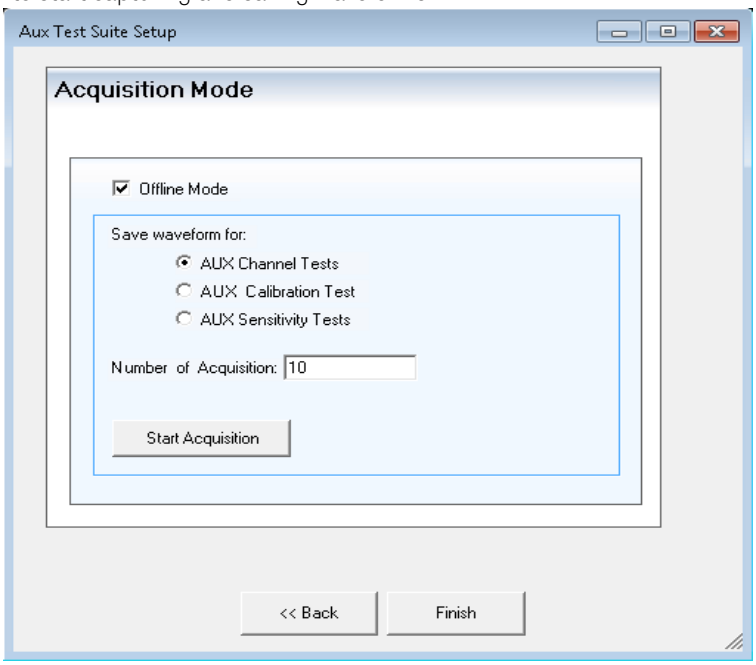
c On the Trigger Setup page, you may click the **Learn** button, which guides you through getting the trigger setup parameters. However, please note that the learning guide may not necessarily work many a times because the actual Auxiliary signals may vary for different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.

d Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.

e You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

5 On the **Acquisition Mode** page, either **Finish** the setup wizard or enable **Offline Mode**, which is de-selected, by default. Offline Mode lets you save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.

6 If you enable **Offline Mode**, define the number of waveforms to be saved. If required, click **Start Acquisition** to start capturing and saving waveforms.



7 Click **Finish** to close the setup wizard. The **Set Up** tab displays.

8 Click the **Select Tests** tab and select the AUX Channel tests you want to run.

Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

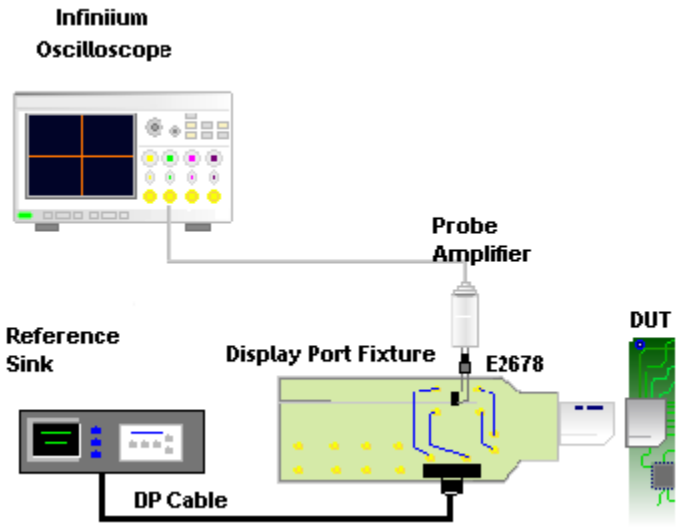


Figure 86 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

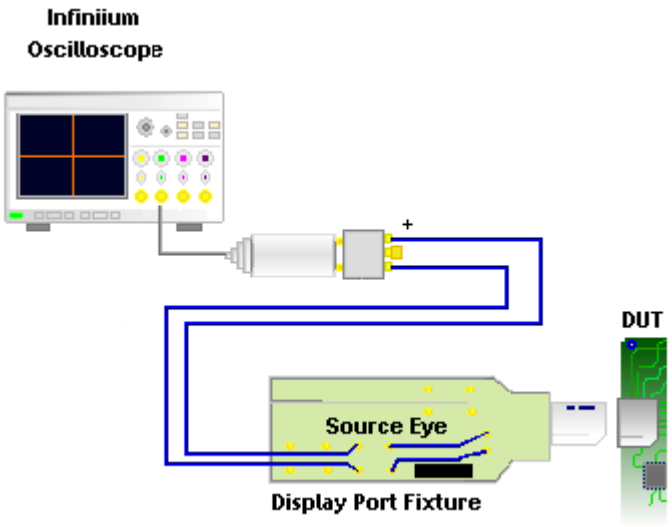


Figure 87 Sample connection diagram for source AUX channel tests without connecting to a reference sink

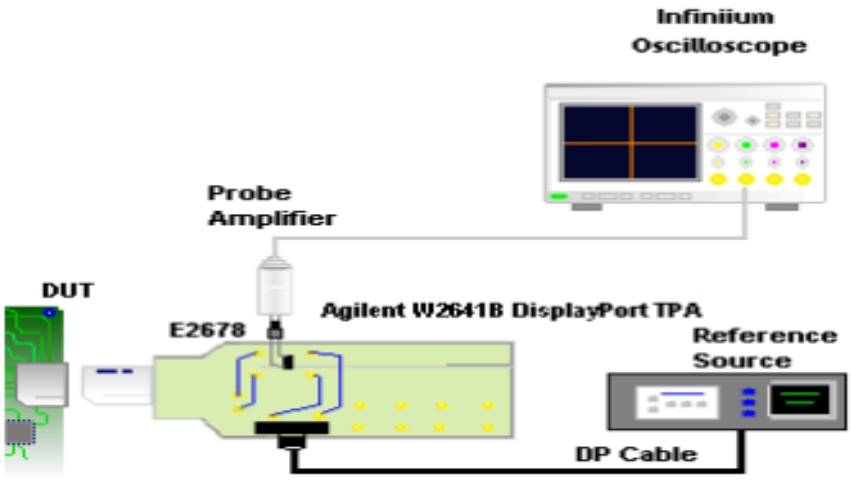


Figure 88 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

9 Check for any signal trajectories entering into the mask.

10 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 86 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

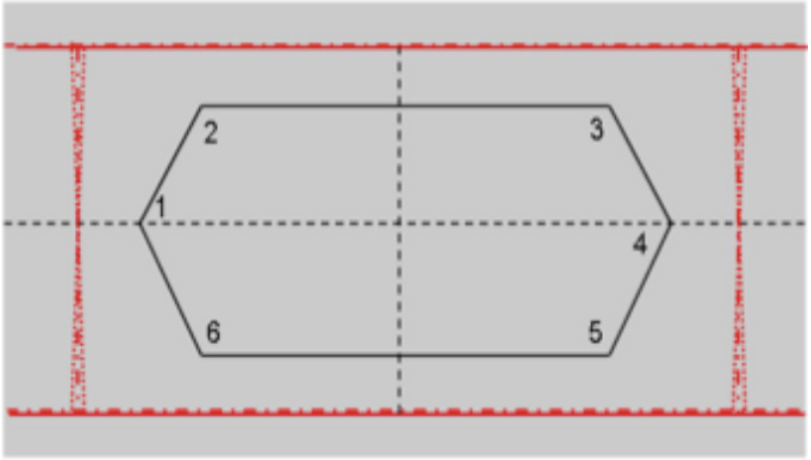


Figure 89 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.1*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.4.2.5, Figure 3-18 and Table 3-5*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1. Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
2. Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
3. Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).
4. Set up the parameter of the measurement:
   - *a* Enable measurement of all edges to obtain a statistical value of the measurement.
   - *b* Set up the measurement threshold.
   - *c* Set up the Clock Recovery.
5. Generate FUNC3 signal, which is the second differential signal of the AUX Channel.
6. Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7. Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.
8. If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:
   - *a* Set up the parameter of the Mask Test:
     - i Load the eye mask based on the settings in the Configuration Variable.
     - ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
     - iii Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.
   - *b* Check for any signal trajectories entering into the mask.
9. Report the measurement results.

PASS Condition

Table 87 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 88 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.4.2, Table 3-4*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

13 DisplayPort 1.3 Inrush Tests

Overview

This section describes the normative and informative inrush tests for compliance verification of DisplayPort1.3 source and sink (a power consumer).

Test Point

The test fixture for inrush tests implements the schematic shown in Figure 90.

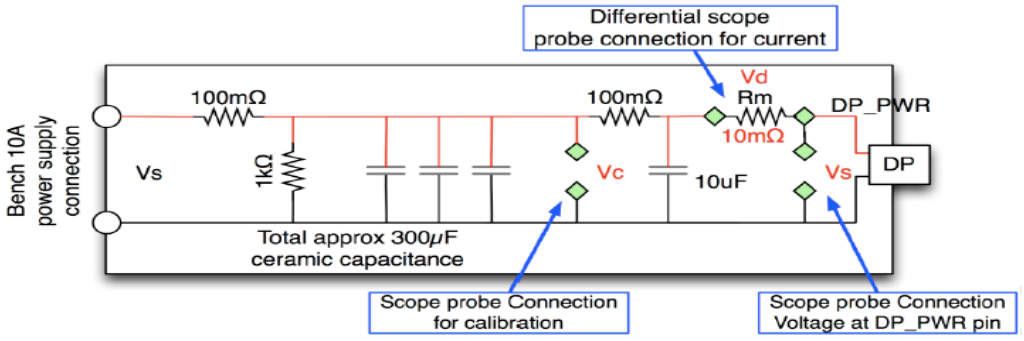


Figure 90 Schematics for testing a Power Consumer Device

The test fixture must be designed and used according to the following guidelines:

- A high gate voltage FET on the DP_PWR line is recommended to allow a fast connect capability, which allows a single connection event for testing. Without such an arrangement, multiple connections will be required to obtain a reasonable “worst-case” attachment event.
- Connection length between the power supply and the test fixture must be minimized. A maximum of four inches is recommended.
- The power supply must have enough outrush capability as to not negatively affect the test fixture’s outrush capability.
- The power supply must be run at 3.6V (3.3V + 10%) read across V_C.

Any Power Consumer test fixture must be calibrated using the Power User test fixture, as shown in Figure 90. Testing with the two fixtures combined should result in the approximate values given below. If required, the component values on the Power Consumer test fixture should be adjusted to match the expected results.

- V_C steady before connection = 3.6V
- V_C droop = ~3.1V
- Inrush Current = ~13.0A

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Inrush Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 91).

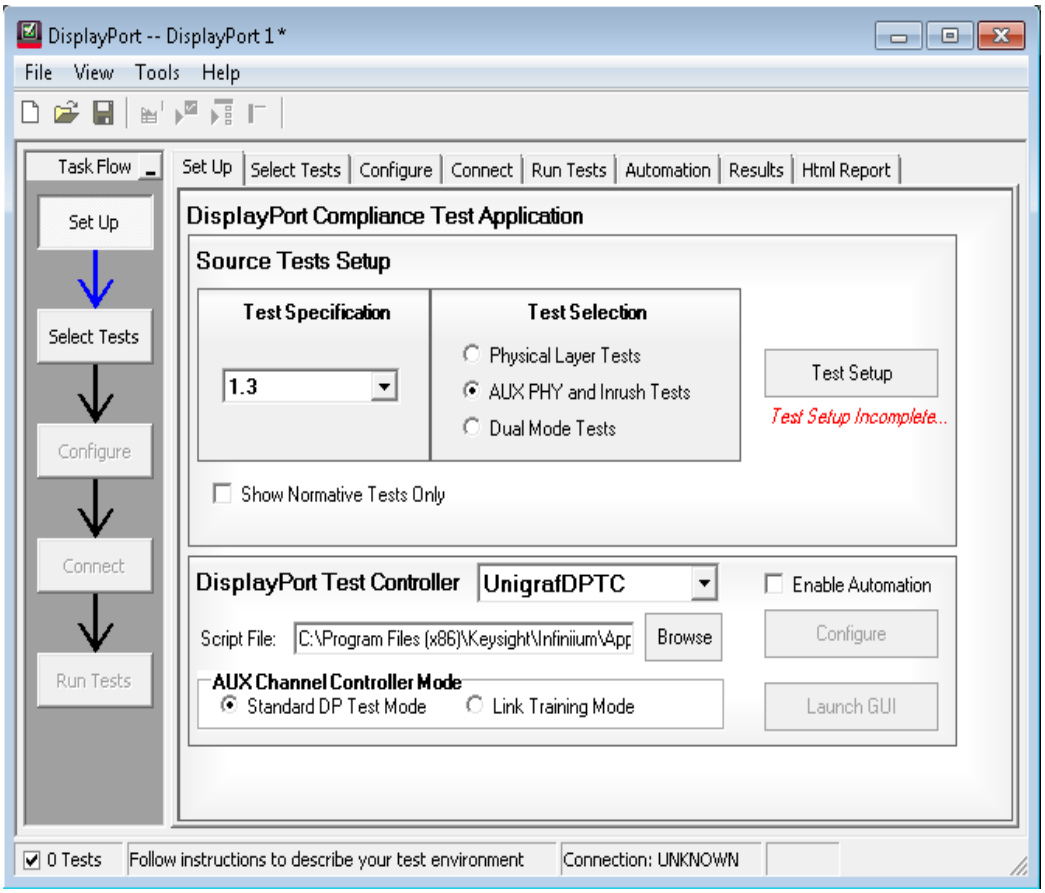


Figure 91 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.3 Standards, select **1.3** from the drop-down options in the **Test Specification** area and select **AUX PHY and Inrush Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests. Refer to "Setting Up for AUX PHY and Inrush Tests" on page 459 to know in detail how to set up the DUT for Inrush Tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	Source–TP2 Sink–TP3

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Energy $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 13.5$ Amps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.5*
- *VESA DisplayPort (DP) Standard Version 1.3, Section 3.2.3*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

14 DisplayPort 1.3 Dual Mode Tests

Overview

This section describes the normative and informative dual mode physical layer (differential and single-ended) tests for compliance verification of DisplayPort1.3 source.

Test Point

The source device for dual mode tests must be tested at Test Point 2 (TP2), as shown in Figure 92.

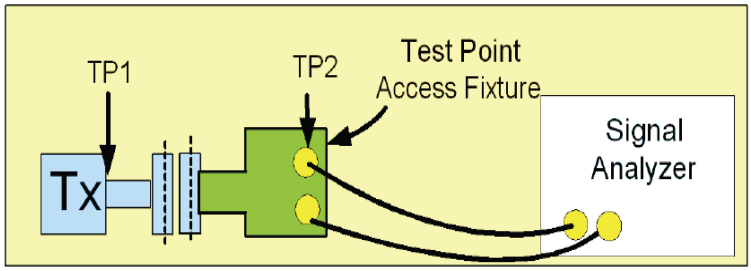


Figure 92 Test Point 2 Connection for Dual Mode Source Tests

Table 89 defines the Test Points used for Dual Mode Tests:

Table 89 Test Point 2 Connections for Dual Mode Tests

Test Requirement	Device Used
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-P* ▪ W2641B DisplayPort Test Point Access Adapter For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-P* ▪ Luxshare ICT mDP Plug (mDP-TPA-P)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort 1.3 Dual Mode Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 93).

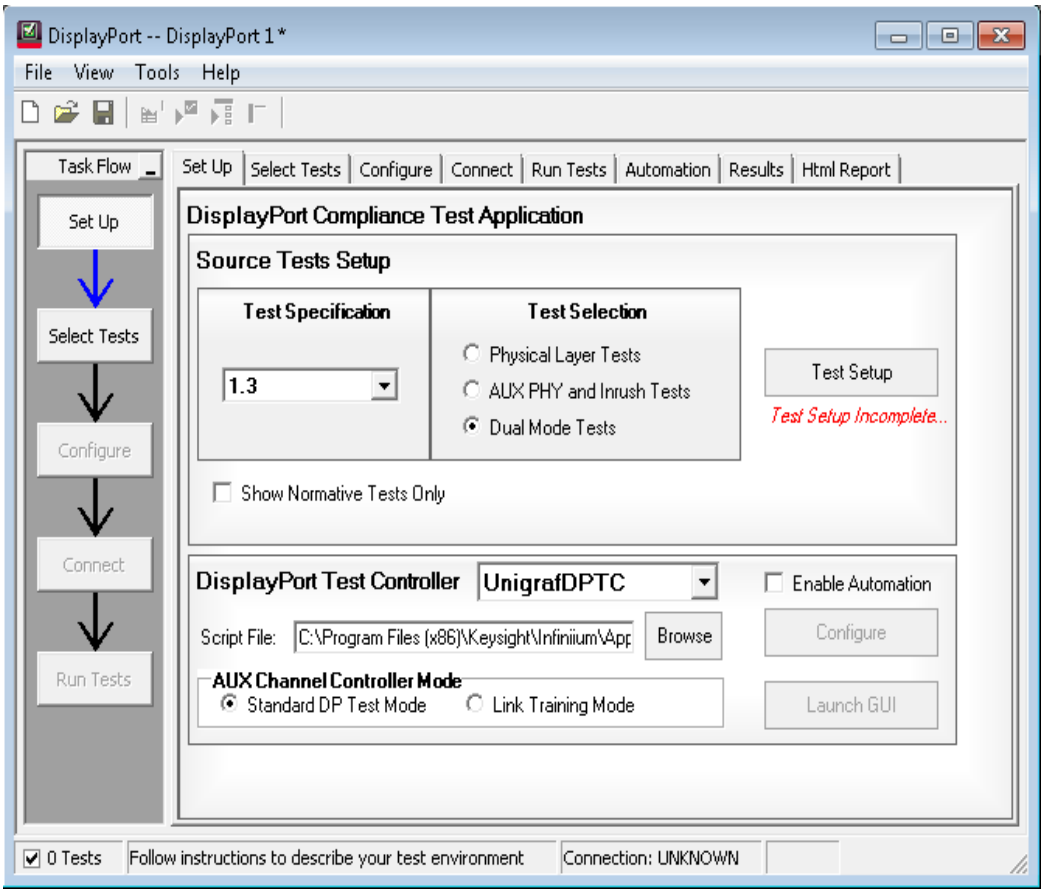


Figure 93 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with DisplayPort 1.3 Standards, select **1.3** from the drop-down options in the **Test Specification** area and select **Dual Mode Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

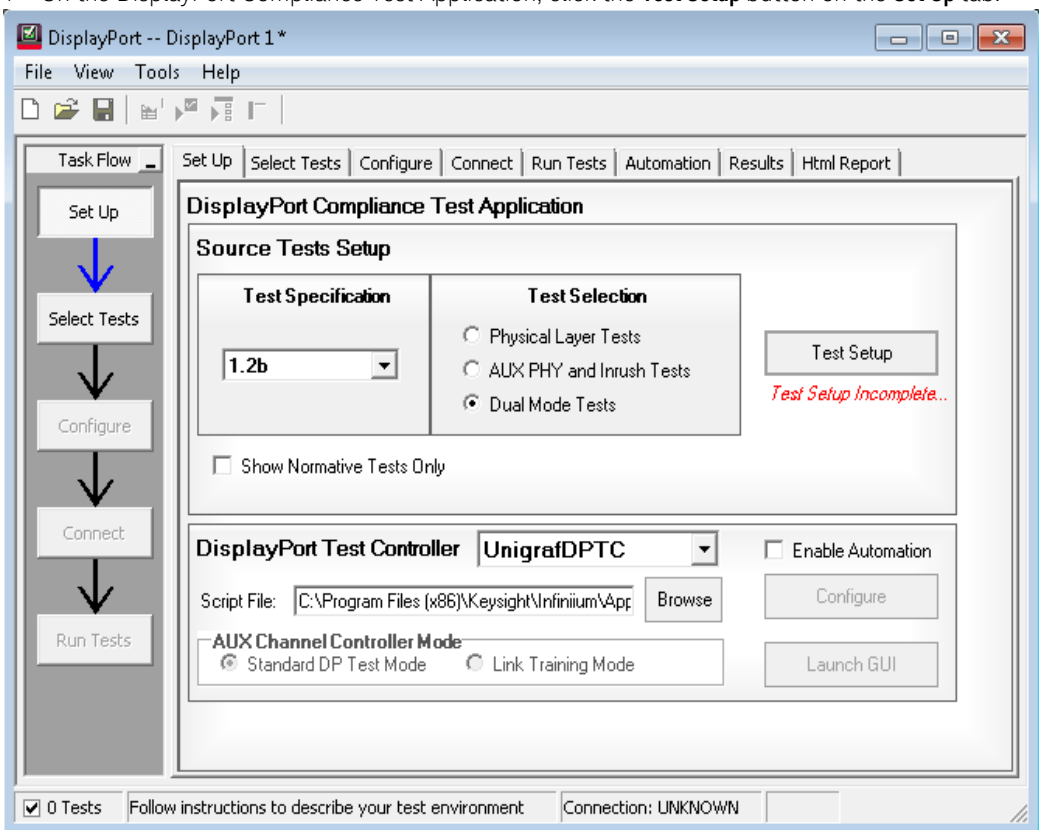
10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

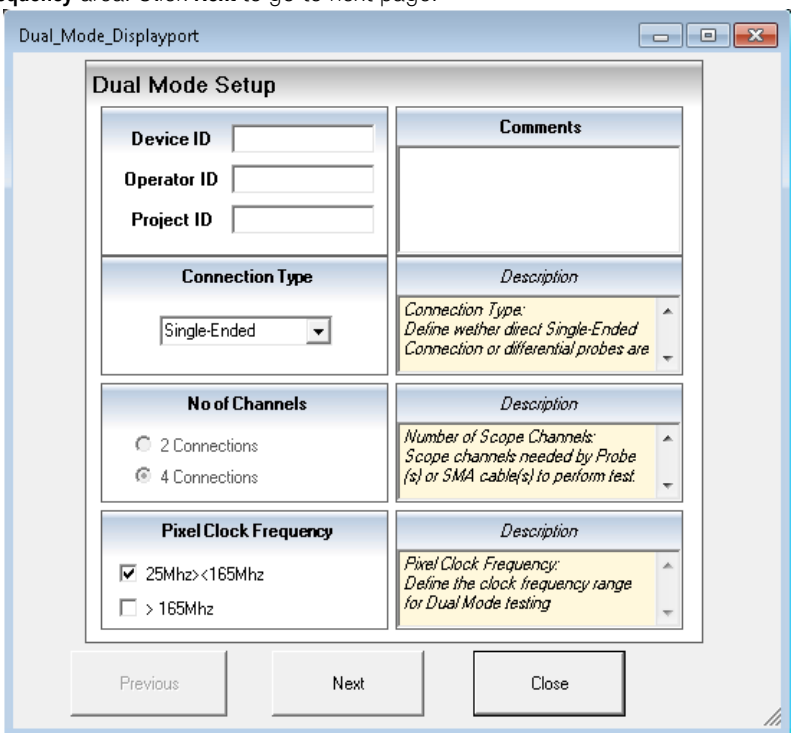
Setting Up for Dual Mode Tests

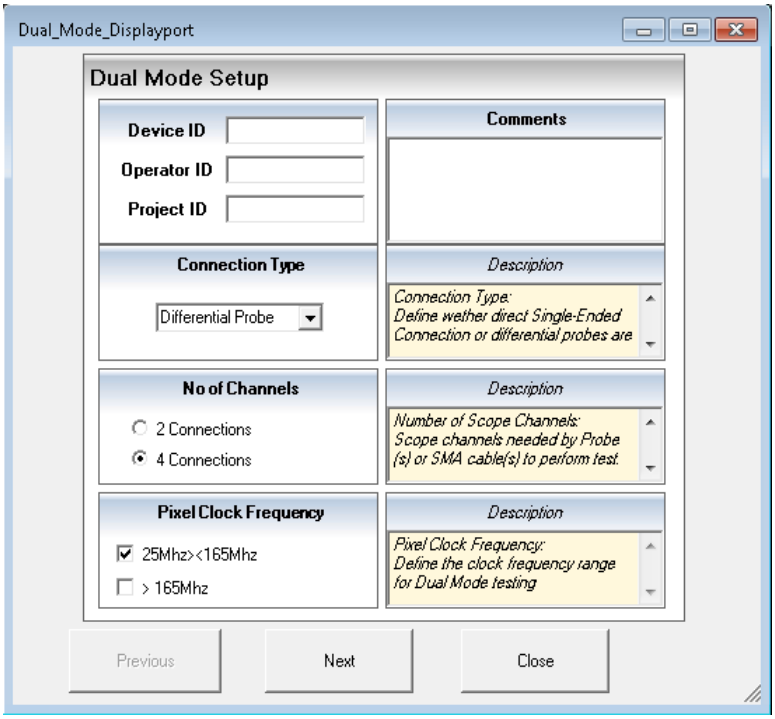
Perform the following steps before you run the Dual Mode tests on the source or sink device:

1 On the DisplayPort Compliance Test Application, click the **Test Setup** button on the **Set Up** tab.

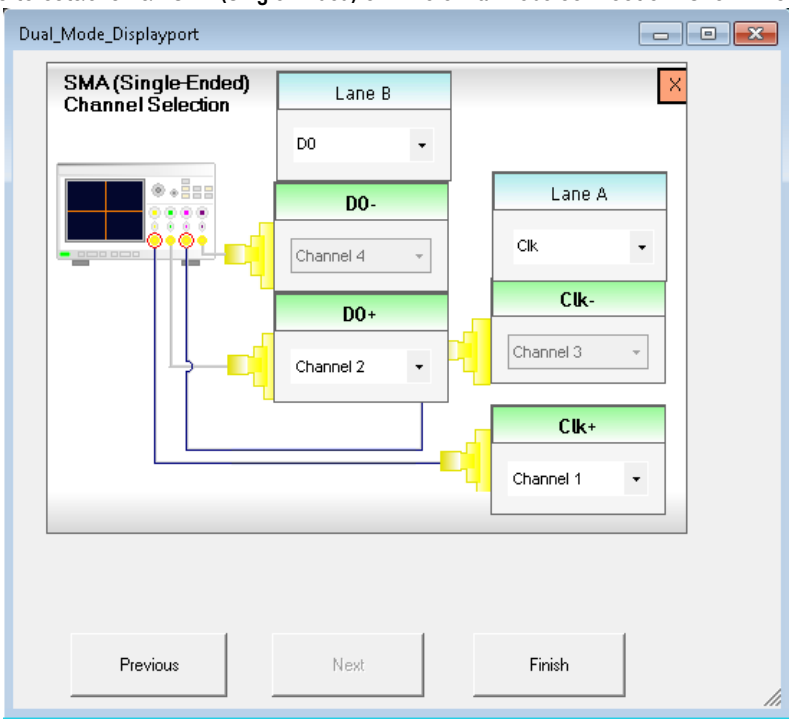


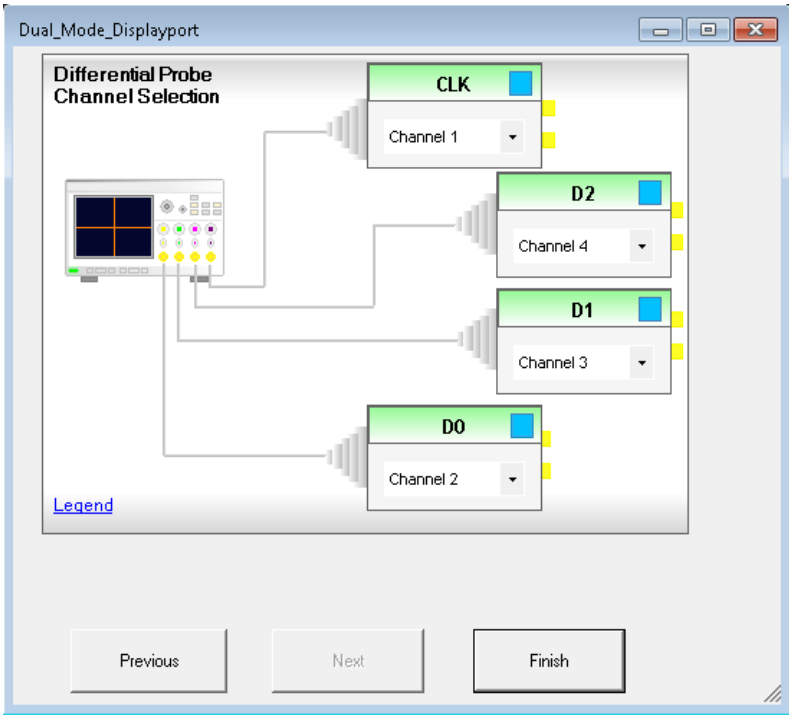
2 On the **Dual Mode Setup** page, select **Single-Ended** or **Differential Probe** from the drop-down in the **Connection Type** area. The option to select the number of oscilloscope channel connections is grayed out if you select **Single-Ended** connection type. For **Differential Probe**, you may choose either a 2-Channel or a 4-Channel setup. Select the clock frequency for Dual Mode signal in the **Pixel Clock Frequency** area. Click **Next** to go to next page.





3 On the **Channel Selection** page, you may assign the data lanes, clock lanes and oscilloscope channels to establish an **SMA (Single-Ended)** or **Differential Probe** connection. Click **Finish**.





Probing/Connection Set Up for Dual Mode Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

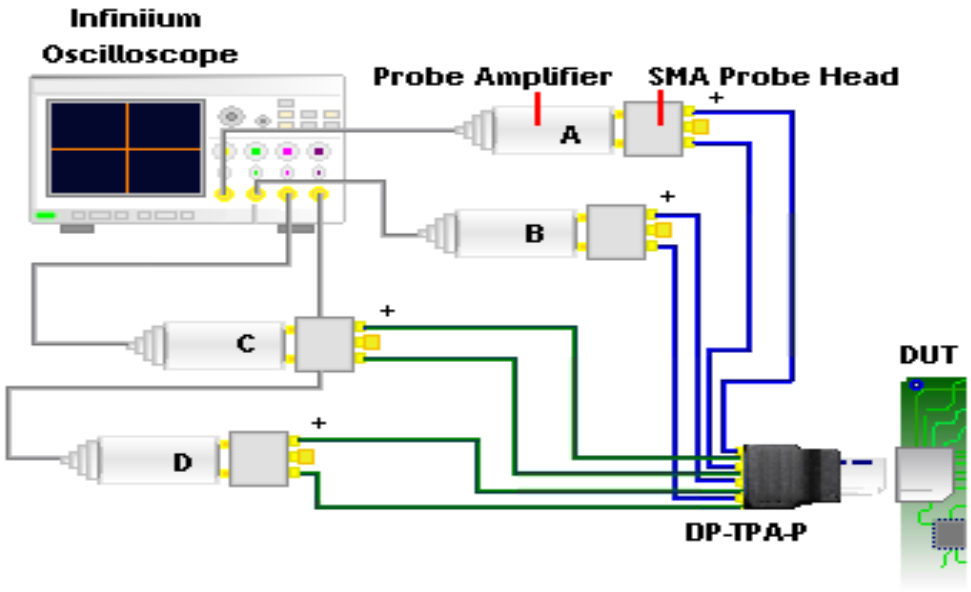


Figure 94 Connection diagram for a 4-Channel Dual Mode Test

Dual Mode TMDS Clock Duty Cycle Test

Test ID

501 – Dual Mode TMDS Clock Duty Cycle (Min)

502 – Dual Mode TMDS Clock Duty Cycle (Max)

Test Overview

The objective of the test is to confirm that the duty cycle of the TMDS Clock waveform of a Source DUT operating in dual mode does not exceed the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_CLOCK

Measurement Procedure

1 Acquire and verify the input TMDS Clock signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Scale the vertical display of the input TMDS Clock signal to optimum value.
   c Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   d Measure the Clock Frequency of the input TMDS Clock signal.
2 Generate FUNC4 signal, which is the differential signal of the TMDS Clock signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit Clock, input TMDS Clock signal).
4 Overlap the TMDS Clock signal to fold the differential signal of the TMDS Clock signal.
   a Acquire the signal until 10,000 clock periods are folded.
5 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the minimum and maximum duty cycle.
   a The minimum duty cycle is measured as the earliest crossing of the TMDS Clock signal falling edge.
   b The maximum duty cycle is measured as the latest crossing of the TMDS Clock signal falling edge.
6 Report the measurement results.

PASS Condition

PASS: 40% < TMDS_CLOCK duty cycle < 60%.

FAIL: TMDS_CLOCK duty cycle < 40% or TMDS_CLOCK duty cycle > 60%

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.18*

Expected/Observable Results

The measured duty cycle of the dual mode TMDS Clock signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode TMDS Clock Jitter Test

Test ID

For 25MHz ≤ TMDS Clock Frequency ≤ 165MHz

- 503 – Dual Mode TMDS Clock Jitter

For TMDS Clock Frequency > 165MHz

- 803 – Dual Mode TMDS Clock Jitter

Test Overview

The objective of the test is to confirm that the TMDS Clock waveform of a Source DUT operating in dual mode does not carry excessive jitter than that defined in the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_CLOCK

Measurement Procedure

1 Acquire and verify the input TMDS Clock signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Scale the vertical display of the input TMDS Clock signal to optimum value.
   c Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   d Measure the Clock Frequency of the input TMDS Clock signal.
2 Generate FUNC4 signal, which is the differential signal of the TMDS Clock signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit Clock, input TMDS Clock signal).
4 Overlap the TMDS Clock signal to fold the differential signal of the TMDS Clock signal.
   a Acquire the signal until 400,000 clock periods are folded.
5 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.
6 Report the measurement results.

PASS Condition

For 25MHz ≤ TMDS Clock Frequency ≤ 165MHz

- PASS: Measured TMDS Clock Jitter ≤ 0.20 Tbit and Data Jitter ≤ 0.25 Tbit

For 165MHz < TMDS Clock Frequency ≤ 300MHz

- PASS: Measured TMDS Clock Jitter ≤ 120 ps and Data Jitter ≤ 150 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.18*
- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured jitter of the dual mode TMDS Clock signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Eye Diagram Test

Test ID

601, 602, 603 – Dual Mode Eye Diagram Testing

Test Overview

The objective of the test is to evaluate the waveform ensuring that the timing variables and amplitude trajectories of a Source DUT operating in dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit First Order PLL, input TMDS Clock signal).
3 Fold the differential signal of the data signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
4 Set up the waveform histogram on the data signal eye diagram to measure the left edge and right edge.
5 Set up the parameter of the Mask Test.
   a Load the Eye mask.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Run the Eye mask until the 400,000 UI are folded.
6 Check for any signal trajectories entering into the mask.
7 Measure the jitter of the eye diagram using the histogram.
8 Measure the eye height of the eye diagram using the histogram.
9 Measure the peak-to-peak voltage at 0.5UI of the eye diagram using the histogram.

10 Overlap the TMDS Clock Signal to fold the differential signal of the data signal.

a Acquire the signal until 400,000 clock period are folded.

11 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.

12 Report the measurement results.

PASS Condition

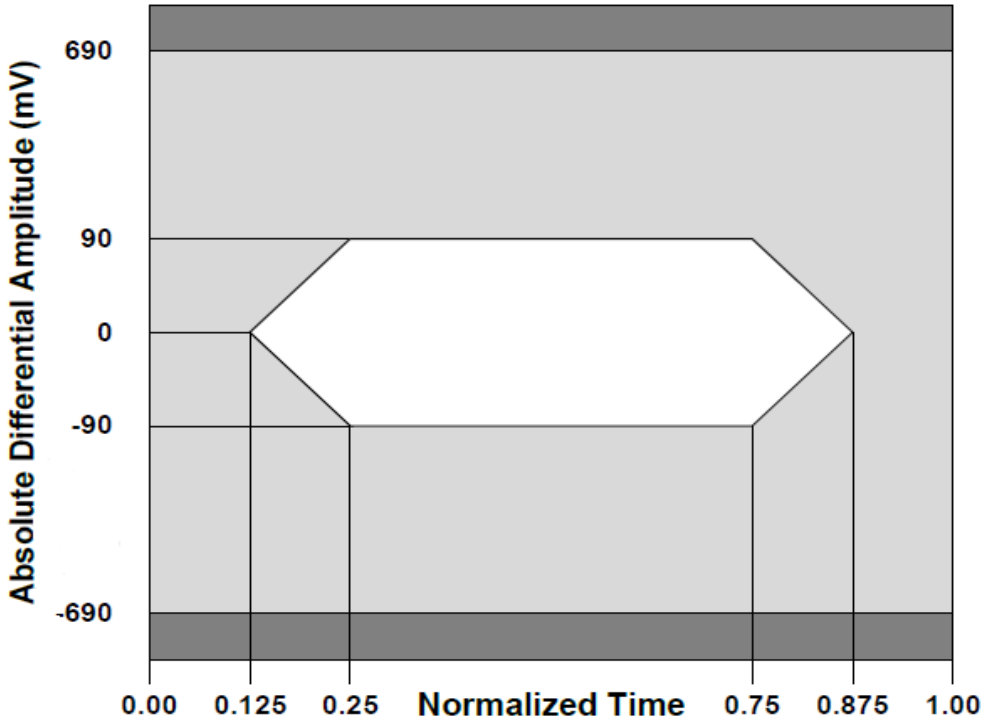
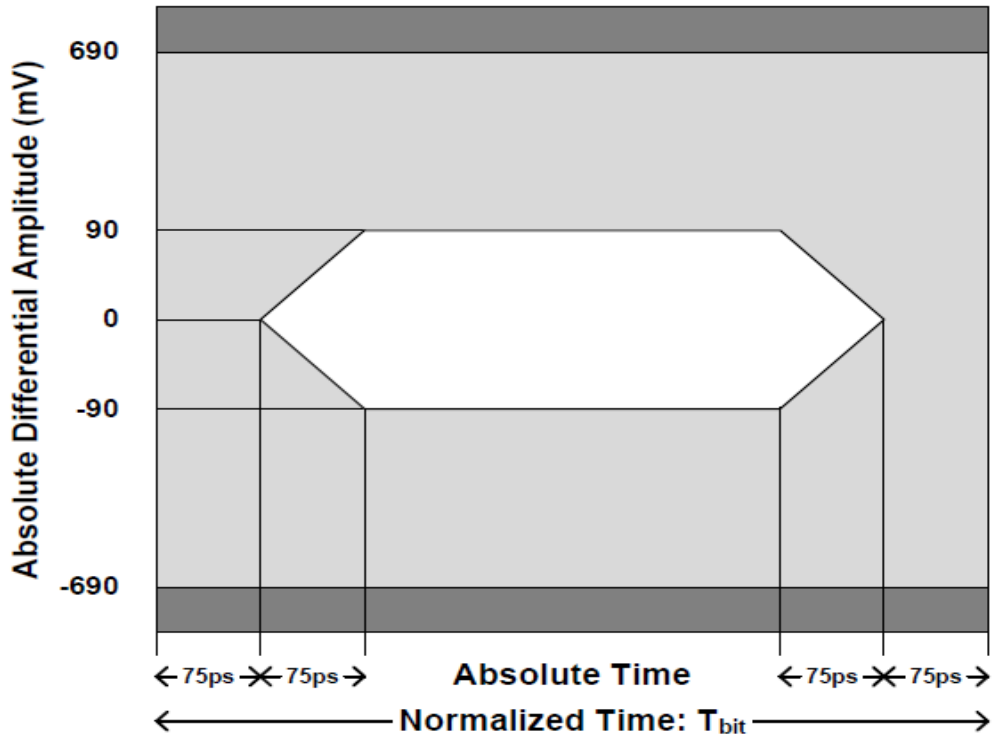


Figure 95 TMDS Data EYE Mask for TMDS Clock Frequencies from 25MHz to 165MHz



TMDS Data EYE Mask for TMDS Clock Frequencies above 165MHz

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.19*
- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2, Figure 3-10* (for 25MHz < TMDS Clock Frequency < 165MHz) and *Figure 3-11* (for TMDS Clock Frequency > 165MHz)

Expected/Observable Results

The measured eye diagram for the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Dual Mode Data Jitter Test

Test ID

For 25MHz ≤ TMDS Clock Frequency ≤ 165MHz

- 611, 612, 613 – Dual Mode Data Jitter

For TMDS Clock Frequency > 165MHz

- 911, 912, 913 – Dual Mode Data Jitter

Test Overview

The objective of the test is to confirm that the data waveform of a Source DUT operating in dual mode does not carry excessive jitter than that defined in the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit First Order PLL, input TMDS Clock signal).
3 Fold the differential signal of the data signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
4 Set up the waveform histogram on the data signal eye diagram to measure the left edge and right edge.
5 Set up the parameter of the Mask Test.
   a Load the Eye mask.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Run the Eye mask until the 400,000 UI are folded.
6 Check for any signal trajectories entering into the mask.
7 Measure the jitter of the eye diagram using the histogram.

8 Measure the eye height of the eye diagram using the histogram.

9 Measure the peak-to-peak voltage at 0.5UI of the eye diagram using the histogram.

10 Overlap the TMDS Clock Signal to fold the differential signal of the data signal.

a Acquire the signal until 400,000 clock period are folded.

11 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.

12 Report the measurement results.

PASS Condition

For 25MHz $\leq$ TMDS Clock Frequency $\leq$ 165MHz

- PASS: Measured TMDS Clock Jitter $\leq$ 0.20 Tbit and Data Jitter $\leq$ 0.25 Tbit

For 165MHz < TMDS Clock Frequency $\leq$ 300MHz

- PASS: Measured TMDS Clock Jitter $\leq$ 120 ps and Data Jitter $\leq$ 150 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.19*
- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured jitter of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Data Peak-Peak Differential Voltage Test

Test ID

811, 812, 813 – Dual Mode Peak-Peak Differential Voltage (Min)

821, 822, 823 – Dual Mode Peak-Peak Differential Voltage (Max)

Test Overview

The objective of the test is to evaluate and confirm that the data waveform ensuring that the timing variables and amplitude trajectories of a Source DUT operating in a dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input data signal.
   c Scale the vertical display of the input TMDS Clock signal to optimum value.
   d Scale the vertical display of the input data signal to optimum value.
   e Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   f Measure V_{TOP} and V_{BASE} of the input data signal.
   g Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery (Explicit First Order PLL, input TMDS Clock signal).
3 Fold the differential signal of the data signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
4 Set up the waveform histogram on the data signal eye diagram to measure the left edge and right edge.
5 Set up the parameter of the Mask Test.
   a Load the Eye mask.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.
   c Run the Eye mask until the 400,000 UI are folded.
6 Check for any signal trajectories entering into the mask.
7 Measure the jitter of the eye diagram using the histogram.
8 Measure the eye height of the eye diagram using the histogram.

9 Measure the peak-to-peak voltage at 0.5UI of the eye diagram using the histogram.

10 Overlap the TMDS Clock Signal to fold the differential signal of the data signal.

a Acquire the signal until 400,000 clock period are folded.

11 Set up the waveform histogram on the differential signal of the TMDS Clock signal to measure the total jitter of the TMDS Clock signal.

12 Report the measurement results.

PASS Condition

For all TMDS Clock Frequencies:

- Minimum Peak-Peak Differential Voltage: 180mV
- Maximum Peak-Peak Differential Voltage: 1380mV

Test References

See:

- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured peak-peak differential voltage of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Inter-Pair Skew Test

Test ID

711 – D0/D1 - Dual Mode Inter Pair Skew Test

712 – D0/D2 - Dual Mode Inter Pair Skew Test

713 – D1/D2 - Dual Mode Inter Pair Skew Test

Test Overview

The objective of the test is to evaluate and confirm that the skew or time delay between differential data lane of a Source DUT operating in a dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   a Verify the trigger and the amplitude of the input TMDS Clock signal.
   b Verify the trigger and the amplitude of the input Lane A data signal.
   c Verify the trigger and the amplitude of the input Lane B data signal.
   d Scale the vertical display of the input TMDS Clock signal to optimum value.
   e Scale the vertical display of the input Lane A data signal to optimum value.
   f Scale the vertical display of the input Lane B data signal to optimum value.
   g Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   h Measure V_{TOP} and V_{BASE} of the input Lane A data signal.
   i Measure V_{TOP} and V_{BASE} of the input Lane B data signal.
   j Measure the Clock Frequency of the input TMDS Clock signal.
2 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain the statistical values of the measurement.
   b Set up the measurement threshold.
3 Set up the parameter of the Inter Pair Skew measurement.
   a Set up two display grids such that each grid displays one test lane data signal.
   b Set up the measurement threshold of each test lane data signal on the Transition Voltage = 0V.
   c Decode the data signal for each test lane.
   d Search the desired pattern from the decoded data signal.

e Measure the time difference between the corresponding edges of both the test lanes using the equation:

$$T_{Transition\_LaneA} - T_{Transition\_LaneB}$$

f Repeat the previous step until you measure 100 edges.

g Calculate the Inter Pair Skew using the equation:

$$\text{Inter Pair Skew} = \{1/\text{Number of Edges}\} \sum |T_{Transition\_LaneA} - T_{Transition\_LaneB}|$$

4 Report the measurement results.

PASS Condition

For all TMDS Clock Frequencies, Inter-Pair Skew $\leq$ 976 ps

Test References

See:

- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured inter pair skew of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Dual Mode Intra-Pair Skew Test

Test ID

701, 702, 703 – Dual Mode Intra Pair Skew Test

Test Overview

The objective of the test is to evaluate and confirm that the skew or time delay between the respective sides of the differential data lane of a Source DUT operating in a dual mode meets the specification requirements.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Clock Rate	Maximum TMDS Clock Rate supported by the DUT
Test Lane	TMDS_DATA0, TMDS_DATA1, TMDS_DATA2

Measurement Procedure

1 Acquire and verify the input TMDS Clock and data signal:
   - *a* Verify the trigger and the amplitude of the input TMDS Clock signal.
   - *b* Verify the trigger and the amplitude of the input data signal.
   - *c* Scale the vertical display of the input TMDS Clock signal to optimum value.
   - *d* Scale the vertical display of the input data signal to optimum value.
   - *e* Measure V_{TOP} and V_{BASE} of the input TMDS Clock signal.
   - *f* Measure V_{TOP} and V_{BASE} of the input data signal.
   - *g* Measure the Clock Frequency of the input TMDS Clock signal.

2 Set up the parameter of the measurement:
   - *a* Enable measurement of all edges to obtain the statistical values of the measurement.
   - *b* Set up the measurement threshold.

3 Set up the parameter to perform High Level Voltage (V_{High}) and Low Level Voltage (V_{Low}) for each single-ended data signal:
   - *a* Scale the vertical display of the single-ended input data signal to optimum value.
   - *b* Acquire the signal for 100 waveforms.
   - *c* Find V_{High} by measuring the average voltage at 0.6UI to 0.75UI of the High level.
   - *d* Find V_{Low} by measuring the average voltage at 0.6UI to 0.75UI of the Low level.
   - *e* Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{High} + V_{Low})/2$$

4 Set up the parameter of the Intra Pair Skew measurement.

a Set up measurement threshold od each single-ended data signal based on the Transition Voltage measured.

b Set up InfiniiScan to trigger on the desired pattern.

c Set up delta time measurement to measure the time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge using the equation:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

d Set up delta time measurement to measure the time difference between the falling edge of the data true signal (D+) and the complement's (D-) falling edge using the equation:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

e Acquire the signal until you measure 100 edges.

f Calculate the Intra Pair Skew using the equation:

$$\text{Intra Pair Skew} = \{1/\text{Number of Edges}\} \sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})]/2\}$$

5 Report the measurement results.

PASS Condition

For all TMDS Clock Frequencies, Intra-Pair Skew $\leq$ 60 ps

Test References

See:

- *VESA DisplayPort Dual-Mode Standard Version 1.1, Section 3.6.2*

Expected/Observable Results

The measured intra pair skew of the dual mode data signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

15 MyDP 1.0 Source Tests

Overview

This section describes the normative and informative main link physical layer tests for compliance verification of Mobility DisplayPort (MyDP) sources.

Test Point Definition for MyDP Tests

Five different test points are identified for the physical layer measurement. See Figure 96.

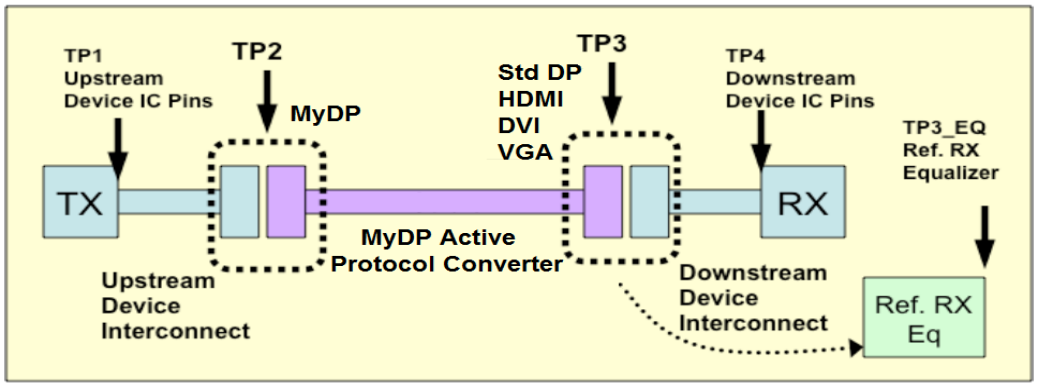


Figure 96 Test Points in a DisplayPort InterConnect System

Table 90 defines the Test Points used for MyDP 1.0 Tests:

Table 90 Test Points for DisplayPort Tests

Test Point	Description
TP1	At the pins of the Transmitter Device
TP2	At the test interface on a test access fixture as close as possible to the DP mated connection to a Source device
TP3	At the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device
TP3_EQ	At TP3, when a defined cable model with equalizer is applied. There are two defined cable models: ▪ Worst Cable Model as defined in VESA DisplayPort 1.2a Standard, ▪ Zero length, zero loss cable. The equalizer is also defined in VESA DisplayPort 1.2a Standard
TP4	At the pins of a receiving device

Cable Models

The two cable models defined in VESA DisplayPort 1.2a Standard are:

1 Worst Case Cable Model—To achieve the TP3_EQ signal with the worst case cable model:

- Acquire the signal at TP2.
- Embed the TP2 signal with a “worst case” HBR cable model using an InfiniiSim Waveform Transformation Toolset software to emulate the insertion loss as defined in Figure 4-10 of the VESA DisplayPort 1.2a Standard.
  - For the DisplayPort Compliance Test Application, the “*CIC_rev0p6.s4p*” cable model transfer function is used.

- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

2 Zero Length Cable Model—To achieve the TP3_EQ signal with the zero length cable model:

- Acquire the signal at TP2.
- No cable model is embedded for the Zero Length cable model.
- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

Equalization

When equalization is required, use the CTLE (Continuous Time Linear Equalization) transfer function, as given in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

For main link, use the CTLE model with the following transfer function for HBR:

The HBR Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.725\times10^9)$$
$$\omega_{p1} = 2\pi(1.35\times10^9)$$
$$\omega_{p2} = 2\pi(2.5\times10^9)$$

Figure 97 Transfer Function of the CTLE model for HBR

For main link, use the CTLE model with the following transfer function for HBR2:

The HBR2 Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 98 Transfer Function of the CTLE model for HBR2

Clock Recovery

When Clock Recovery is required, the clock recovery technique follows the definition of the receiver PLL as defined in Section 3.5.3.5 of the VESA DisplayPort 1.2a Standard. For main link, use the second-order clock recovery function with a closed loop tracking bandwidth and damping factor, with respect to the PRBS7 pattern, as shown in Table 91:

Table 91 Main Link Second-Order Clock Recovery Function

Bit Rate	Band wid th	Damping Factor
HBR2	10 MHZ	1.00
HBR	10 MHz	1.51
RBR	5.4 MHz	1.51

Test Point Definition for MyDP 1.0 Source Tests

Test the Source DUT at Test Point 2 (TP2) as shown in Figure 99.

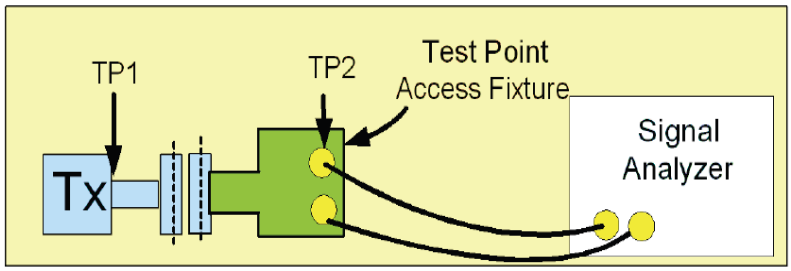


Figure 99 Test Point 2 Connection for MyDP 1.0 Source Tests

Use MyDP Test Fixtures (MyDP-to-DP type or MyDP-to-SMA type) to perform PHY compliance tests specific to MyDP. Figure 100 shows the layout of a MyDP passive cable adapter or a MyDP protocol converter:

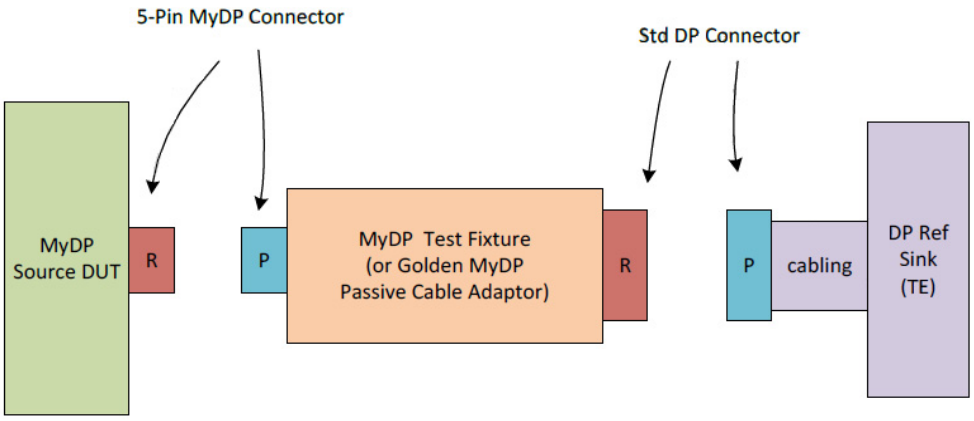


Figure 100 Schematics of MyDP to SMA Test Fixtures used for PHY Compliance Tests

Table 92 defines the test point fixtures and instruments used for MyDP 1.0 Source Tests:

Table 92 Test Point Fixtures and Instruments for MyDP 1.0 Source Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 101).

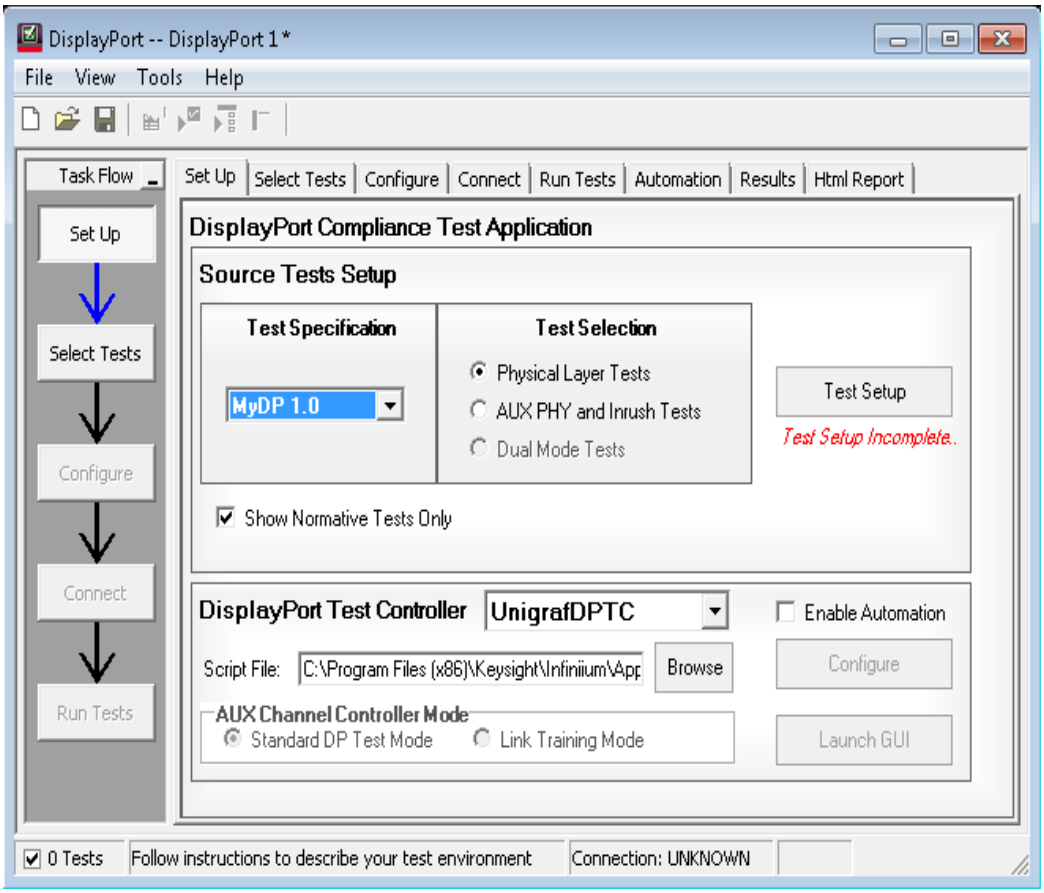


Figure 101 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with Mobility DisplayPort 1.0 Standards, select **MyDP 1.0** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for MyDP 1.0 Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

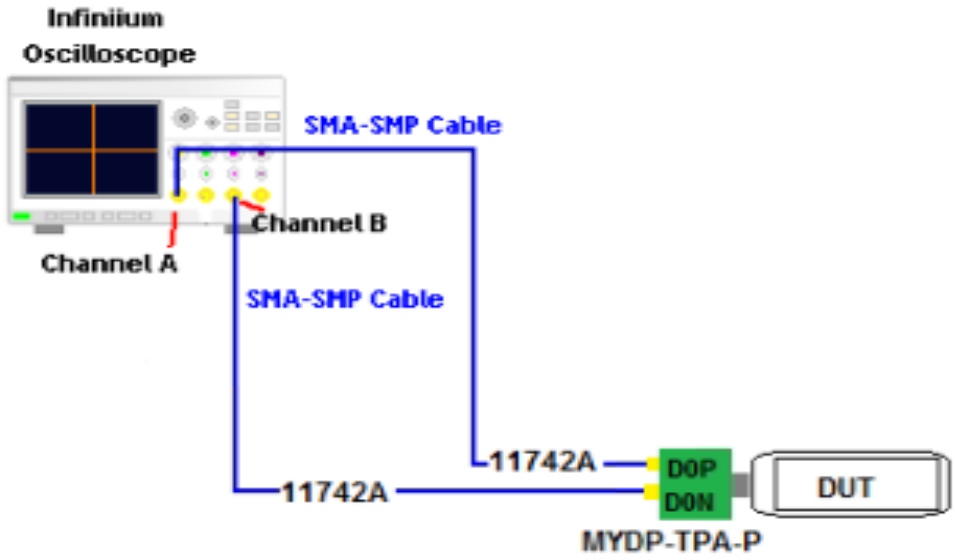


Figure 102 Sample connection diagram for MyDP 1.0 Source Tests

Source Eye Diagram Test

Test ID

1210001 – Eye Diagram Test

Test Overview

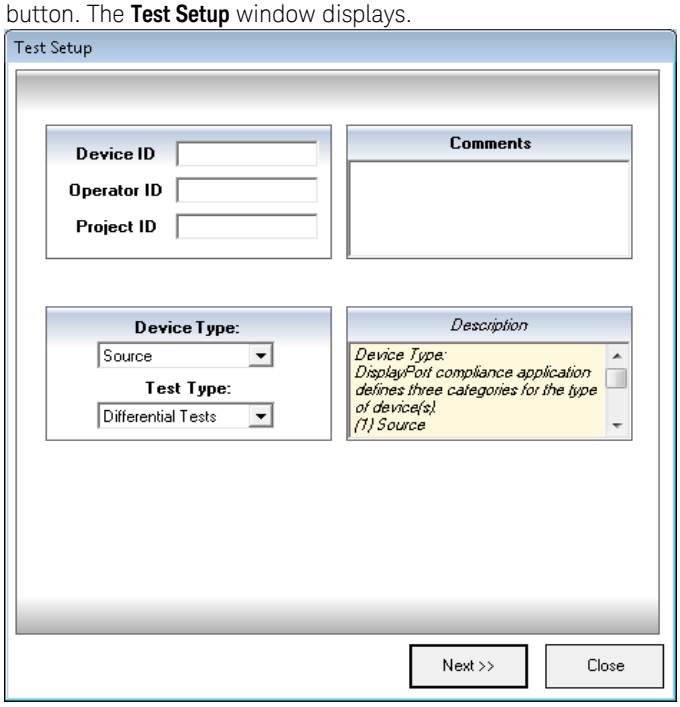
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



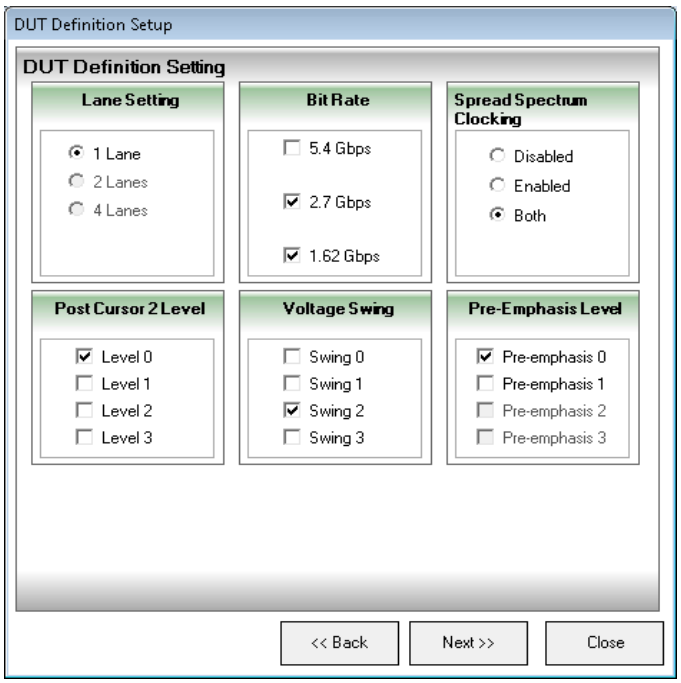
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

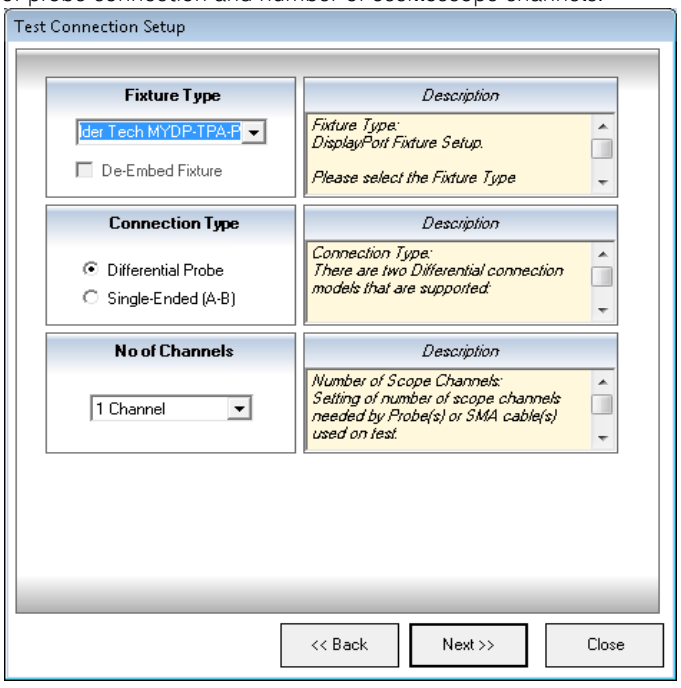
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

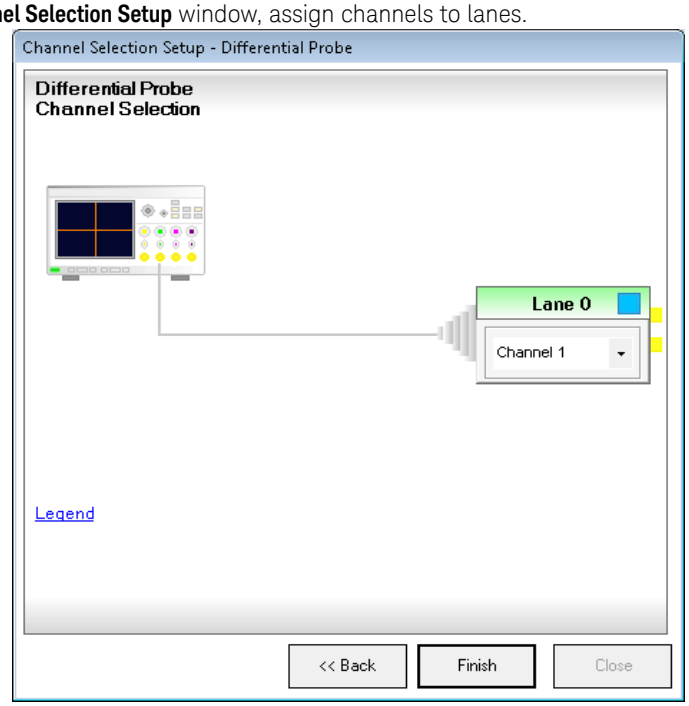
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

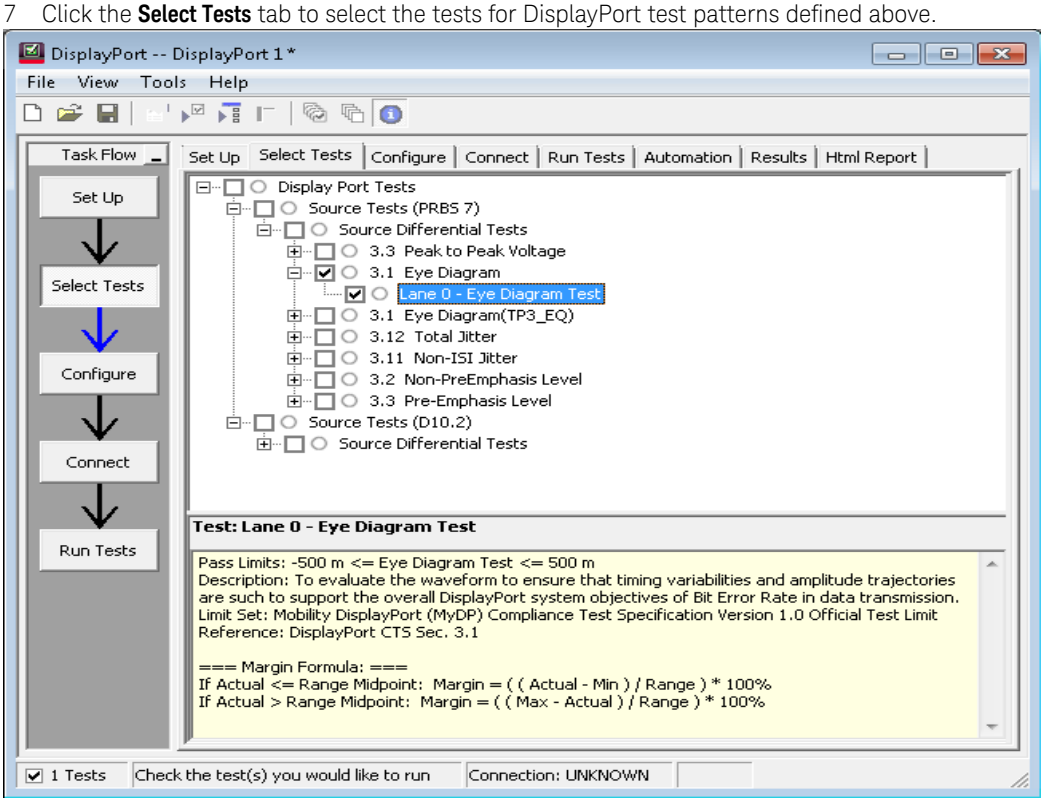


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.
11 Check for any signal trajectories that may have entered into the mask.
12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 93 shows the voltage and time coordinates for the mask used in the eye diagram.

Table 93 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	High (2.7 Gb/s)
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

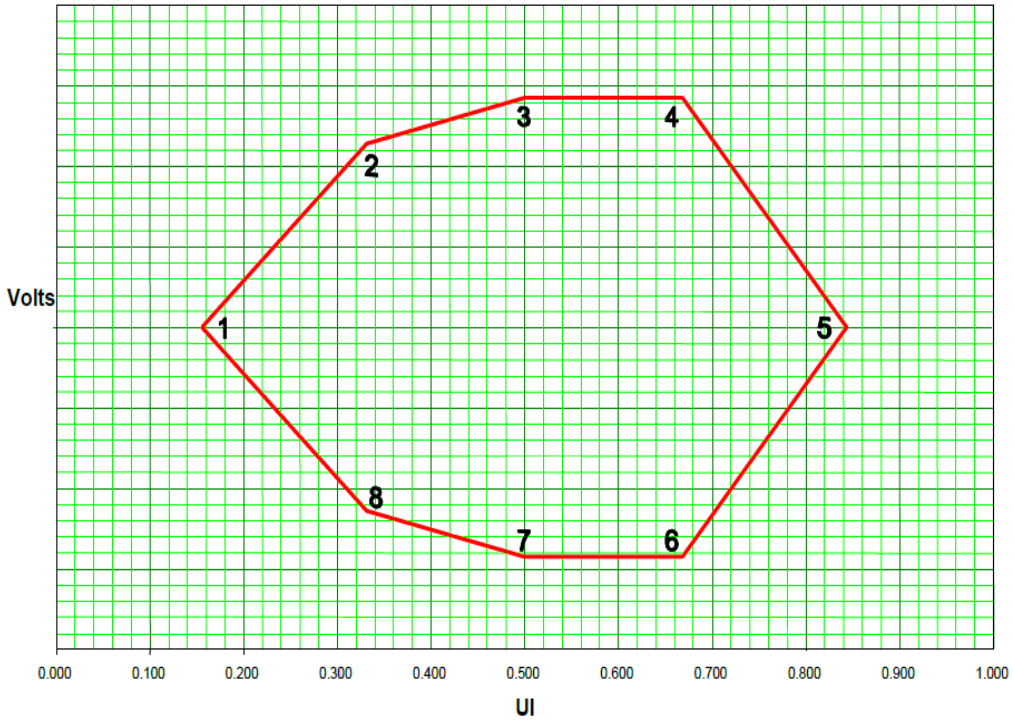


Figure 103 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*

- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-24 for RBR and Table 3-23 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

1220001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

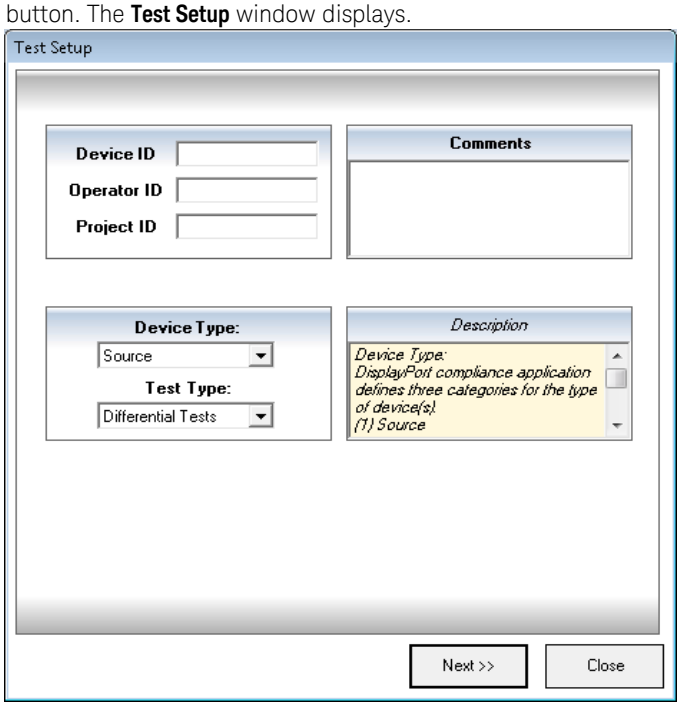
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



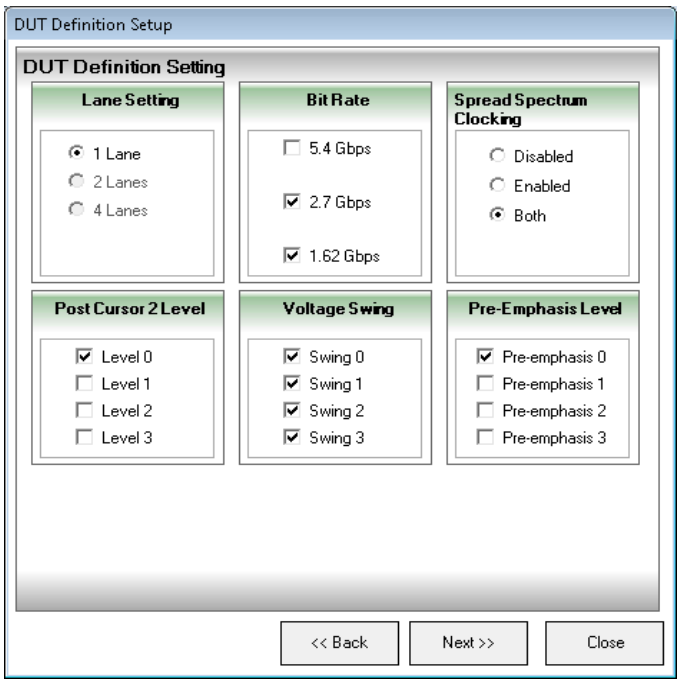
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

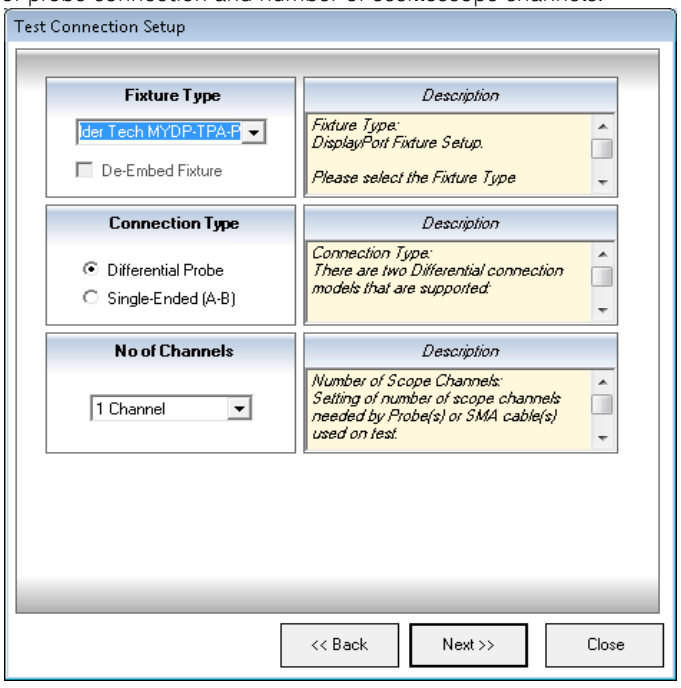
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

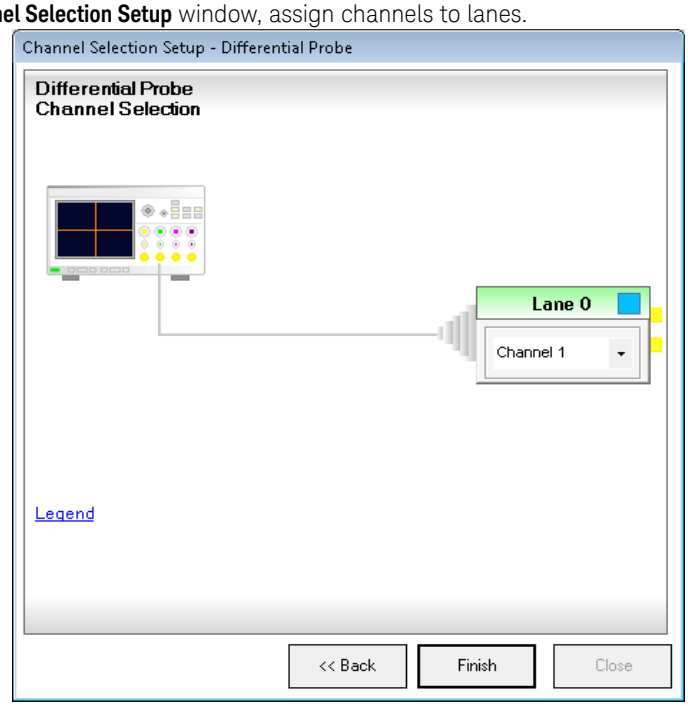
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

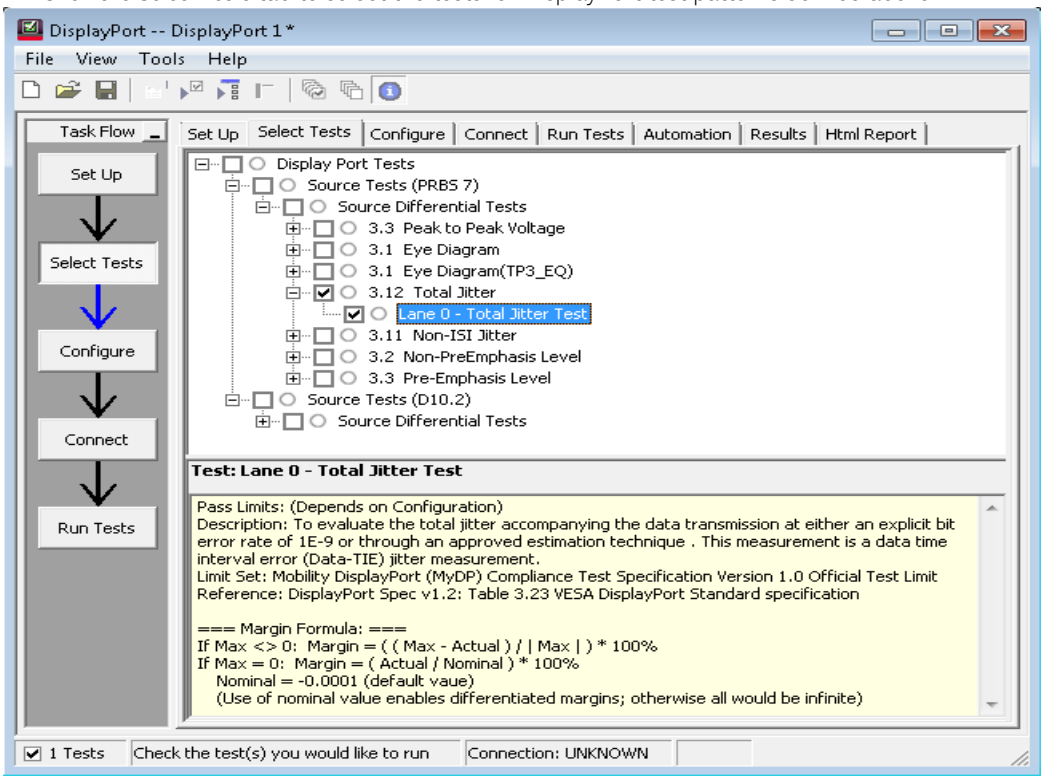


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 94 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
Ap-p	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
Ap-p	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non-ISI Jitter Test

Test ID

1230001 – Non ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission.

The jitter is separated into each jitter components based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

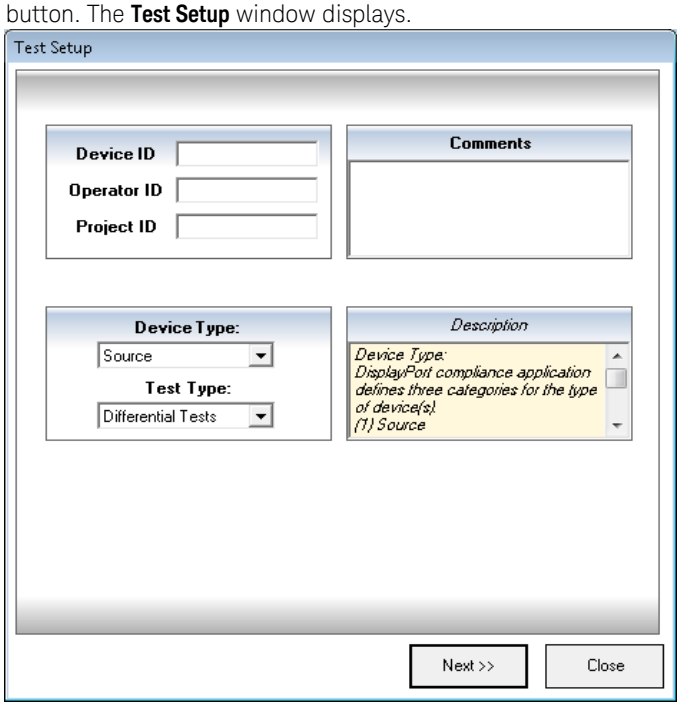
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



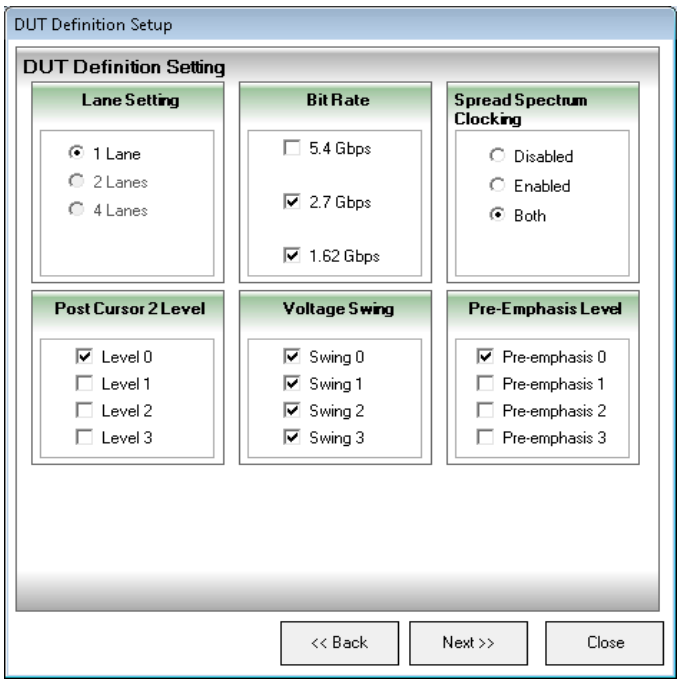
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

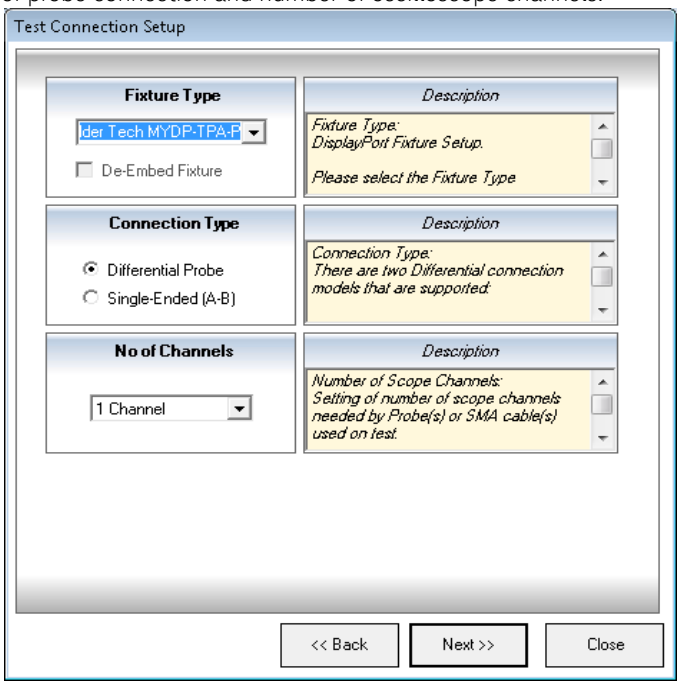
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

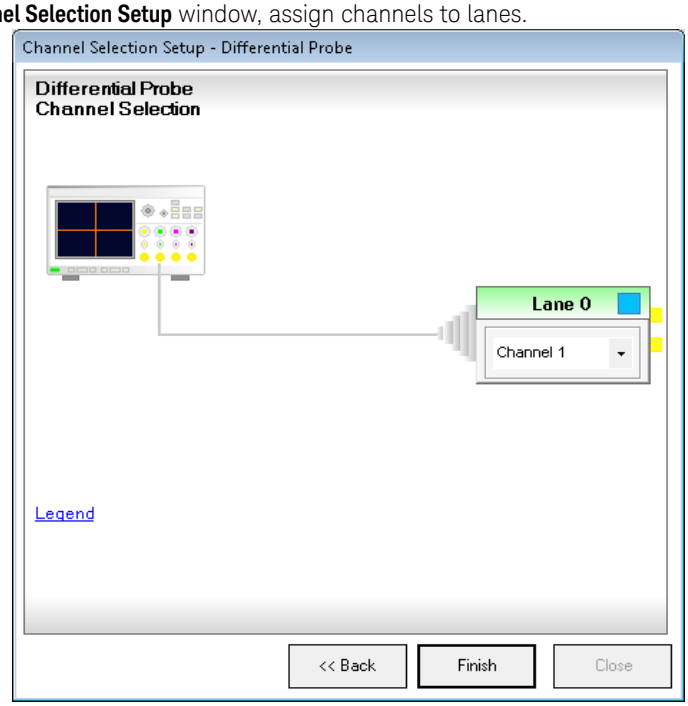
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

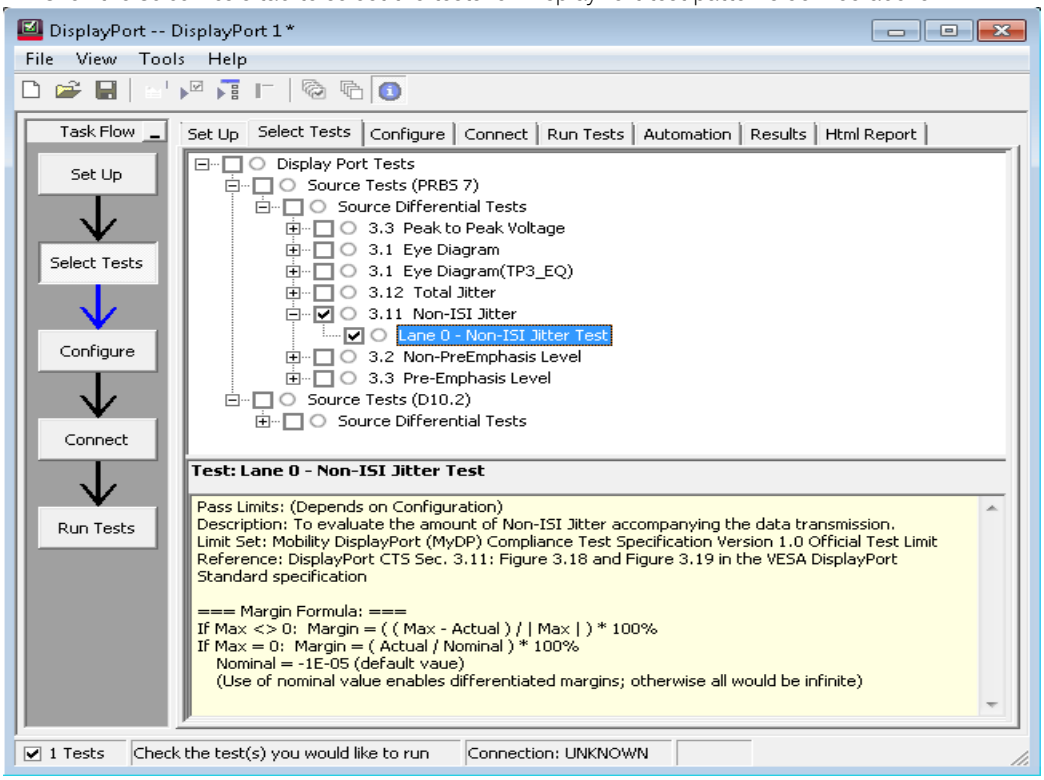


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = TJ - ISI$$

7 Report the measurement results.

PASS Condition

Table 95 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.210 UI

UI is Unit Interval.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.11*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1261001 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For HBR2:

- 1264101 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

Test Overview

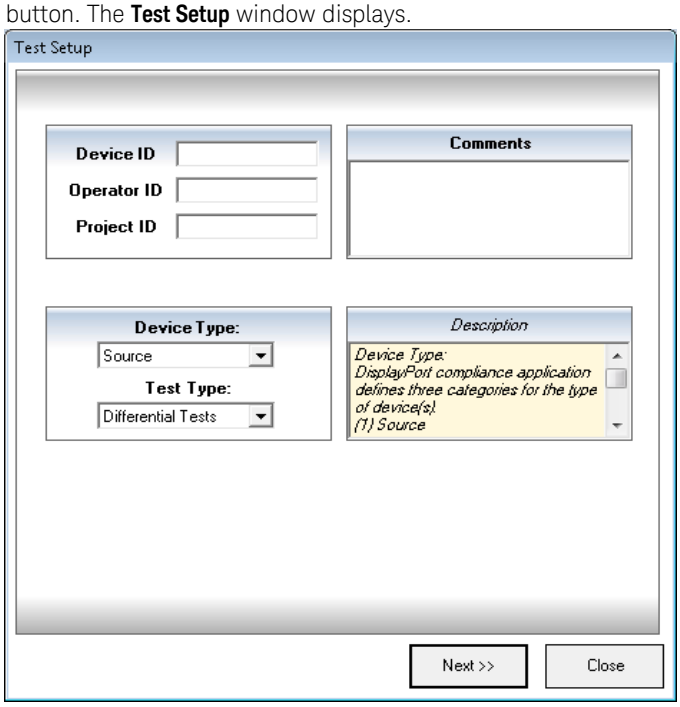
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



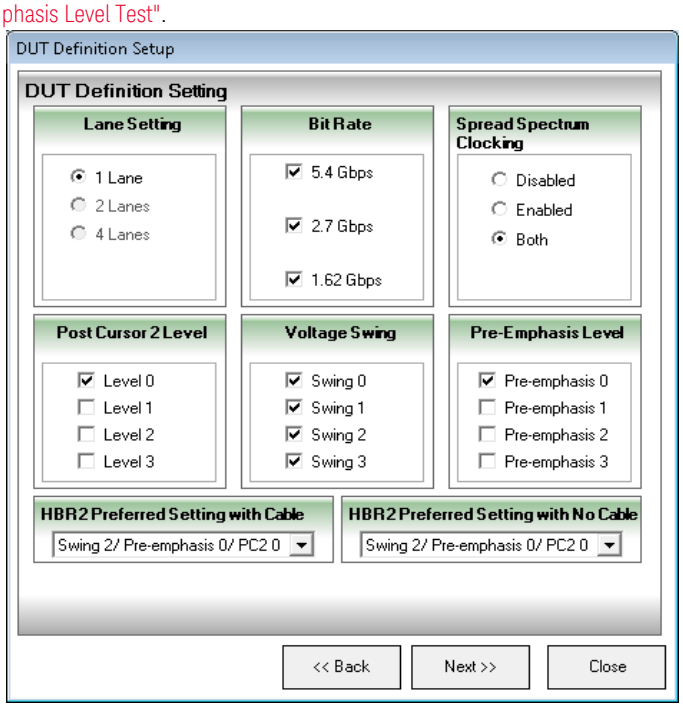
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

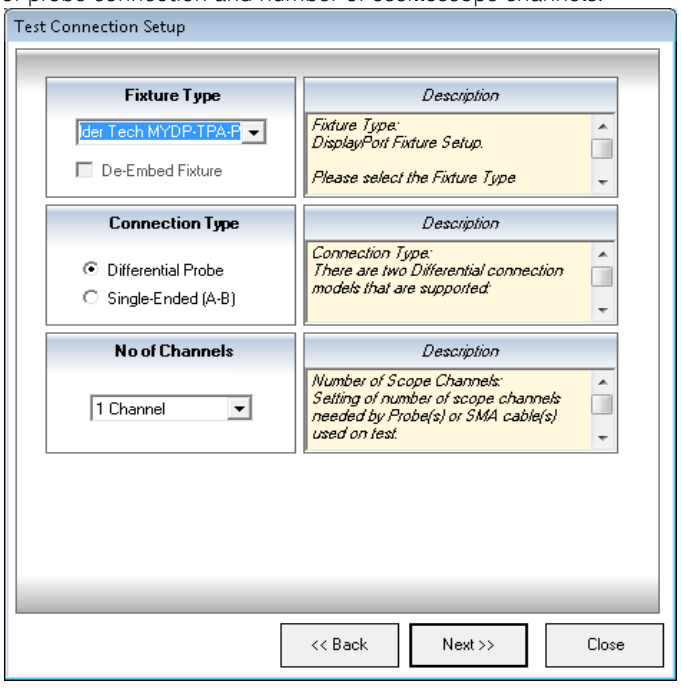
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

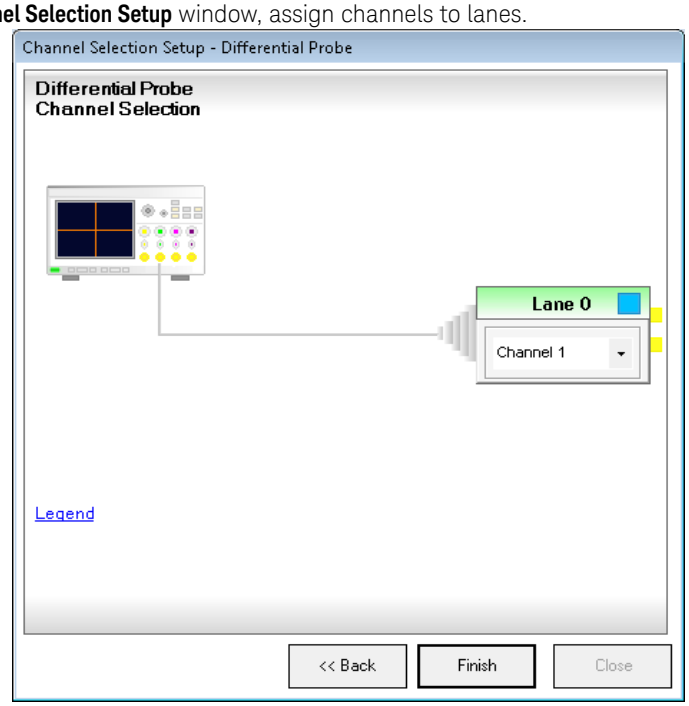
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non Pre-Emphasis Level Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

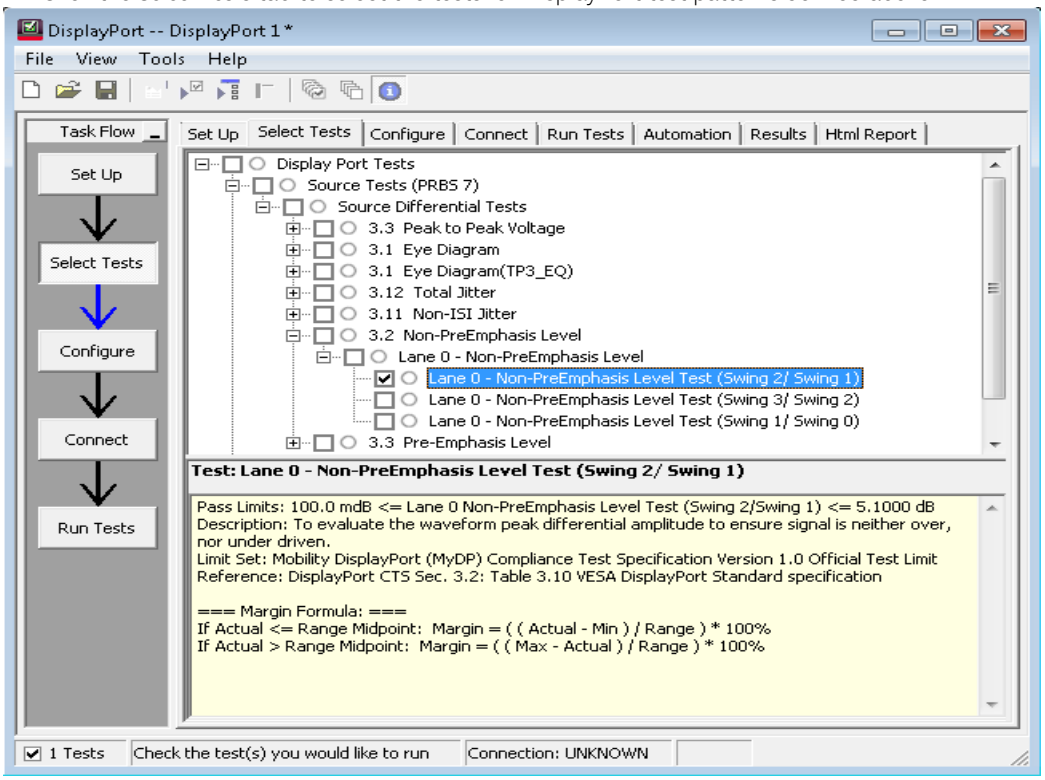


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

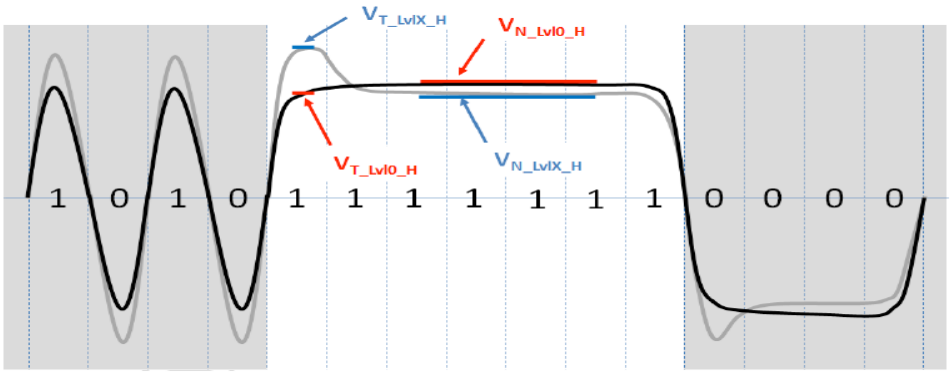


Figure 104 High Voltage measurement for RBR and HBR

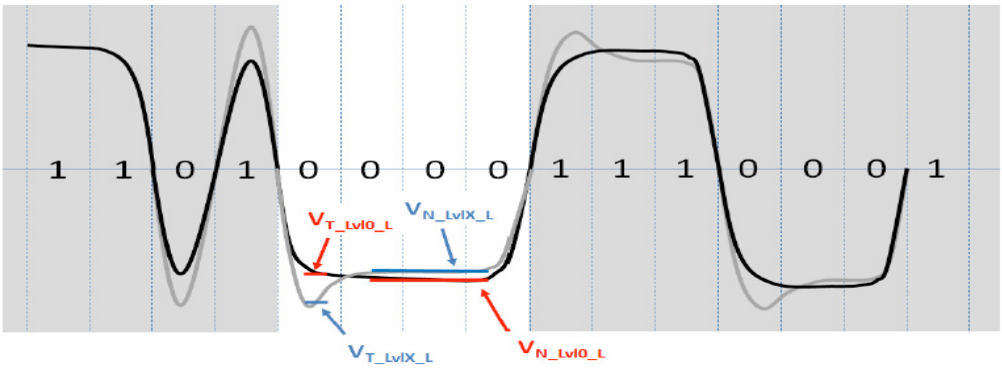


Figure 105 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

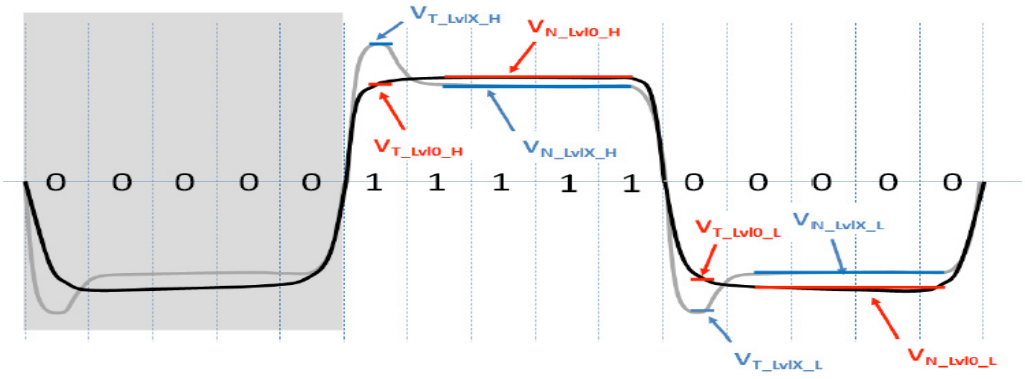


Figure 106 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * Log_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

Resultant = $20 * Log_{10}[Voltage_{Peak\text{-}Peak\_LevelA} / Voltage_{Peak\text{-}Peak\_LevelB}]$

Table 96 Compared Levels

Measurement#	$Voltage_{Peak\text{-}Peak\_LevelA}$	$Voltage_{Peak\text{-}Peak\_LevelB}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
HBR2		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
* if device optionally capable of Level 3		

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1 dB ≤ Resultant ≤ 4.4 dB

Table 97 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-OUTPUT-RATIO\_RBR\_HBR}$	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	
$V_{TX-OUTPUT-RATIO\_HBR2}$	Ratio of Output Voltage Level 2/Level 0	5.2	-	6.9	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	1.6	-	3.5	dB	
	Ratio of Output Voltage Level 3/Level 2	1	-	4.4	dB	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Differential Tests

Test ID

For RBR and HBR:

- 1270001 – Pre-Emphasis Level Test

For HBR2:

- 1270501 – Pre-Emphasis Level Test

Test Overview

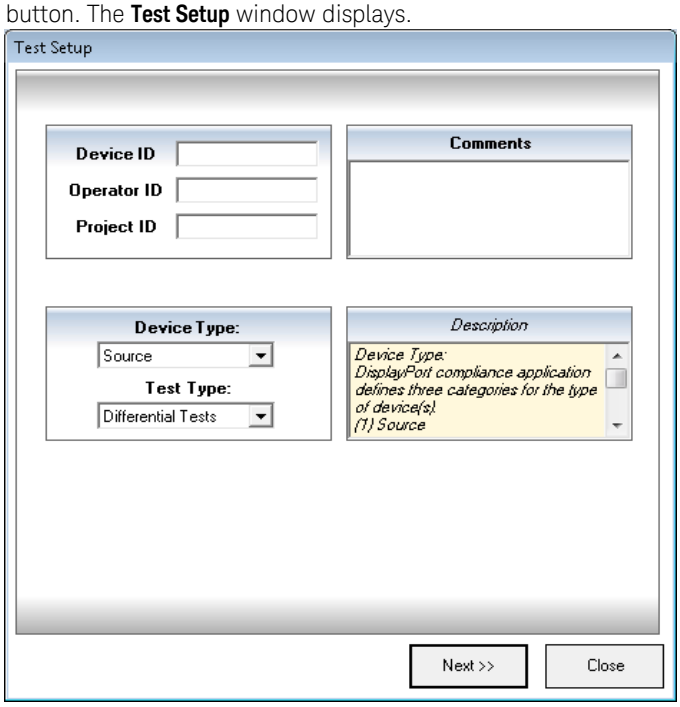
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



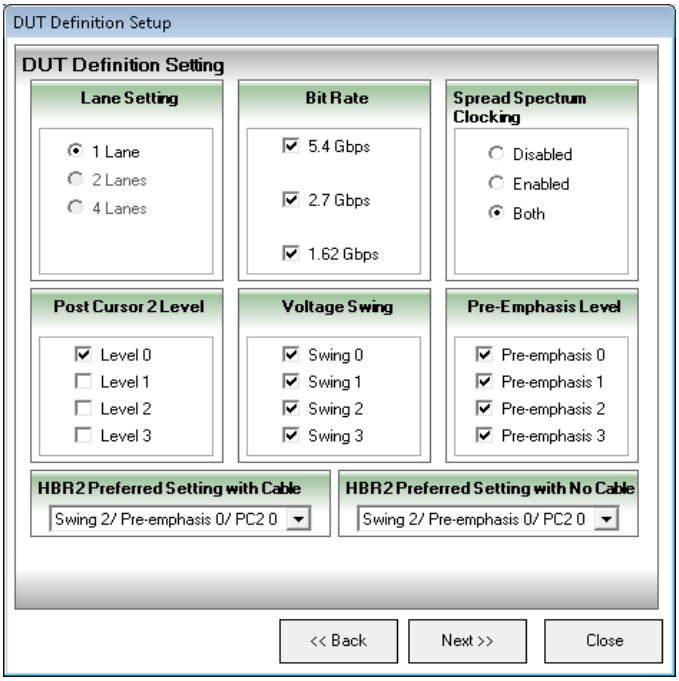
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

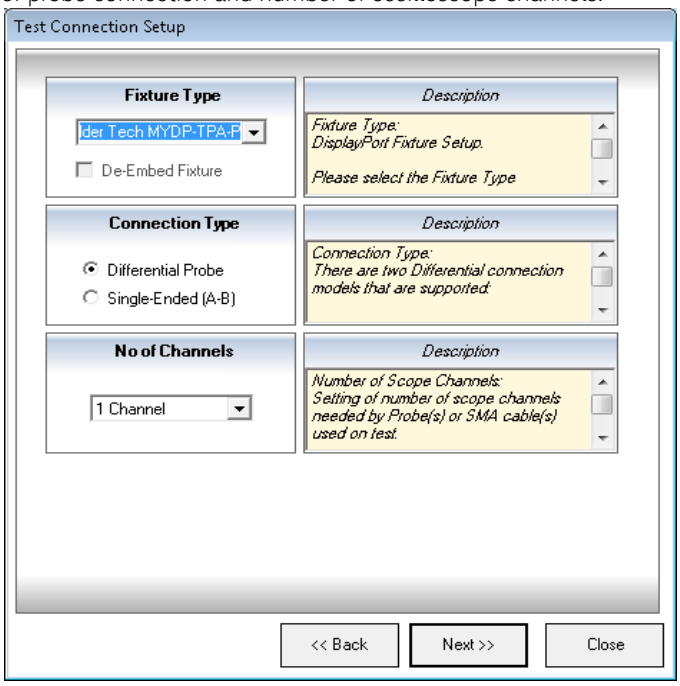
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

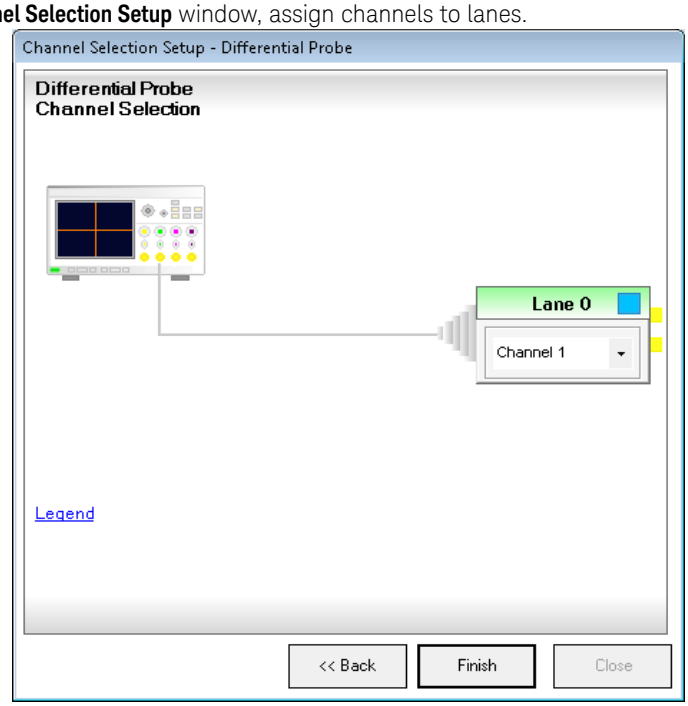
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Pre-Emphasis Level Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

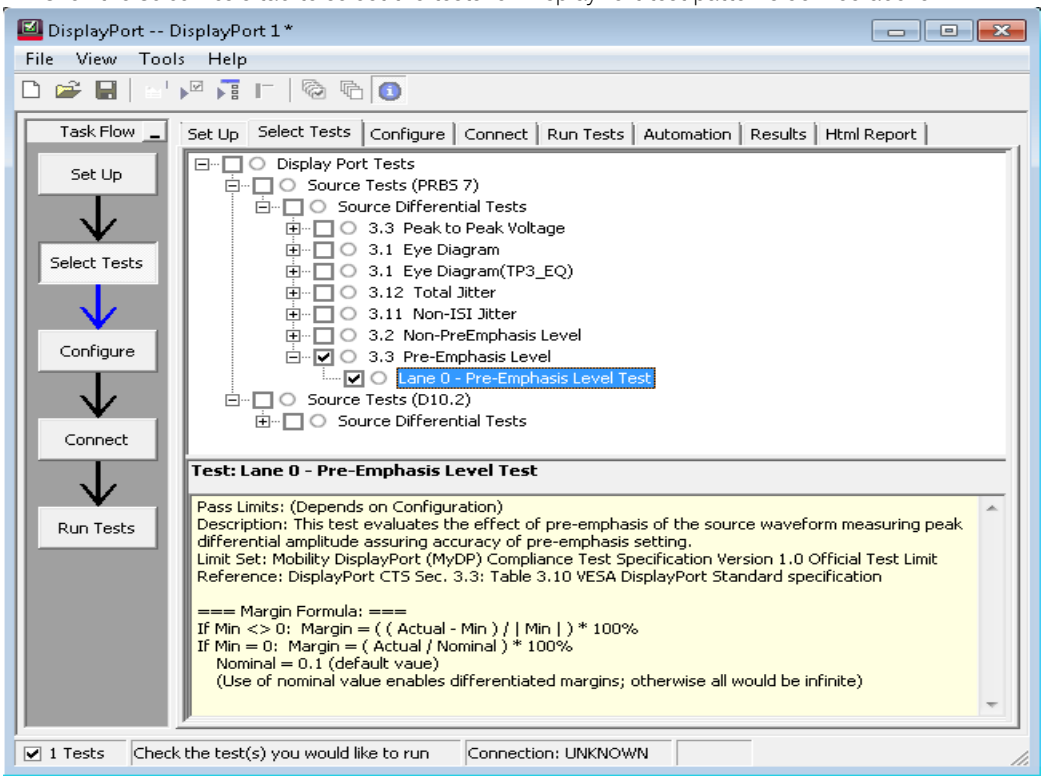


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

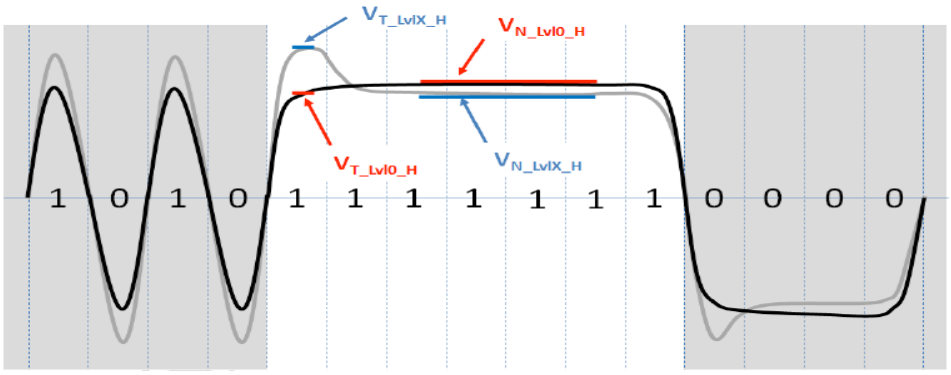


Figure 107 High Voltage measurement for RBR and HBR

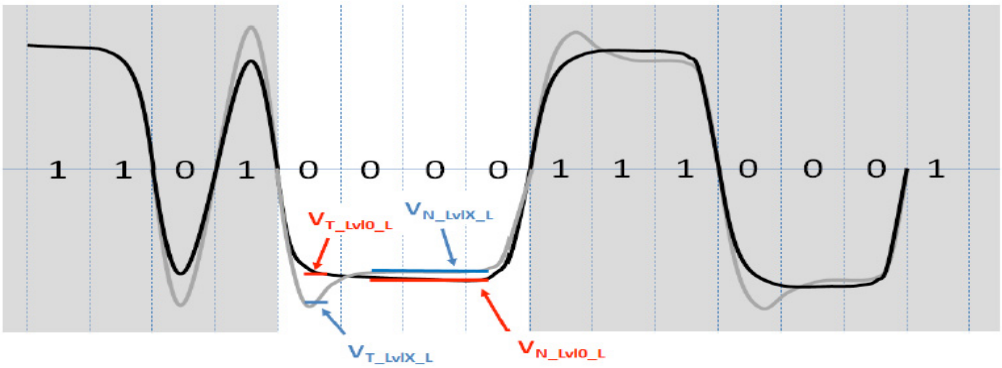


Figure 108 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

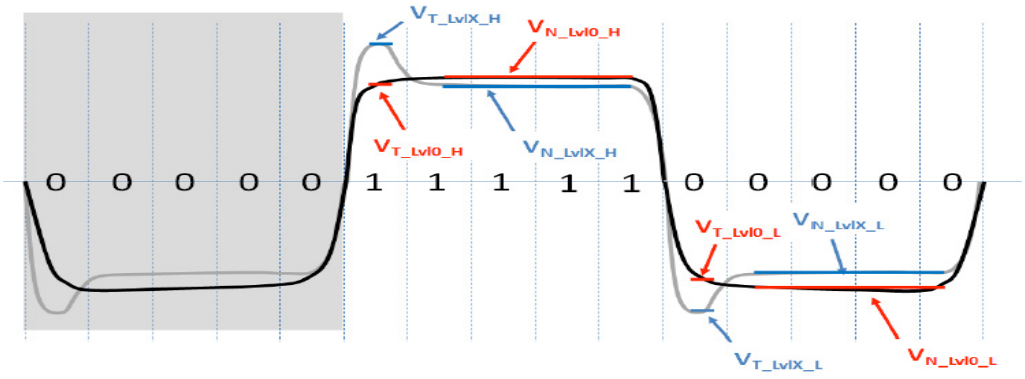


Figure 109 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl1\_PP} / \text{Voltage}_{N\_Lvl1\_PP}] - 20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl2\_PP} / \text{Voltage}_{N\_Lvl2\_PP}] - 20 * \text{Log}[\text{Voltage}_{T\_Lvl1\_PP} / \text{Voltage}_{N\_Lvl1\_PP}]$ for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl3\_PP} / \text{Voltage}_{N\_Lvl3\_PP}] - 20 * \text{Log}[\text{Voltage}_{T\_Lvl2\_PP} / \text{Voltage}_{N\_Lvl2\_PP}]$ for Voltage Swing Level 0, if supported.

Table 98 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For RBR and HBR:

- 1272001 – Non-Transition Voltage Range Measurement (Swing 0)
- 1273001 – Non-Transition Voltage Range Measurement (Swing 1)
- 1274001 – Non-Transition Voltage Range Measurement (Swing 2)

For HBR2:

- 1272101 – Non-Transition Voltage Range Measurement (Swing 0)
- 1273101 – Non-Transition Voltage Range Measurement (Swing 1)
- 1274101 – Non-Transition Voltage Range Measurement (Swing 2)

Test Overview

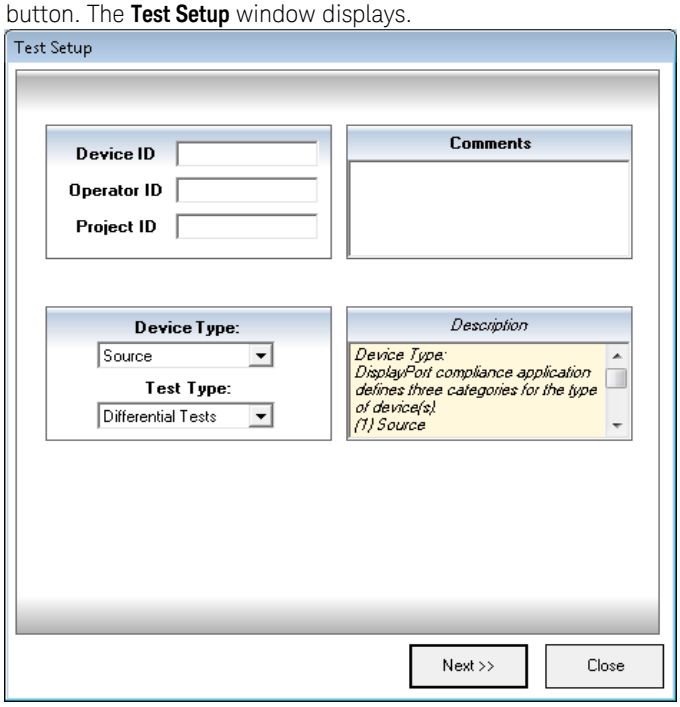
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



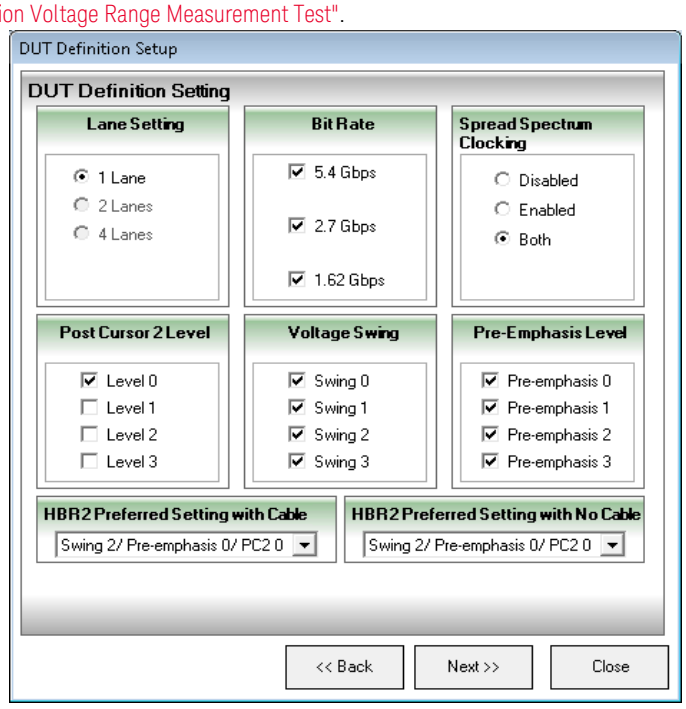
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

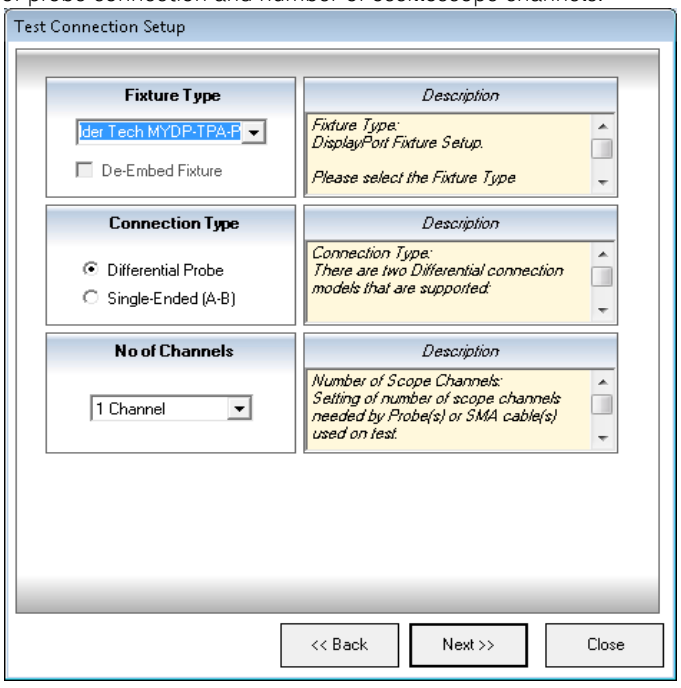
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

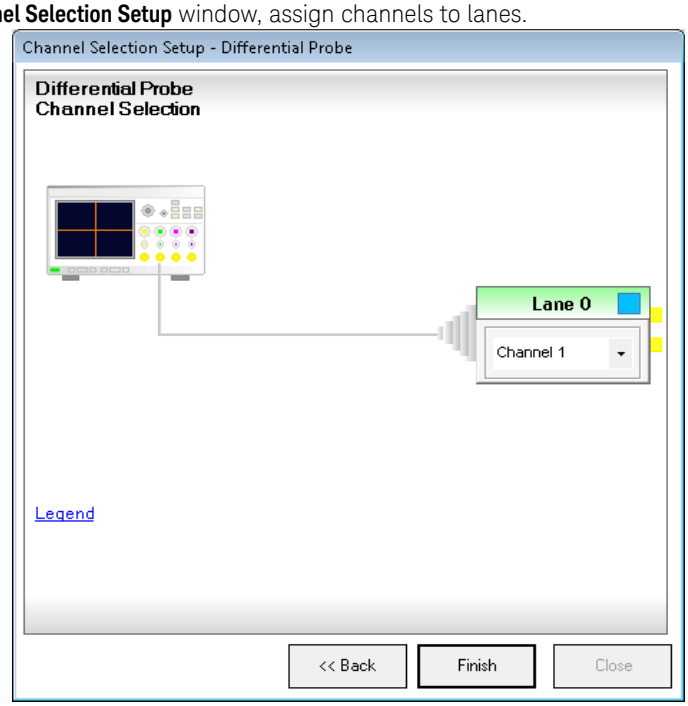
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non Transition Voltage Range Measurement Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

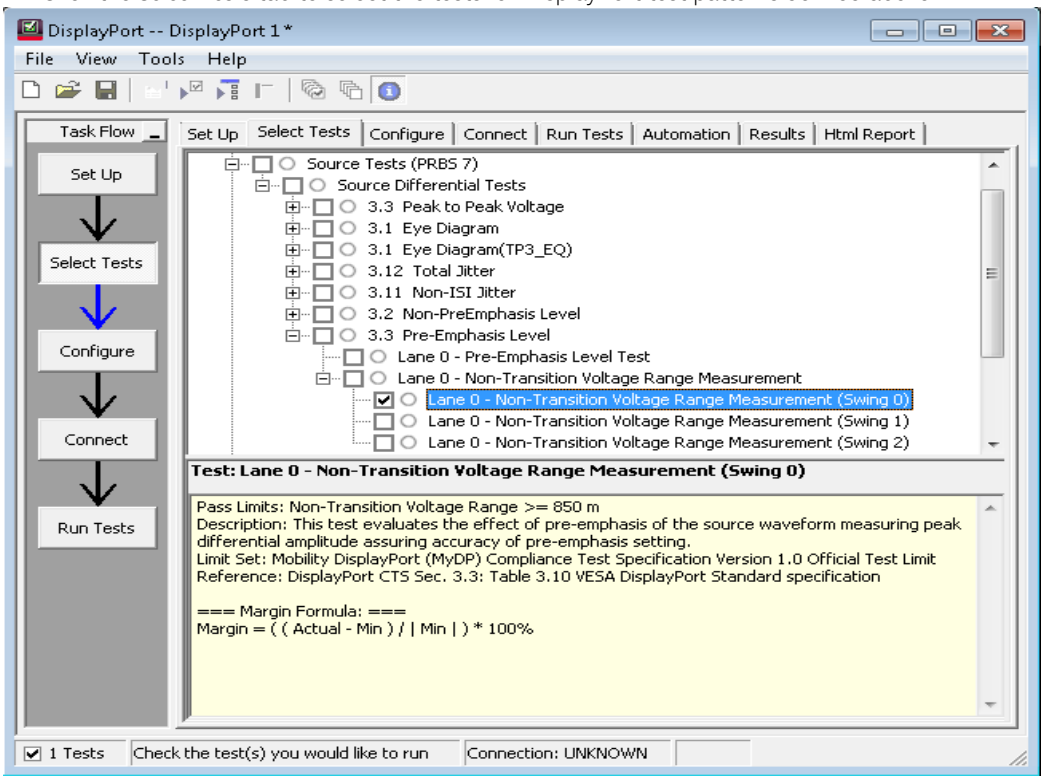


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

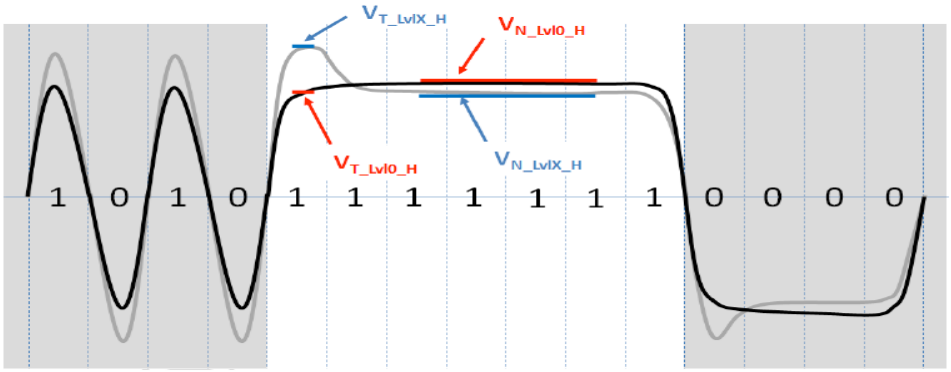


Figure 110 High Voltage measurement for RBR and HBR

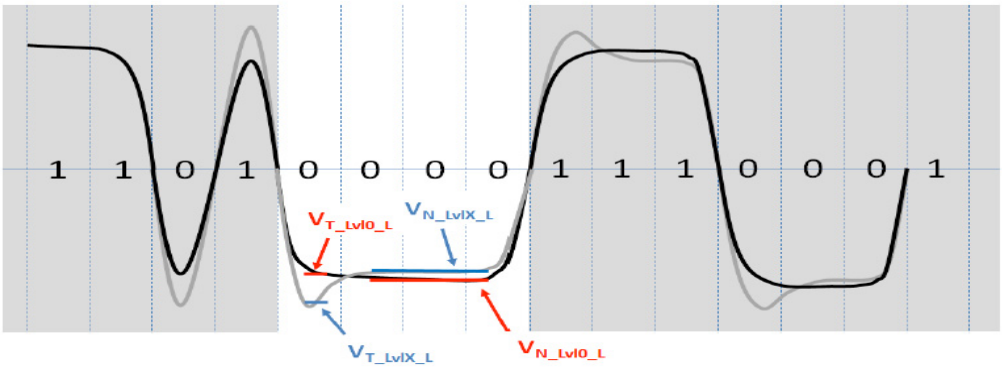


Figure 111 Low Voltage measurement for RBR and HBR

e For HBR2 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

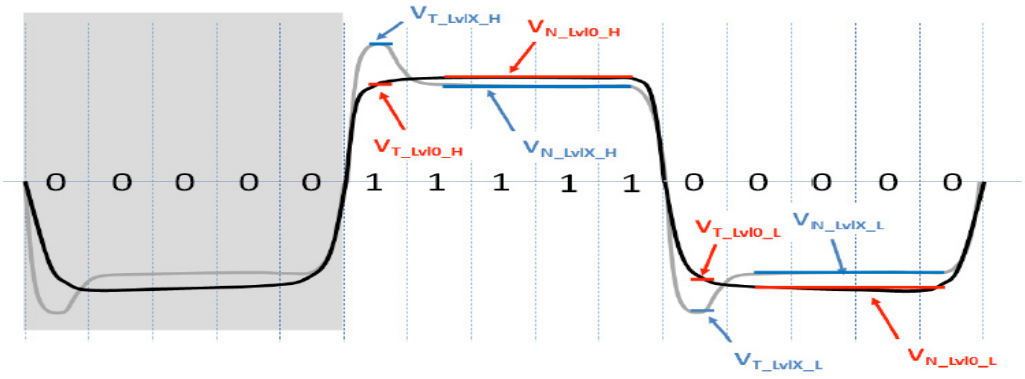


Figure 112 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant $\geq$ 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant $\geq$ 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant $\geq$ 0.85 OR 20*log(Resultant) > -1.4dB

Table 99 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX\text{-}DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX\text{-}DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For RBR and HBR:

- 1266001 – Peak to Peak Voltage Test

For HBR2:

- 1266101 – Peak to Peak Voltage Test

Test Overview

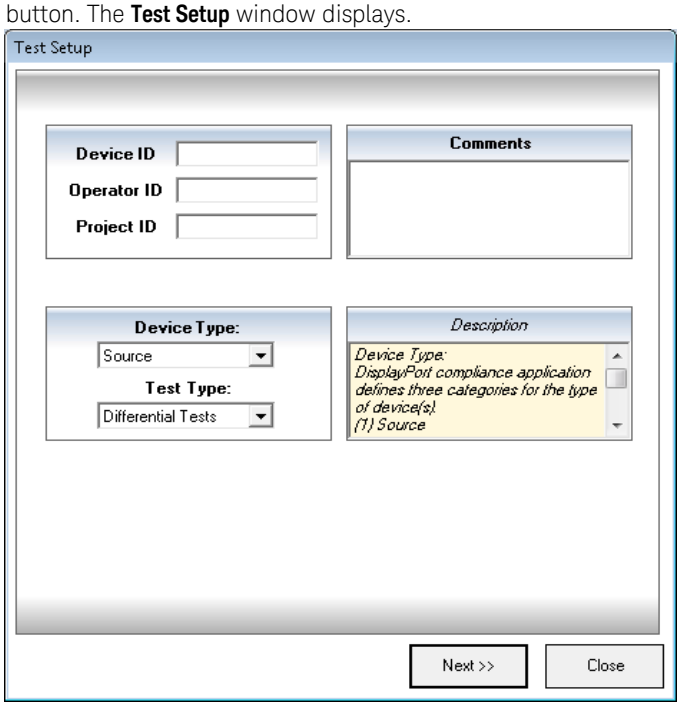
The objective of this test is to evaluate the maximum differential peak to peak voltage.

Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



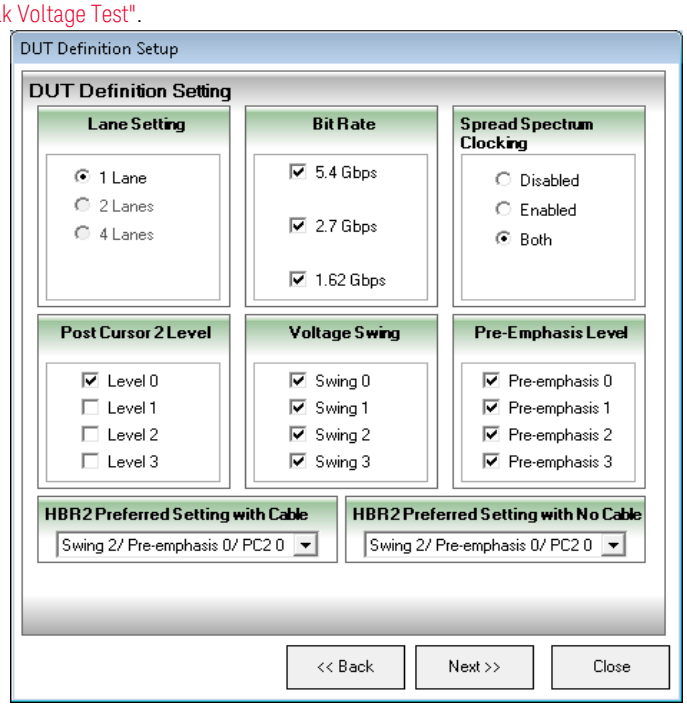
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

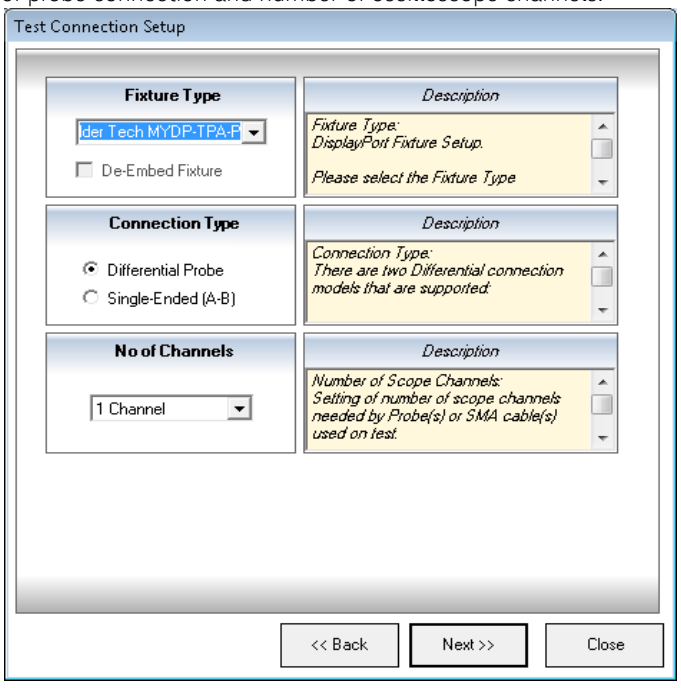
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

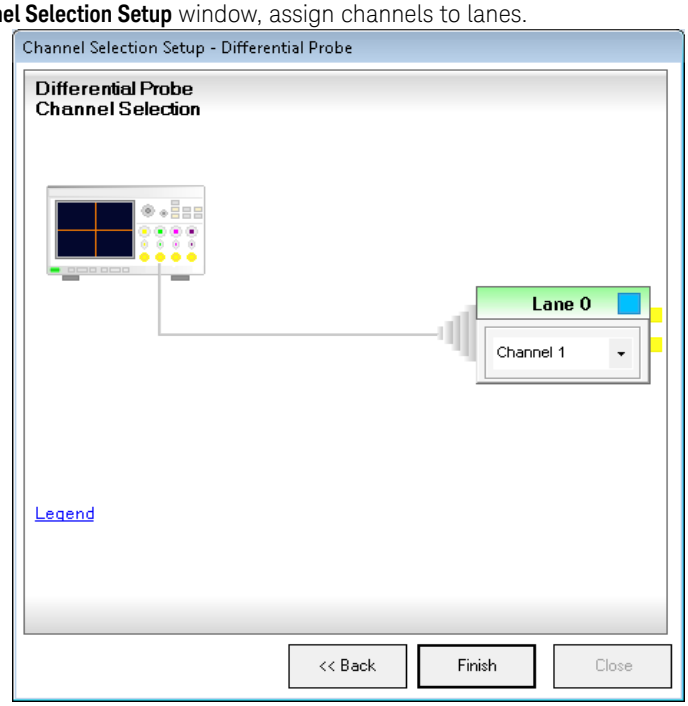
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Peak to Peak Voltage Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

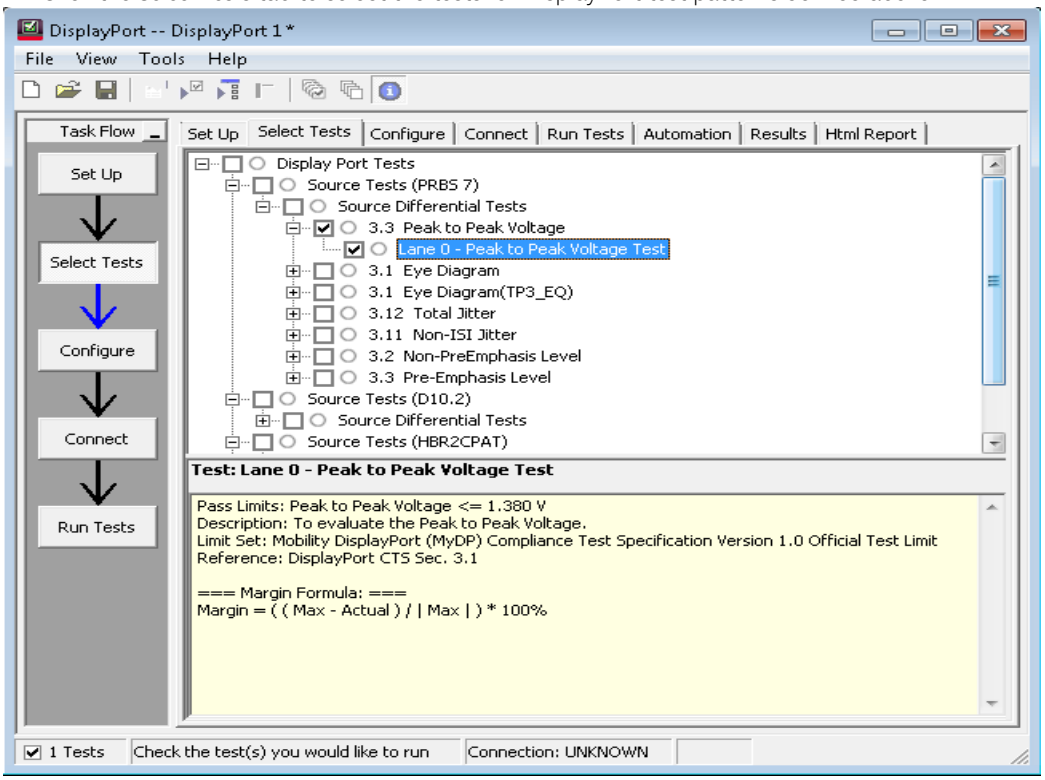


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = \text{Maximum Voltage} - \text{Minimum Voltage}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V

Table 100 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Main Link Frequency Compliance Test

Test ID

12193001 – Main Link Frequency Compliance

Test Overview

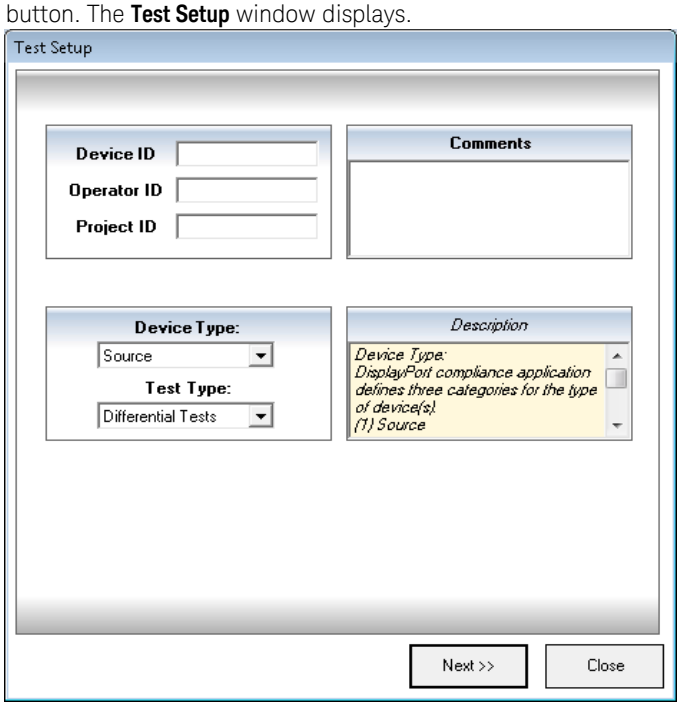
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.2a Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



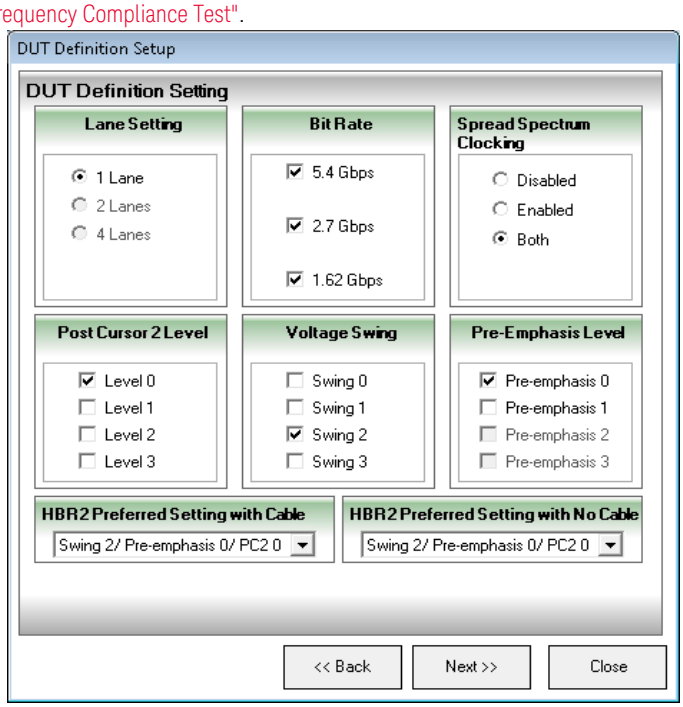
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

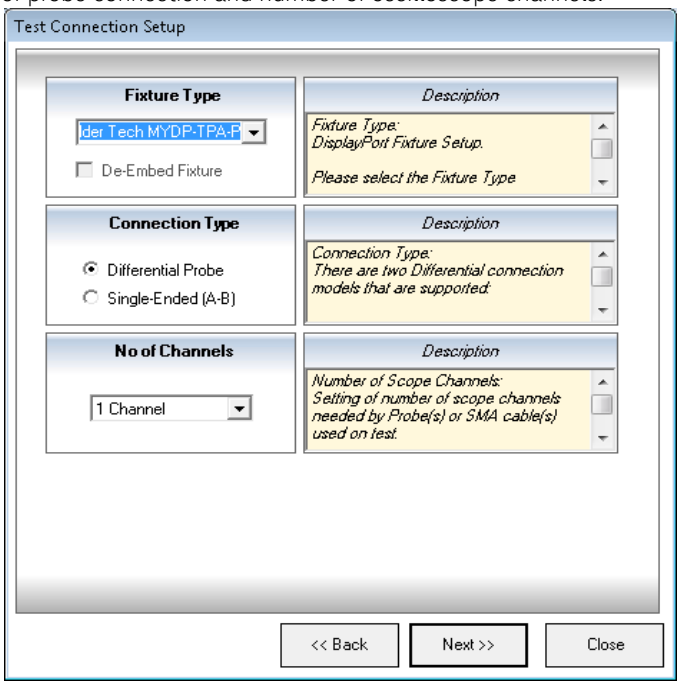
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

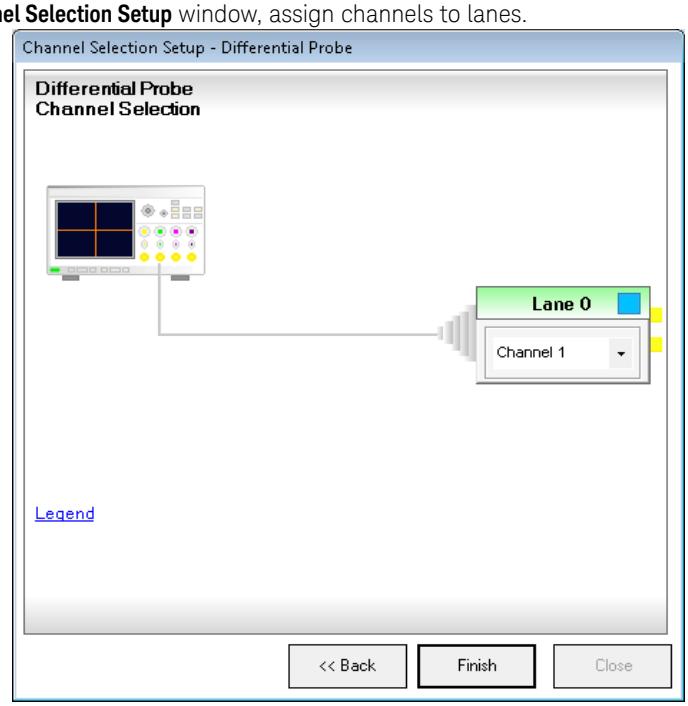
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Main Link Frequency Compliance Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

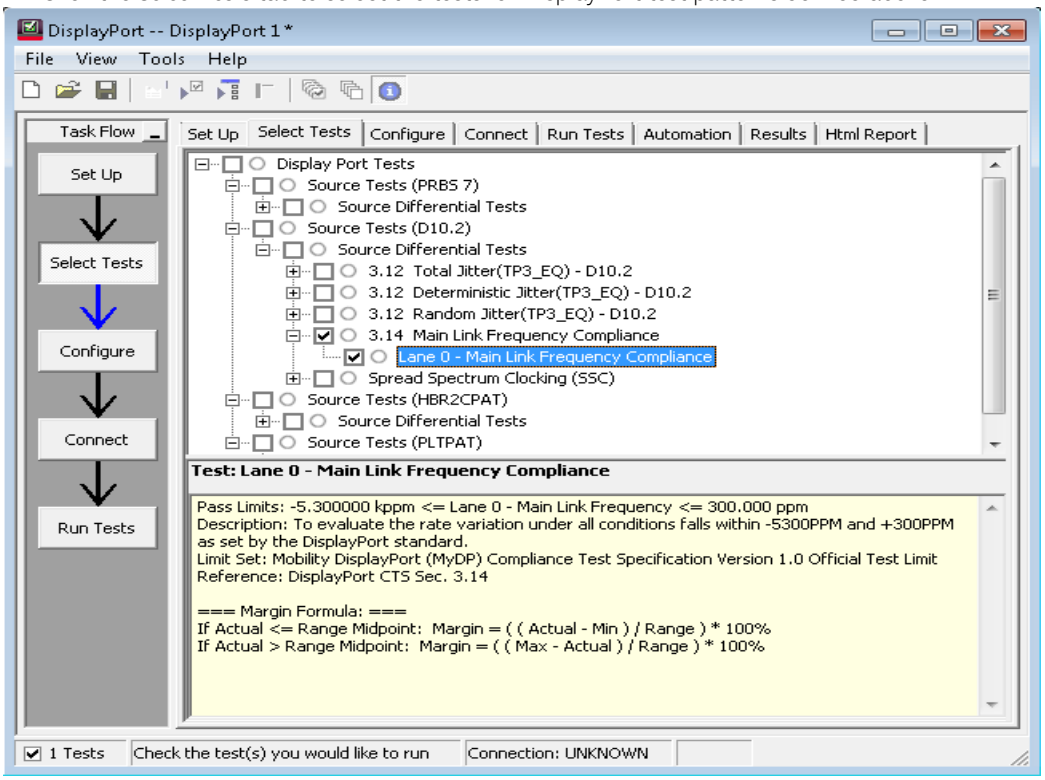


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.
5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.

9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:

a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.

b Acquire the signal with one complete SSC cycle.

c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

Maximum Data Rate = 1 / (Minimum Unit Interval)

d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

Minimum Data Rate = 1 / (Maximum Unit Interval)

e Repeat steps b, c and d until you acquire 10 SSC Cycles.

f Calculate the mean value for the maximum and minimum data rates.

10 Report the measurement results.

PASS Condition

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

Table 101 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.14*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

12170001 – SSC Modulation Frequency Test

Test Overview

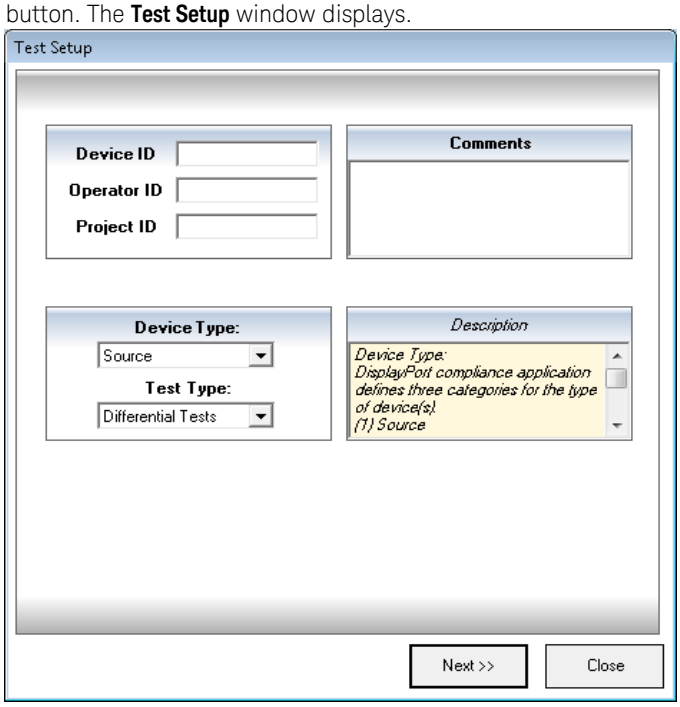
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



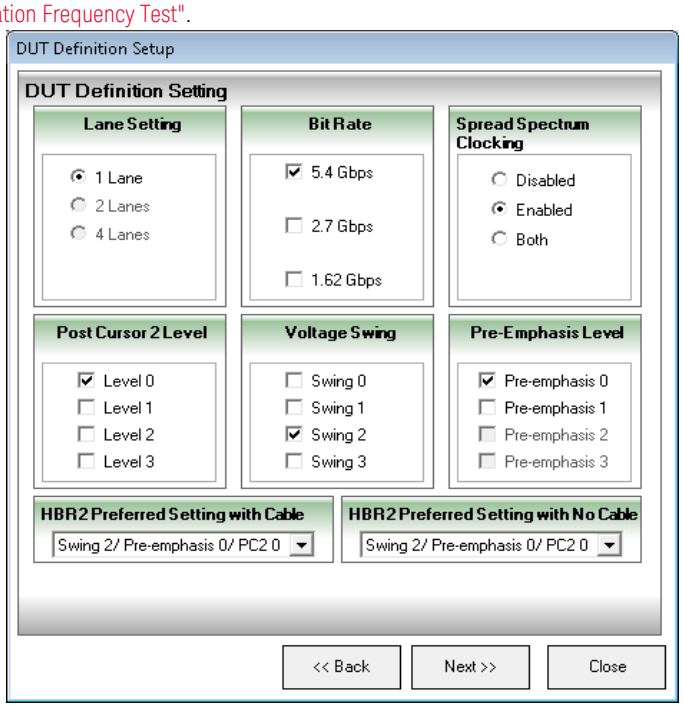
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

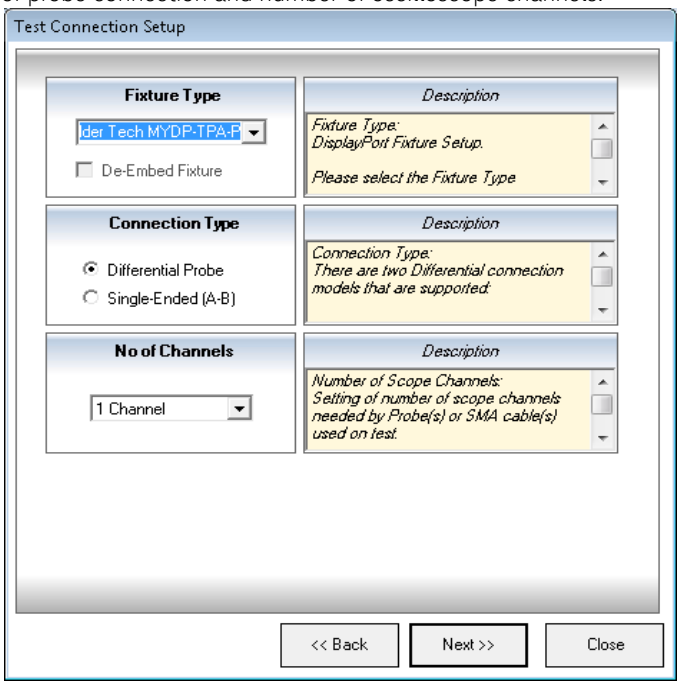
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

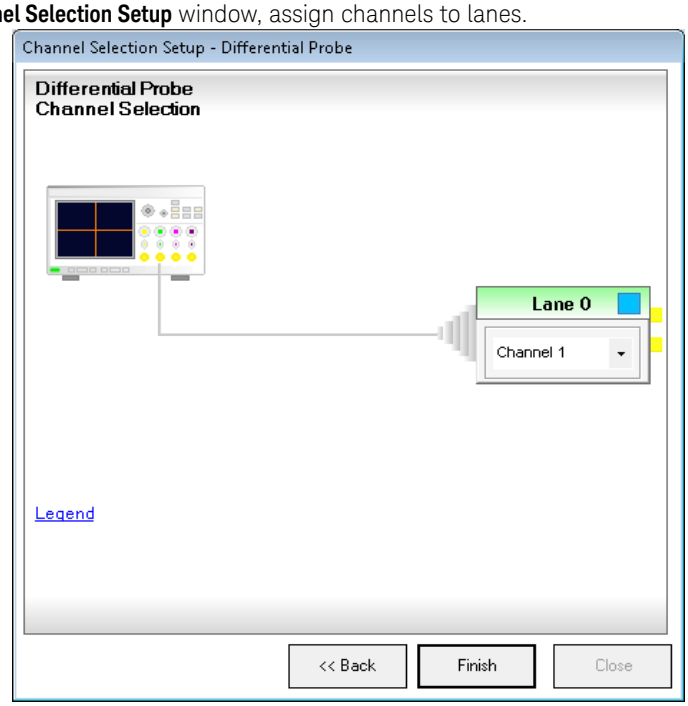
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Modulation Frequency Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

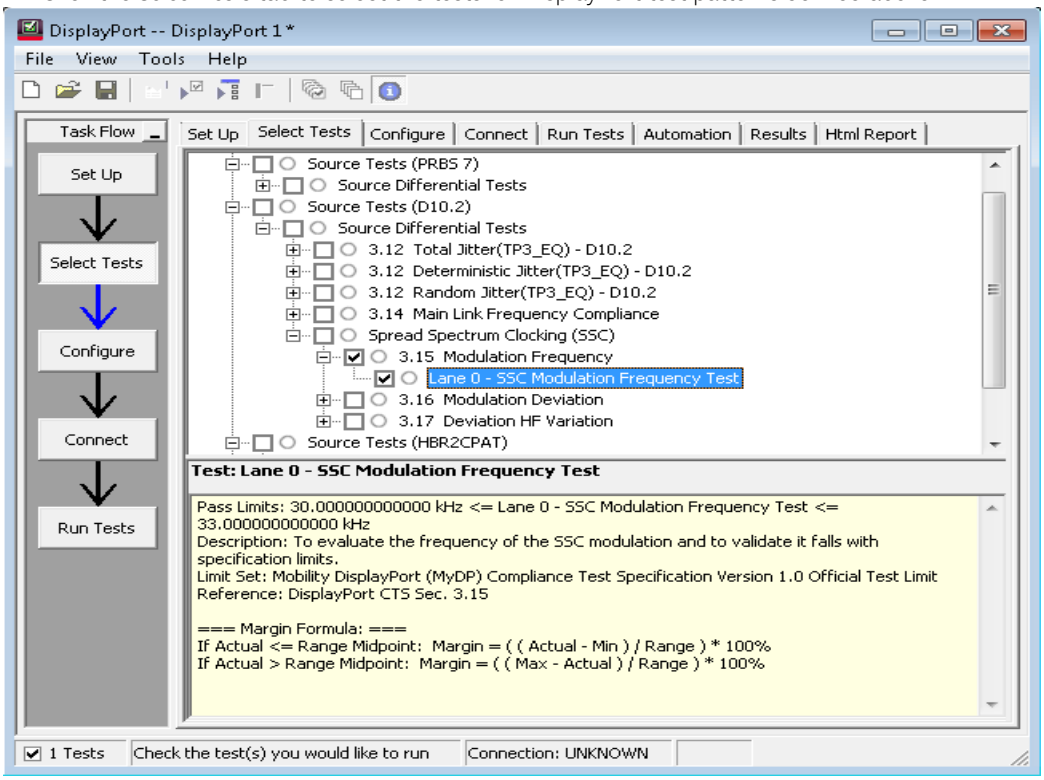


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
   g Acquire the signal for 10 SSC Cycles.
6 Get the mean value for the SSC Modulation frequency.
7 Report the measurement results.

PASS Condition

30kHz ≤ SSC Modulation Frequency (f_{SSC}) ≤ 33kHz

Table 102 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

12180001 – SSC Modulation Deviation Test

Test Overview

The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2^{nd} order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

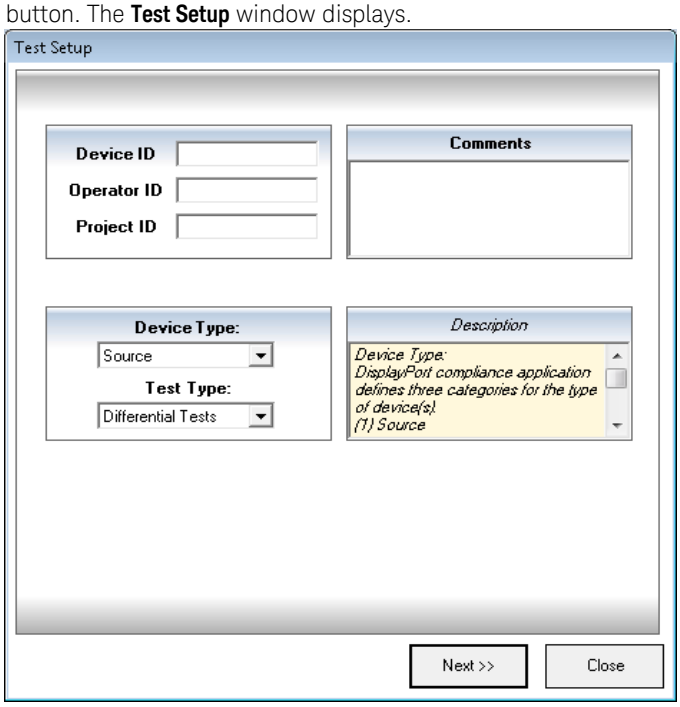
SSC Modulation Deviation = {[Average (Maximum Data Rate) - Average (Minimum Data Rate)] / Nominal Data Rate}*1e6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



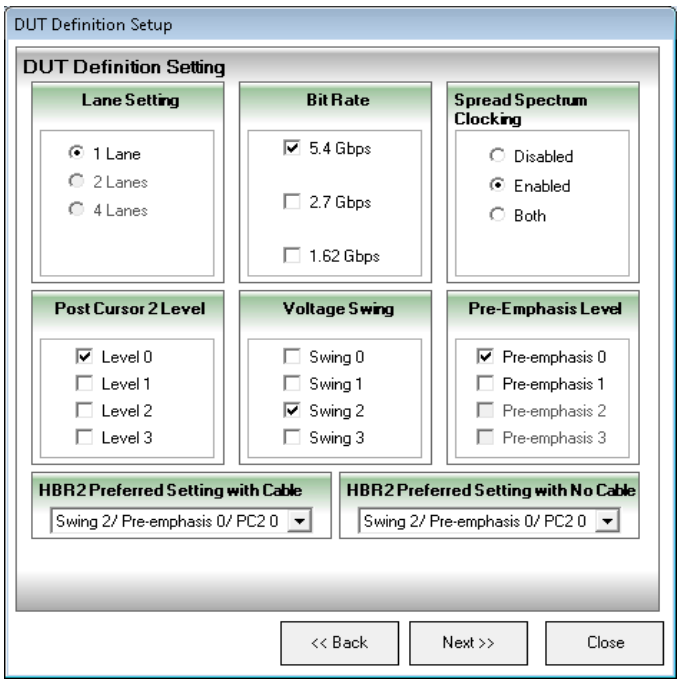
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

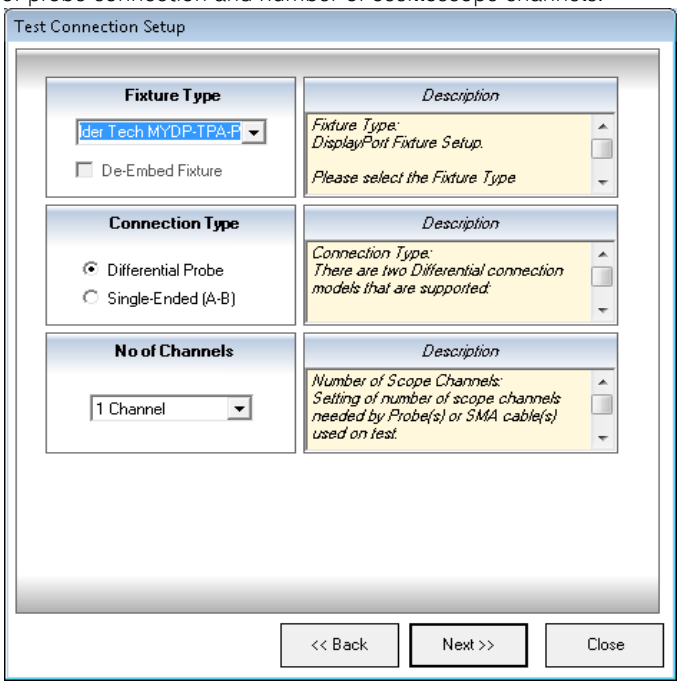
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

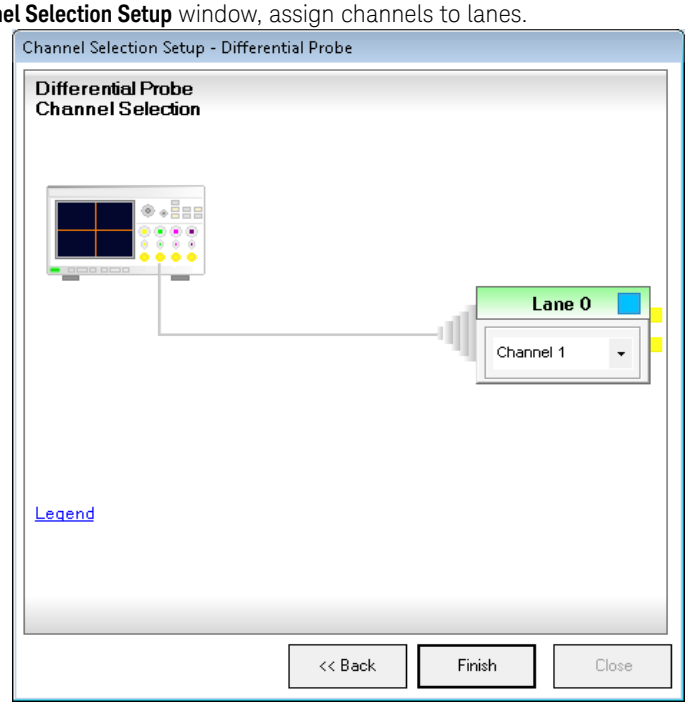
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Modulation Deviation Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

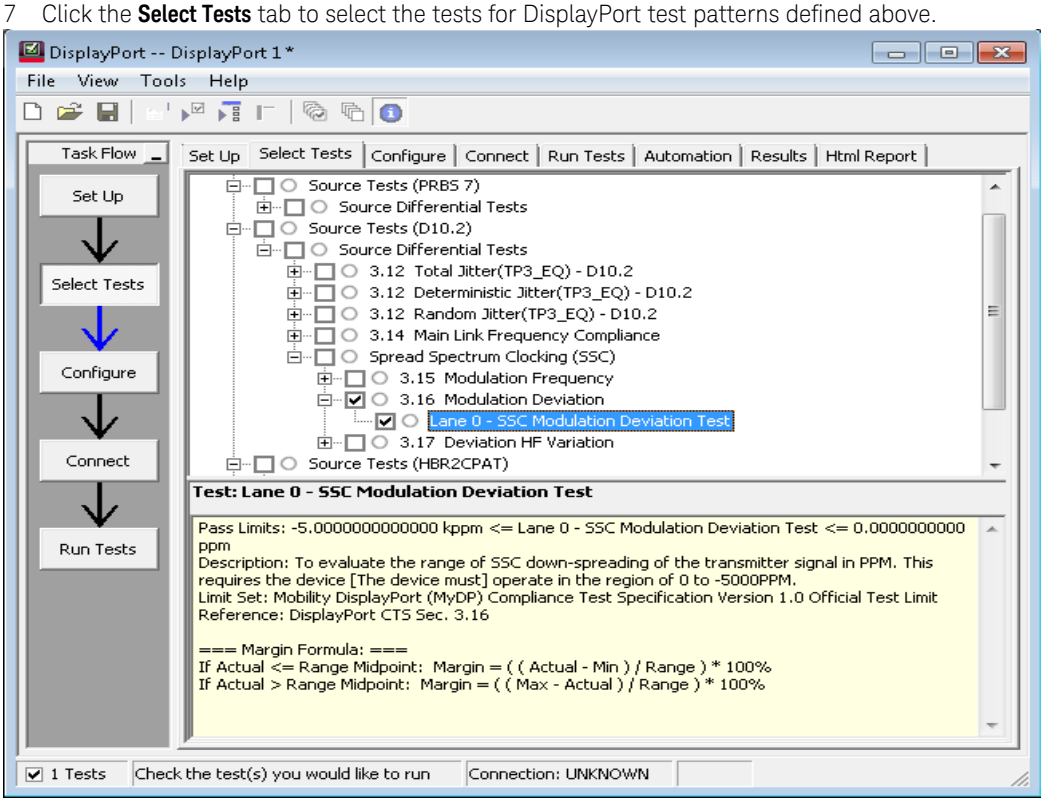


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.
5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.

9 Set up the parameters for SSC measurement.

a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.

b Acquire the signal with one complete SSC Cycle.

c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

Maximum Data Rate = 1/Minimum Unit Interval

d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

Minimum Data Rate = 1/Maximum Unit Interval

e Repeat step b,c and d until you acquire 10 SSC Cycles.

f Calculate the mean value for the maximum and minimum data rate.

10 Calculate the SSC Modulation Deviation using the equation:

SSC Modulation Deviation = (Maximum Data Rate - Minimum Data Rate) / (Nominal Data Rate) * 1E6

11 Report the measurement results.

PASS Condition

-5000ppm ≤ SSC Modulation Deviation ($Resultant_{SSC\ Range}$) ≤ 0ppm

Table 103 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.16*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

12200001 – SSC Deviation HF Variation Test (Informative)

Test Overview

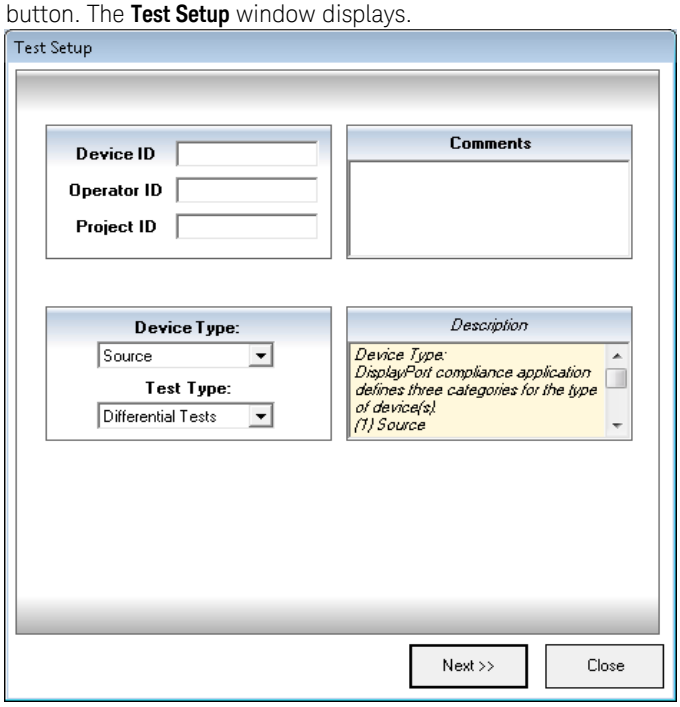
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



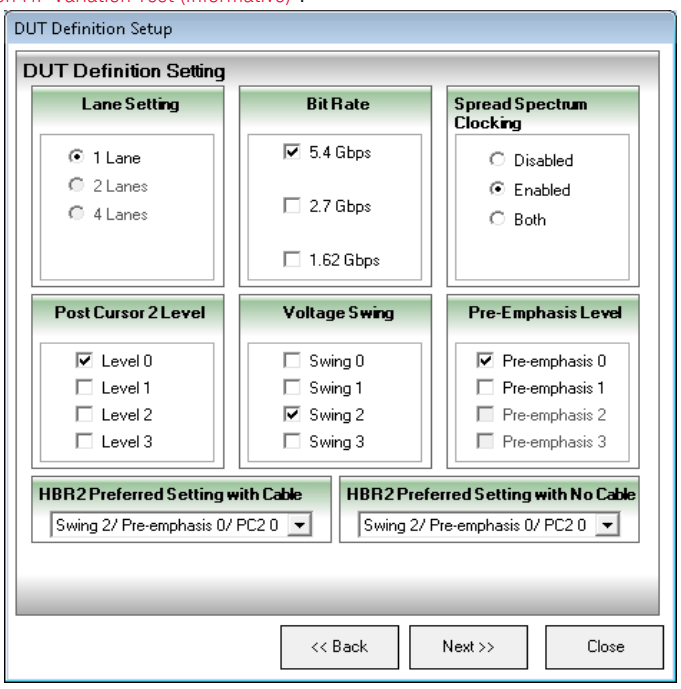
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

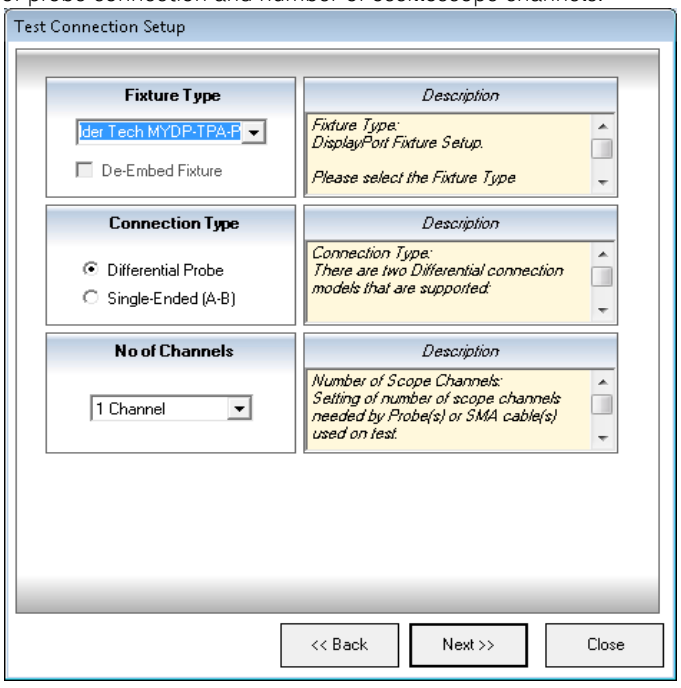
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

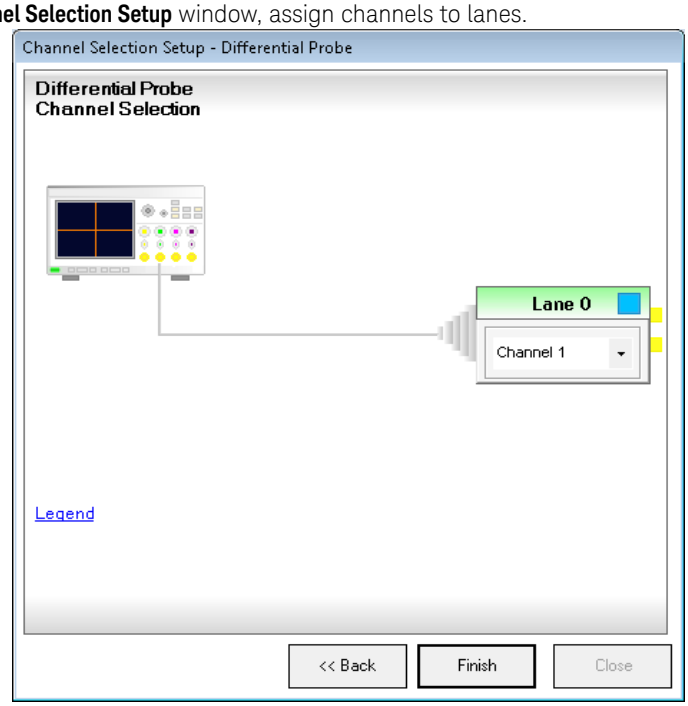
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Deviation HF Variation Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

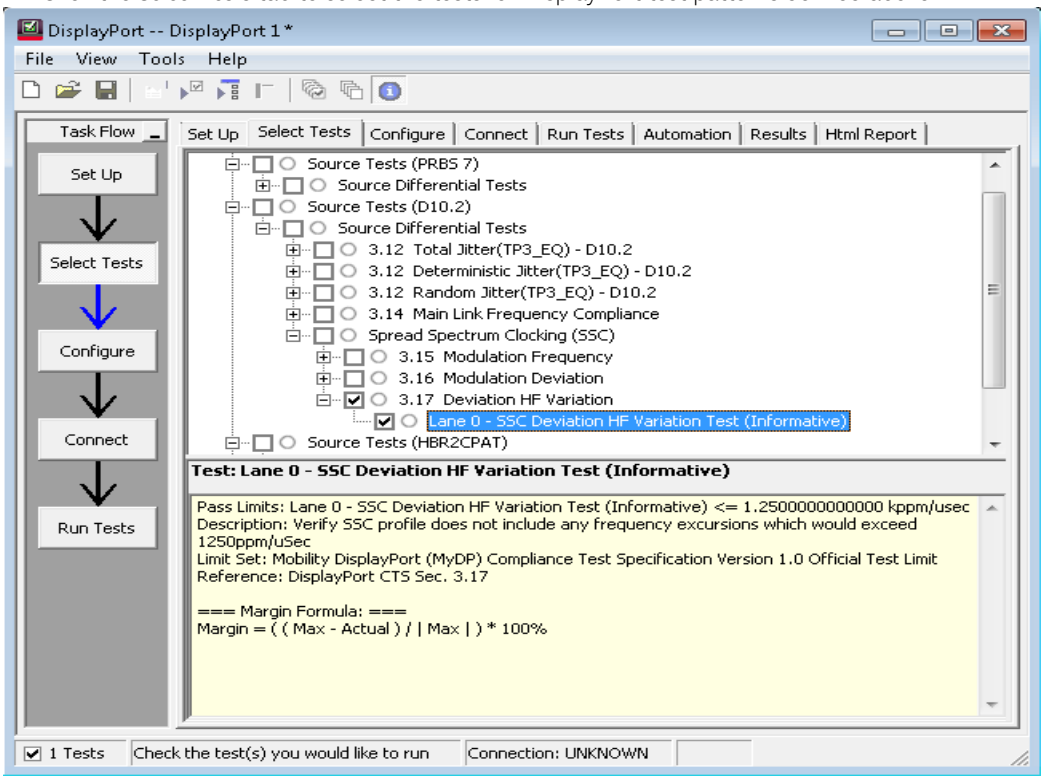


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
6 Set up the parameters for the SSC measurement.
   a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.
   b Acquire the signal with one complete SSC Cycles.
   c Read the FUNC2 filtered unit interval measurement trend.
   d Compute the slope using the “Sliding Window” with 1.00 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t\text{-}1.00\ \mu\text{sec})/1.00\ \mu\text{sec}]$$

   e Repeat step b, c and d until you acquire 10 SSC Cycles.
   f Get the maximum value for the computed value of slope.
7 Report the measurement results.

PASS Condition

- SSC_t dF/dt $\leq$ 1250ppm/µsec

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.17*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Post-Cursor 2 Verification Test (Informative)

Test ID

1279001 – Post Cursor 2 Verification Test - Level 1/Level 0 (Informative)

1279101 – Post Cursor 2 Verification Test - Level 2/Level 1 (Informative)

1279201 – Post Cursor 2 Verification Test - Level 3/Level 2 (Informative)

Test Overview

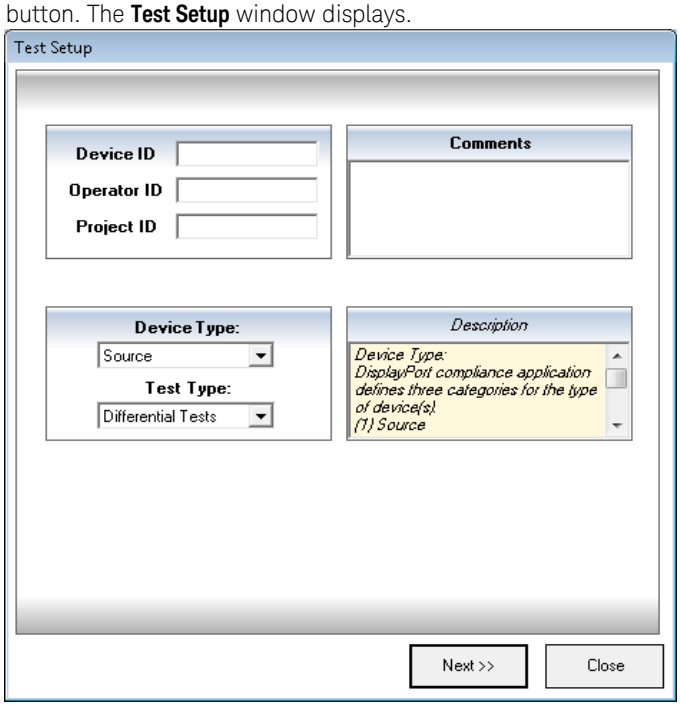
The objective of this test is to evaluate the effect of adding Post-Cursor 2 of the source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor 2 settings.

Test Conditions for Post-Cursor 2 Verification Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR2
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	All Post-Cursor 2 levels supported
Test Lane	Lane 0
Test Pattern	PCTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



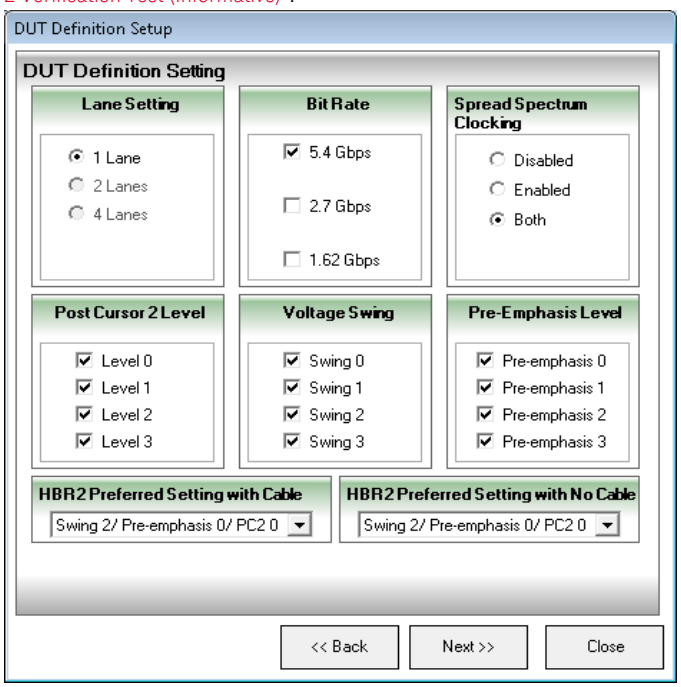
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

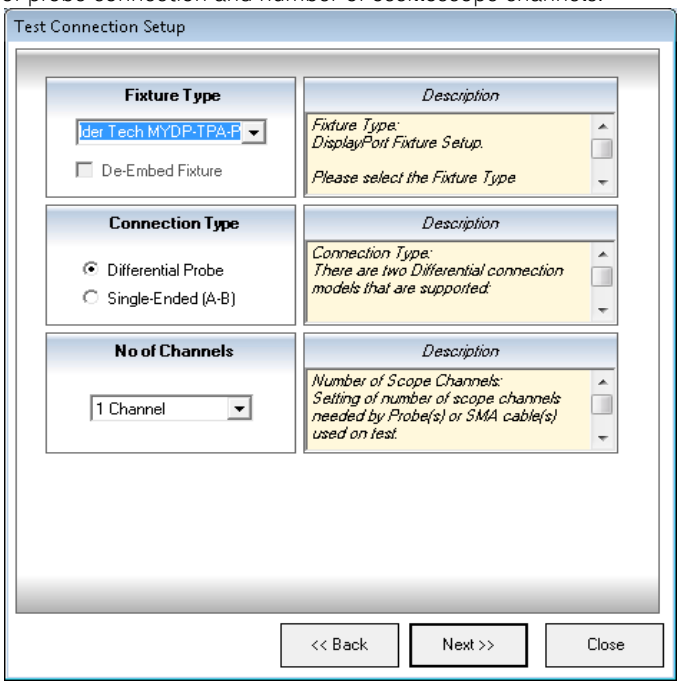
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

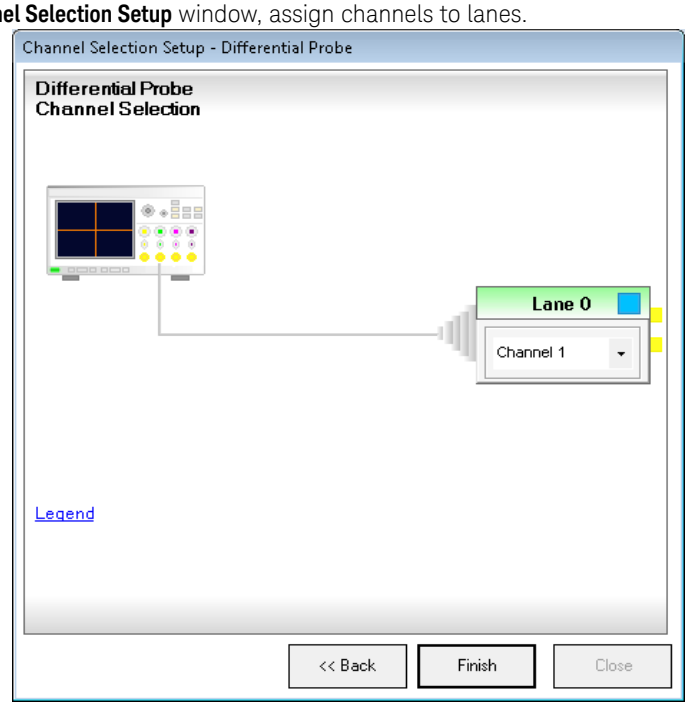
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Post-Cursor 2 Verification Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

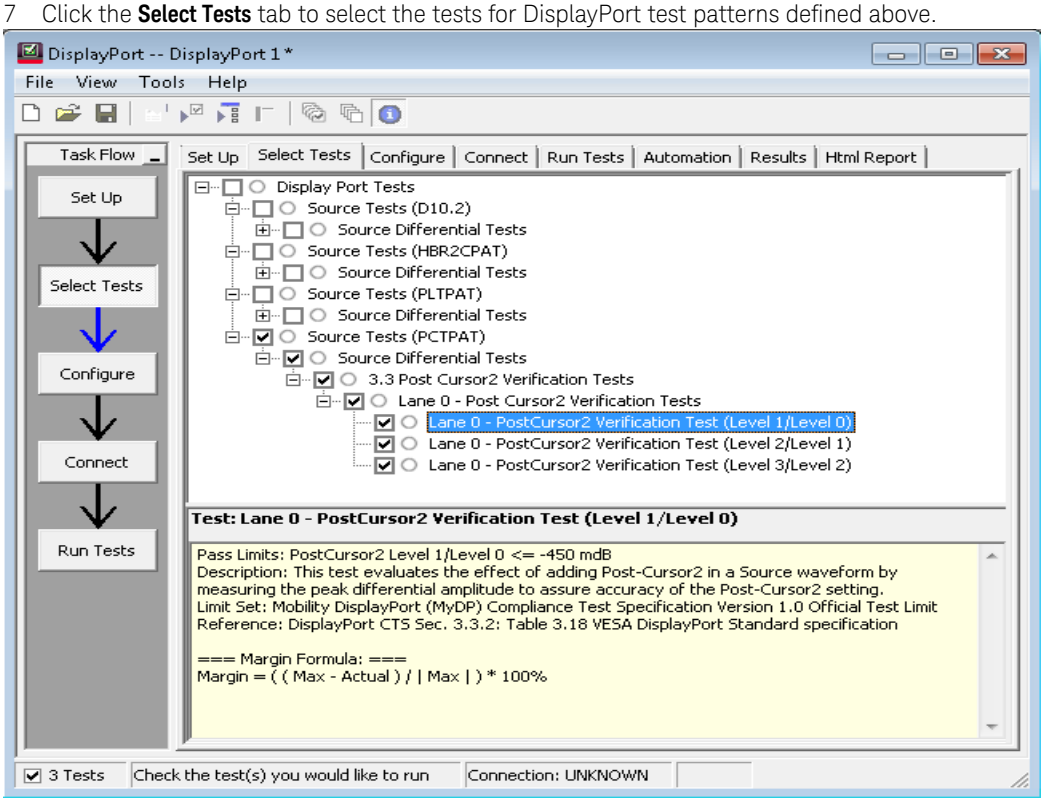


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level, Pre-Emphasis Level and Post-Cursor 2 Level X:
   a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   b Acquire and verify the input signal:
      i Verify the trigger and the amplitude of the input signal.
      ii Scale the vertical display of the input signal to optimum value.
      iii Measure V_{TOP} and V_{BASE} of the input signal.
      iv Measure the data rate of the input signal.
   c Set up the parameter of the measurement:
      i Enable measurement of all edges to obtain a statistical value of the measurement.
      ii Set up the measurement threshold.
      iii Set up the Clock Recovery as described in the section “Clock Recovery”.
   d Pattern fold the input signal based on the qualifying pattern 00101010 for the measurement of voltage $V_{T1010\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.
   e Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1010\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1010\_PC2\_LvlX\_L}$.
      i $V_{T1010\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1010 portion of the qualifying pattern.
      ii $V_{T1010\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1010 portion of the qualifying pattern.
   f Calculate the peak-to-peak voltage $V_{T1010\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1010\_PC2\_LvlX\_PP} = V_{T1010\_PC2\_LvlX\_H} - V_{T1010\_PC2\_LvlX\_L}$$

   g Pattern fold the input signal based on the qualifying pattern 00011001100 for the measurement of voltage $V_{T1100\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.
   h Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1100\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1100\_PC2\_LvlX\_L}$.
      i $V_{T1100\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1100 portion of the qualifying pattern.
      ii $V_{T1100\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1100 portion of the qualifying pattern.
   i Calculate the peak-to-peak voltage $V_{T1100\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1100\_PC2\_LvlX\_PP} = V_{T1100\_PC2\_LvlX\_H} - V_{T1100\_PC2\_LvlX\_L}$$

   j Calculate the Post-Cursor 2 ratio using the equation:

$$\text{Post-Cursor 2 Ratio}_{LvlX} = V_{T1100\_PC2\_LvlX\_PP} / V_{T1010\_PC2\_LvlX\_PP}$$

2 Compare the pre-emphasis delta of Post-Cursor 2 Level with the limits by repeating Step 1 with another Post-Cursor2 Level.
3 Calculate the pre-emphasis delta of Post-Cursor 2 Level using the equation:

$$\text{Post-Cursor 2 Delta (Level 1 vs Level 0)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl1} / \text{Post-Cursor 2 Ratio}_{Lvl0}]$$

$$\text{Post-Cursor 2 Delta (Level 2 vs Level 1)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl2} / \text{Post-Cursor 2 Ratio}_{Lvl1}]$$

$$\text{Post-Cursor 2 Delta (Level 3 vs Level 2)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl3} / \text{Post-Cursor 2 Ratio}_{Lvl2}]$$

4 Report the measurement results.

PASS Condition

Post Cursor 2 Verification Measurements

For Level 1 vs. Level 0 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl0\_to\_Lvl1} < -0.45$ dB

For Level 2 vs. Level 1 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl1\_to\_Lvl2} < -0.5$ dB

For Level 3 vs. Level 2 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl2\_to\_Lvl3} < -0.6$ dB

Table 104 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX-PREEMP\_POST2-DELTA}$	Delta of Pre-emphasis Post Cursor2 Level 1 vs. Level 0	-0.45	-	-	dB	Measured on 2nd TBIT at Pre-emphasis Level 0
	Delta of Pre-emphasis Post Cursor2 Level 2 vs. Level 1	-0.5	-	-	dB	Support for Pre-emphasis Post Cursor2 is optional
	Delta of Pre-emphasis Post Cursor2 Level 3 vs. Level 2	-0.6	-	-	dB	

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2a, Section 3.3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis delta of Post-Cursor 2 for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Eye Diagram Test (TP3_EQ)

Test ID

For HBR

- 1211001 – Eye Diagram Test (TP3_EQ)
- 1211011 – Eye Diagram Test with No Cable Model (TP3_EQ)

For HBR2

- 1215001 – Eye Diagram Test (TP3_EQ)
- 1215011 – Eye Diagram Test with No Cable Model (TP3_EQ)

Test Overview

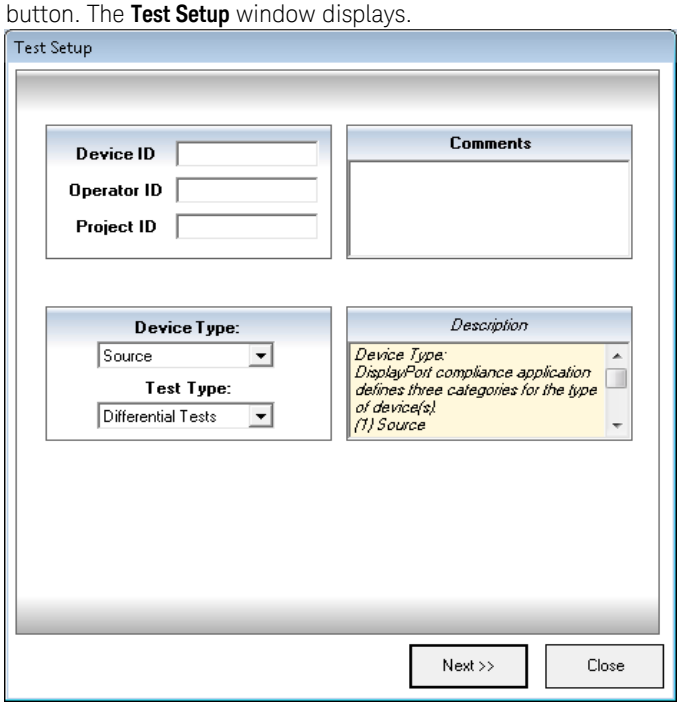
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative) and HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	HBR – Level 2 HBR2 – Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR–PRBS7 HBR2–HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



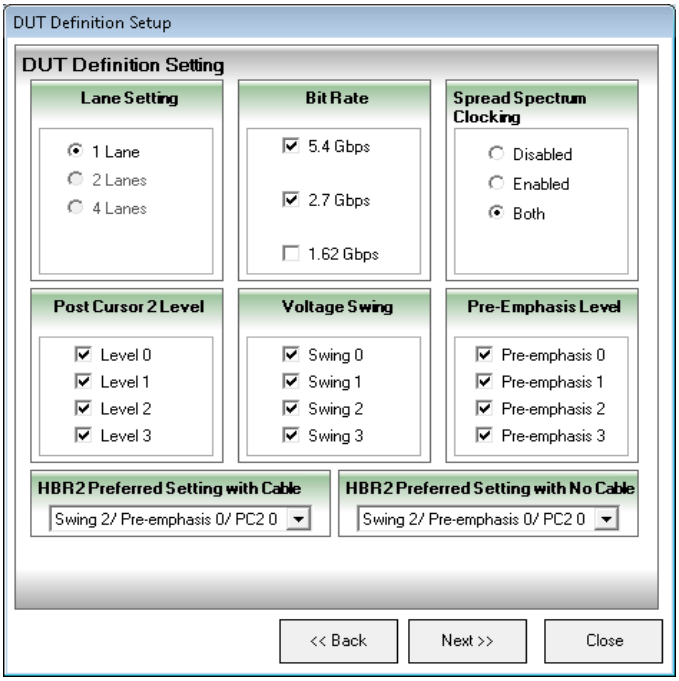
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

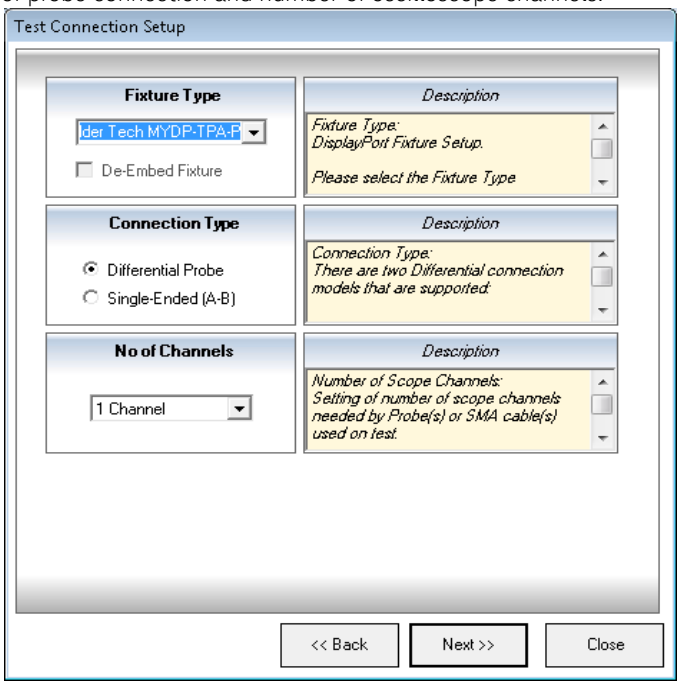
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

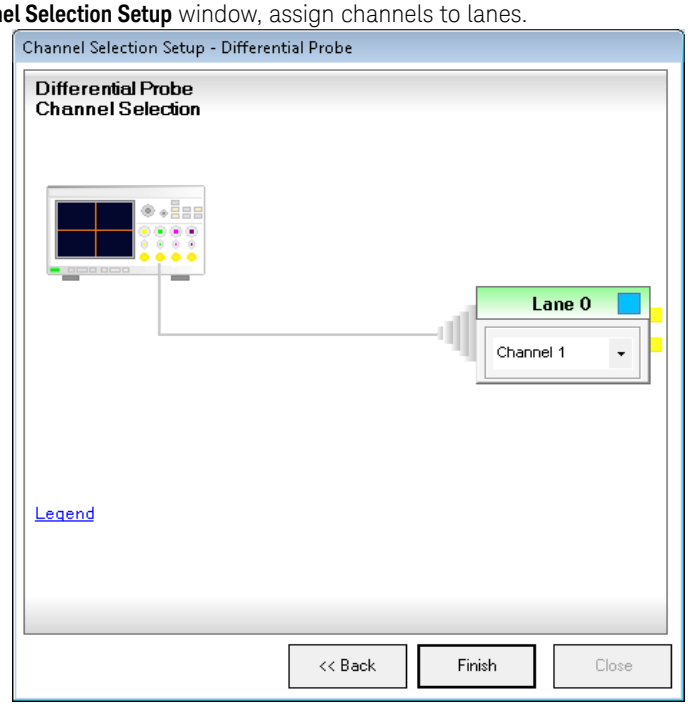
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

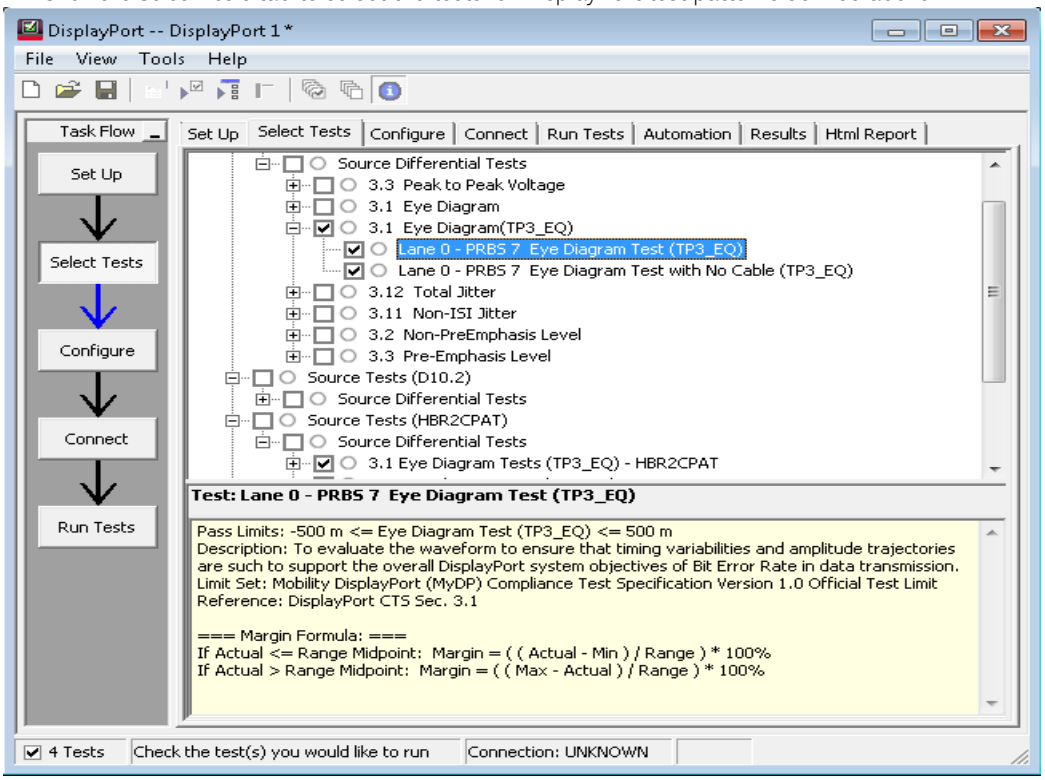


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure for HBR

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.

4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 1,000,000 edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If you select more than one lane (2 lanes or 4 lanes DUT configuration), the eye mask height and width is derate in the following manner, to include crosstalk as defined in DisplayPort 1.2b Compliance Test Specification:
      i Eye Mask Width Derate (Crosstalk) = 0.04 UI
      ii Eye Mask Height Derate (Crosstalk) = 0.014V
   b If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

c Place the eye mask height at the point of the maximum eye height found in Step 9.

d Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification (0.38 UI) + Eye Mask Width Derate (Crosstalk) + 2 * Eye Mask Width Derate (Random Jitter)

e Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification (0.09 UI) + Eye Mask Height Derate (Crosstalk)}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification (0.09 UI) + Eye Mask Height Derate (Crosstalk)}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 1,000,000 UI are folded.

13 Measure the eye height of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 105 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 105 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

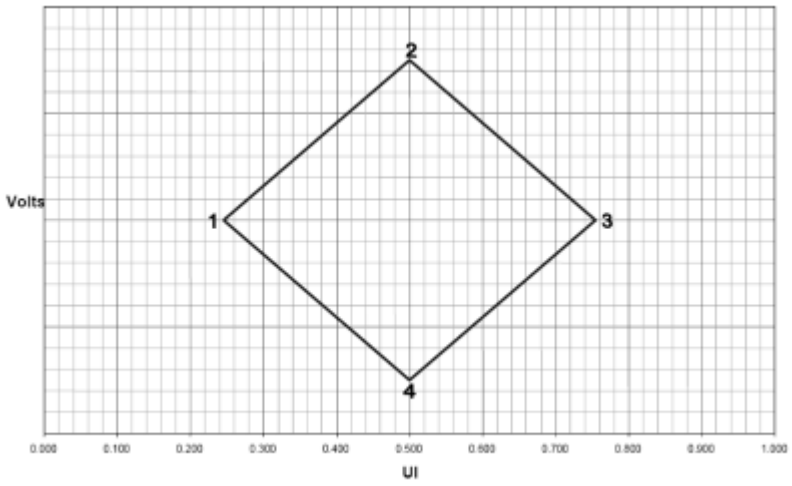


Figure 113 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 106 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045

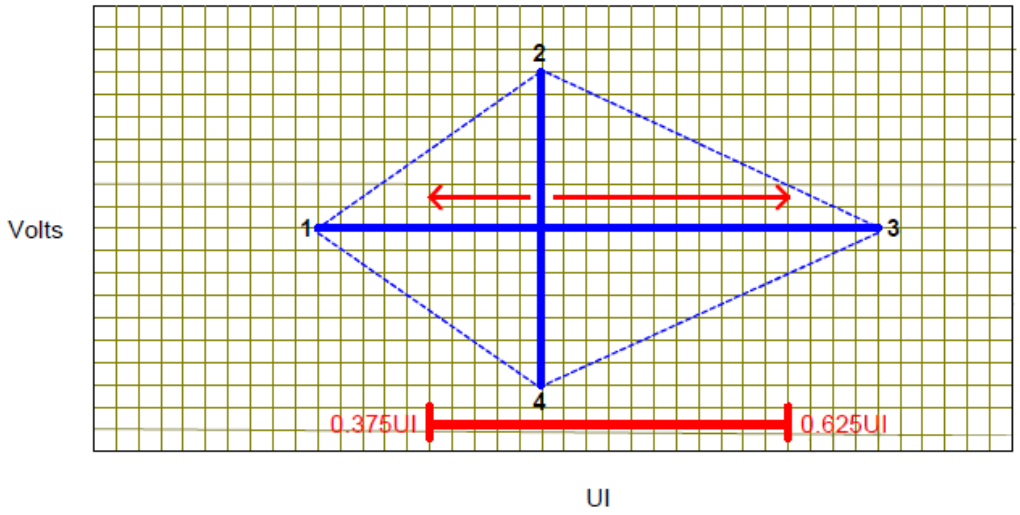


Figure 114 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Total Jitter Test (TP3_EQ)

Test ID

For HBR2:

- 1222001 – Total Jitter Test (TP3_EQ) – HBR2CPAT
- 1222011 – Total Jitter Test with No Cable Model (TP3_EQ) – HBR2CPAT
- 1221001 – Total Jitter Test (TP3_EQ) – D10.2
- 1221011 – Total Jitter Test with No Cable Model (TP3_EQ) – D10.2

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

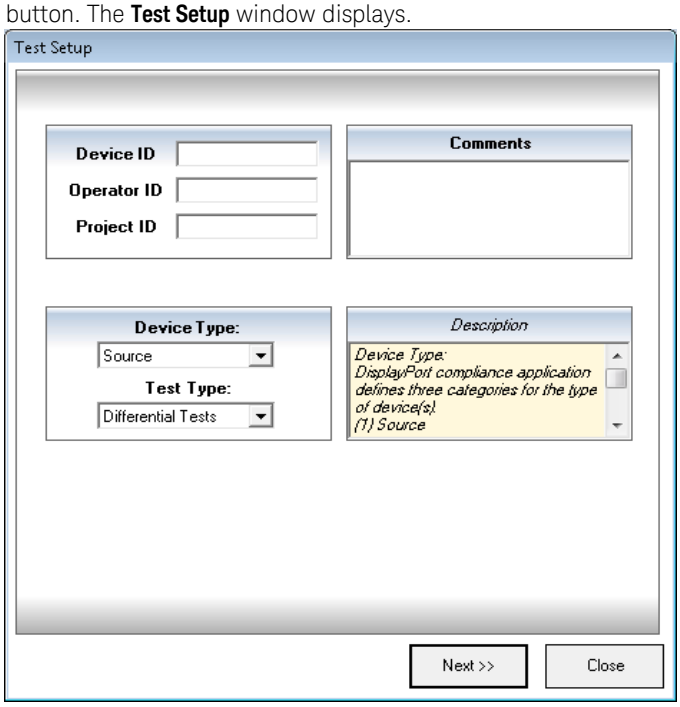
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



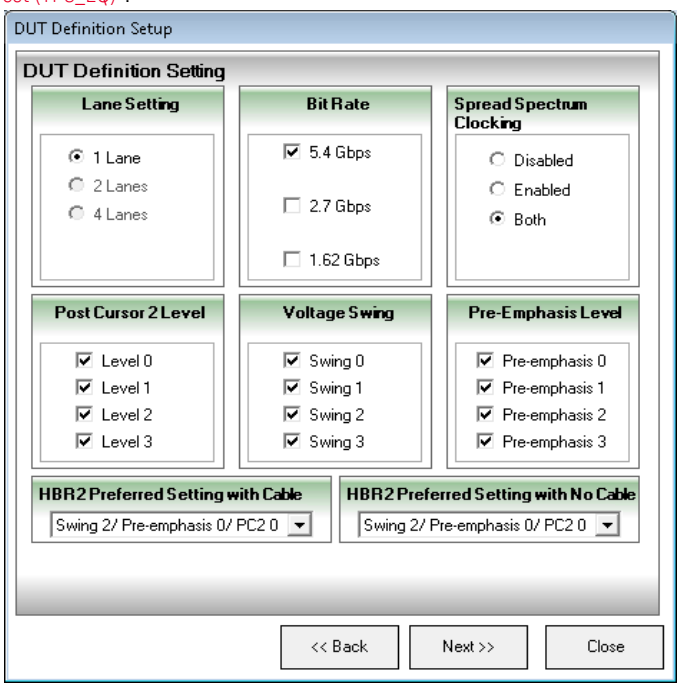
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

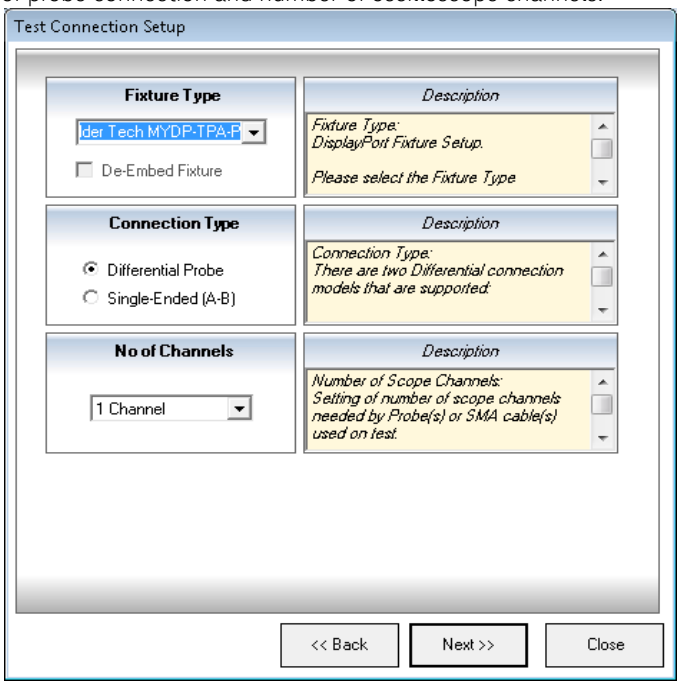
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

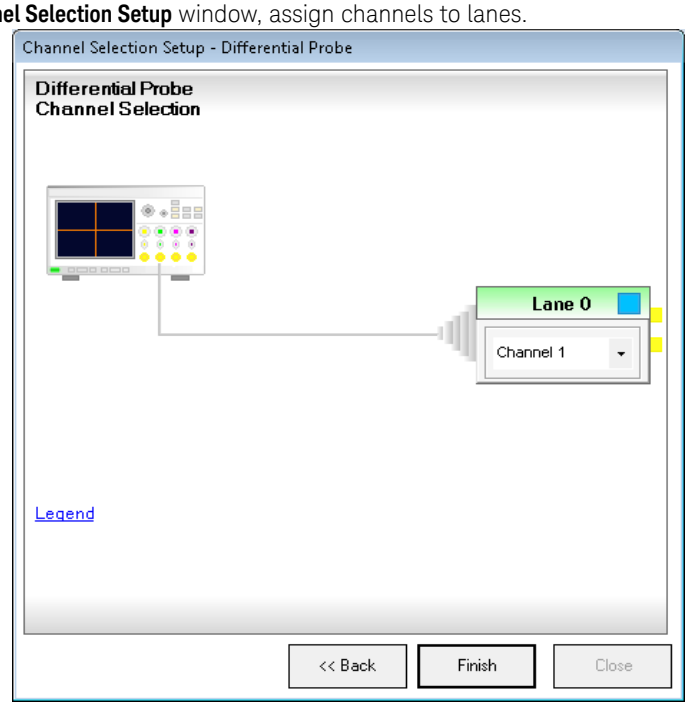
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

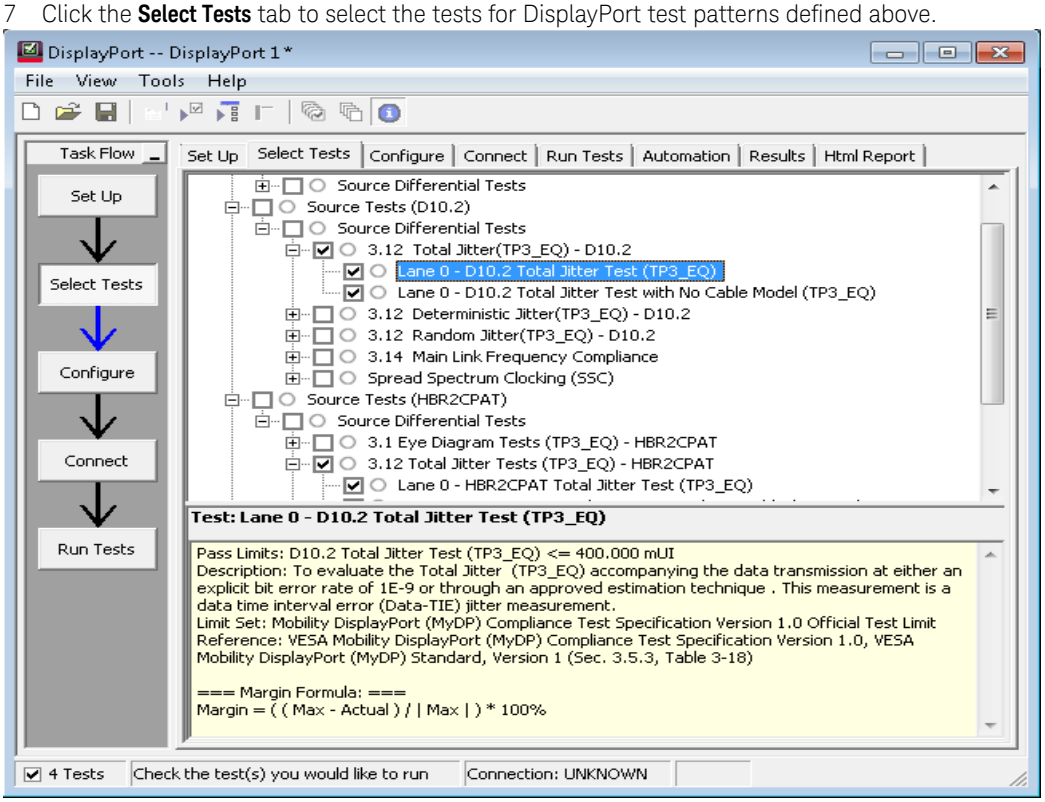


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 107 Total Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 108 Total Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.40 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22

For D10.2

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Deterministic Jitter Test (TP3_EQ)

Test ID

For HBR2:

- 1236001 – Deterministic Jitter Test (TP3_EQ) – HBR2CPAT
- 1236011 – Deterministic Jitter Test with No Cable Model (TP3_EQ) – HBR2CPAT
- 1235001 – Deterministic Jitter Test (TP3_EQ) – D10.2
- 1235011 – Deterministic Jitter Test with No Cable Model (TP3_EQ) – D10.2

Test Overview

The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

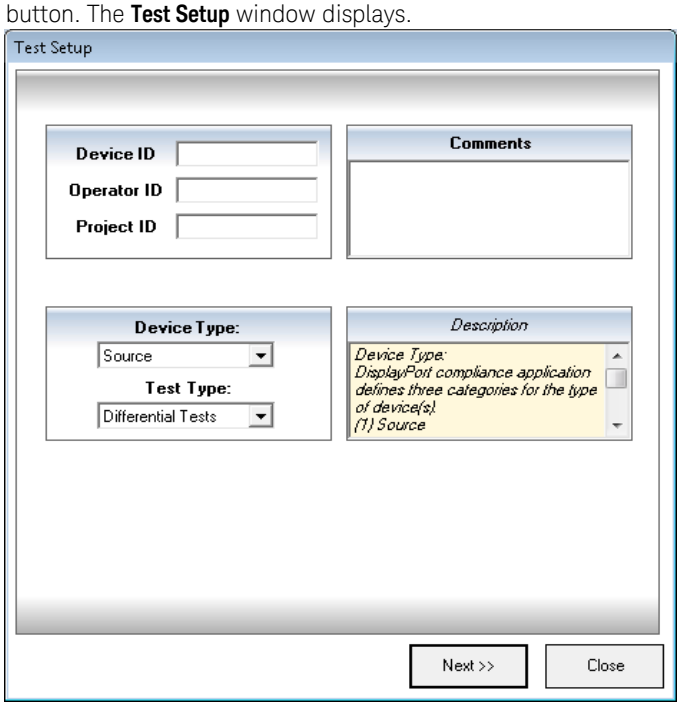
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



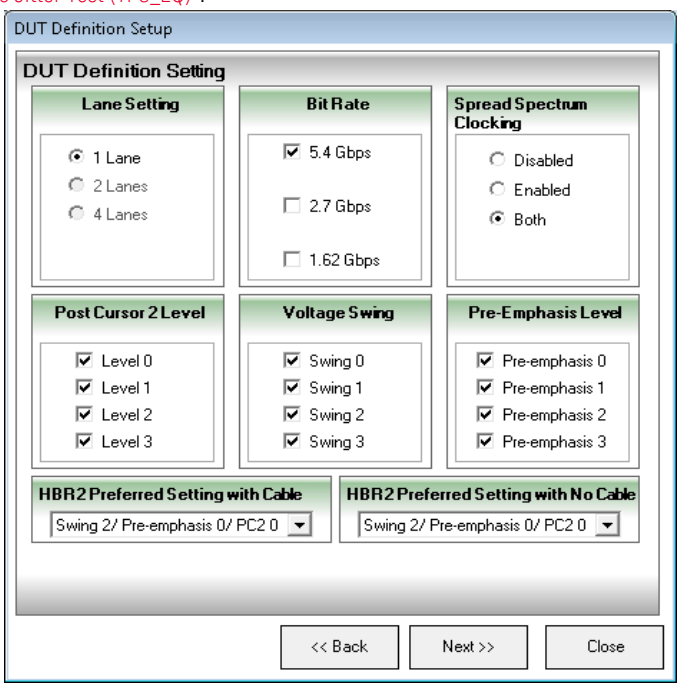
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

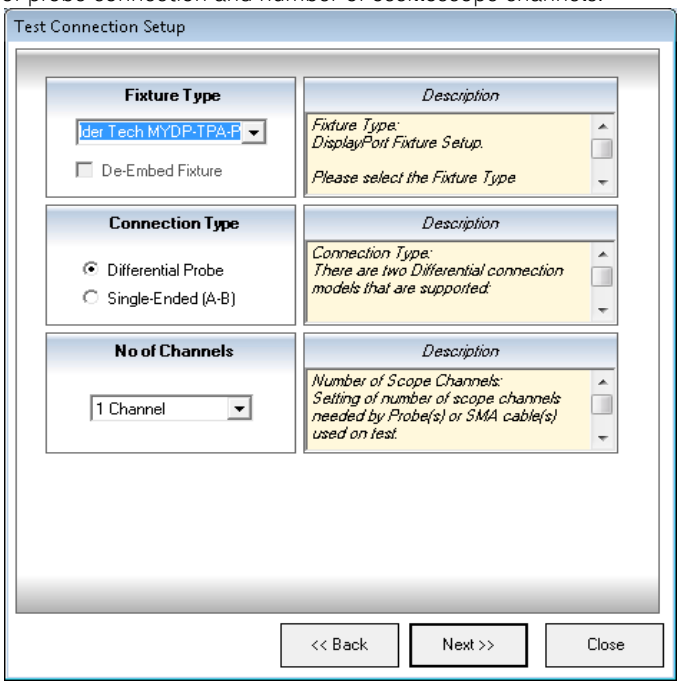
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

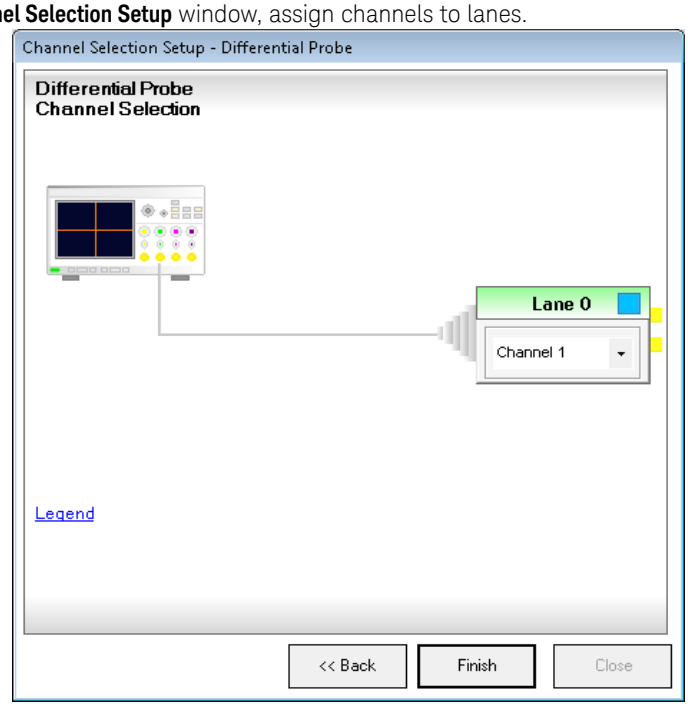
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Deterministic Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

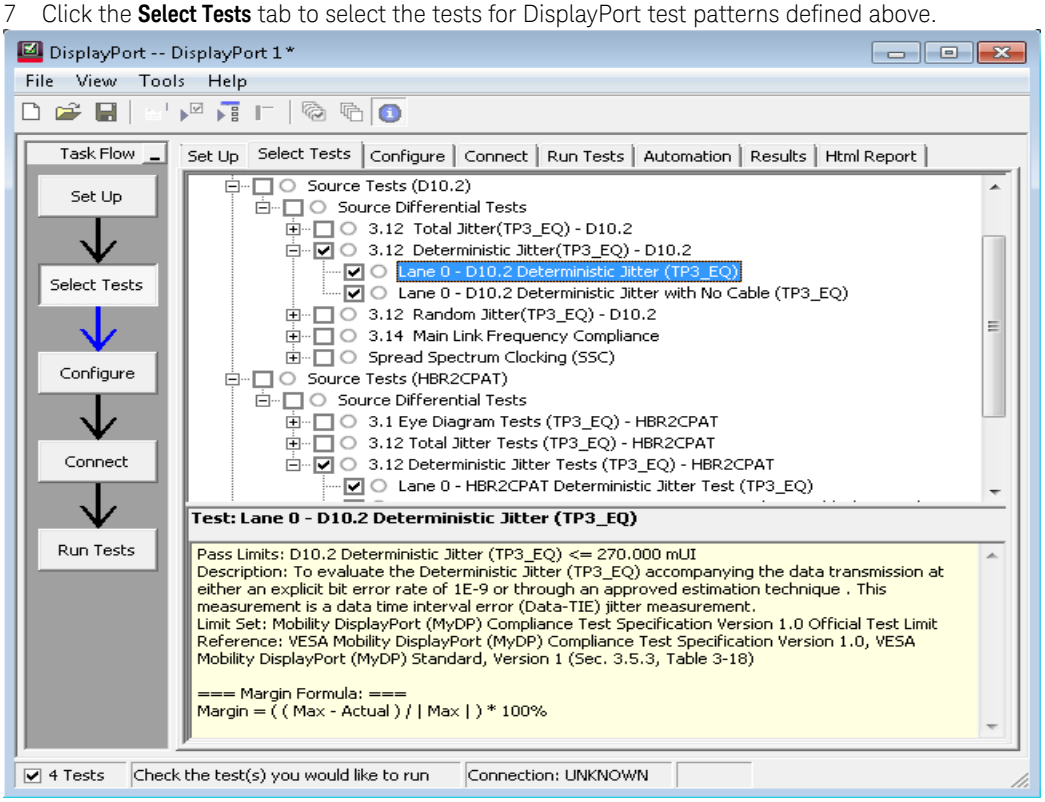


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 109 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 110 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.25 UI

UI is Unit Interval.

Test References

See:

For HBR2CPAT

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Random Jitter Test (TP3_EQ)

Test ID

For HBR2:

- 1238001 – Random Jitter Test (TP3_EQ) – D10.2
- 1238011 – Random Jitter Test with No Cable Model (TP3_EQ) – D10.2

Test Overview

The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

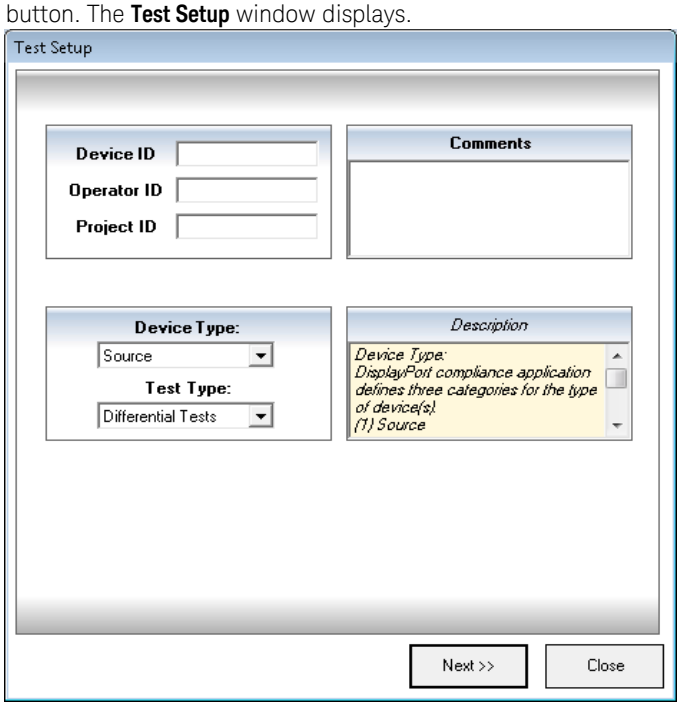
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



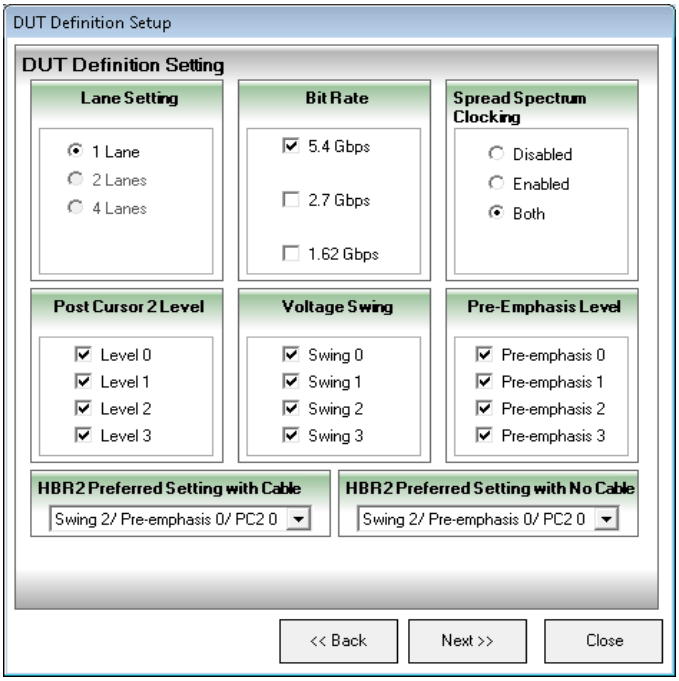
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

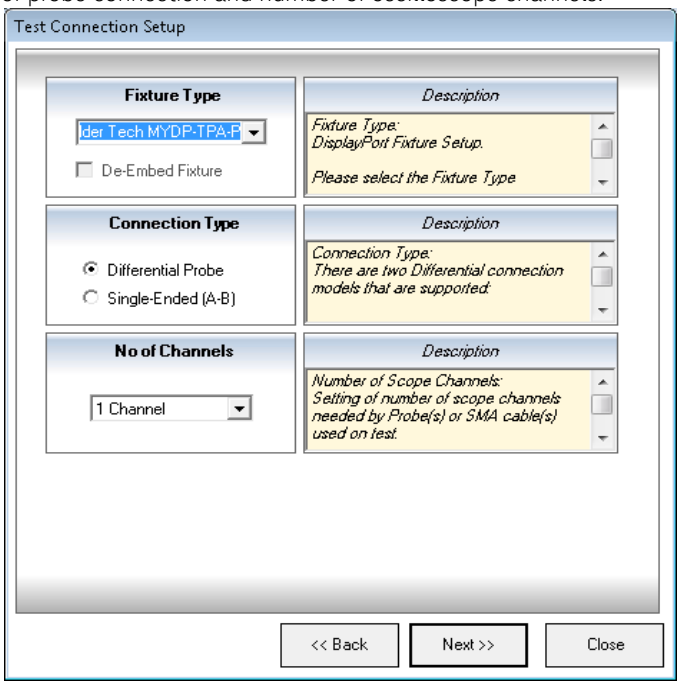
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

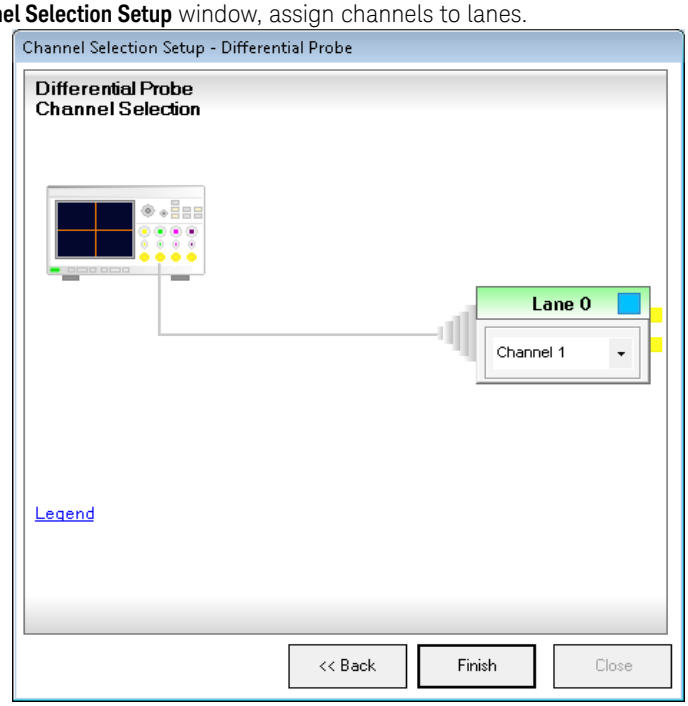
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Random Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

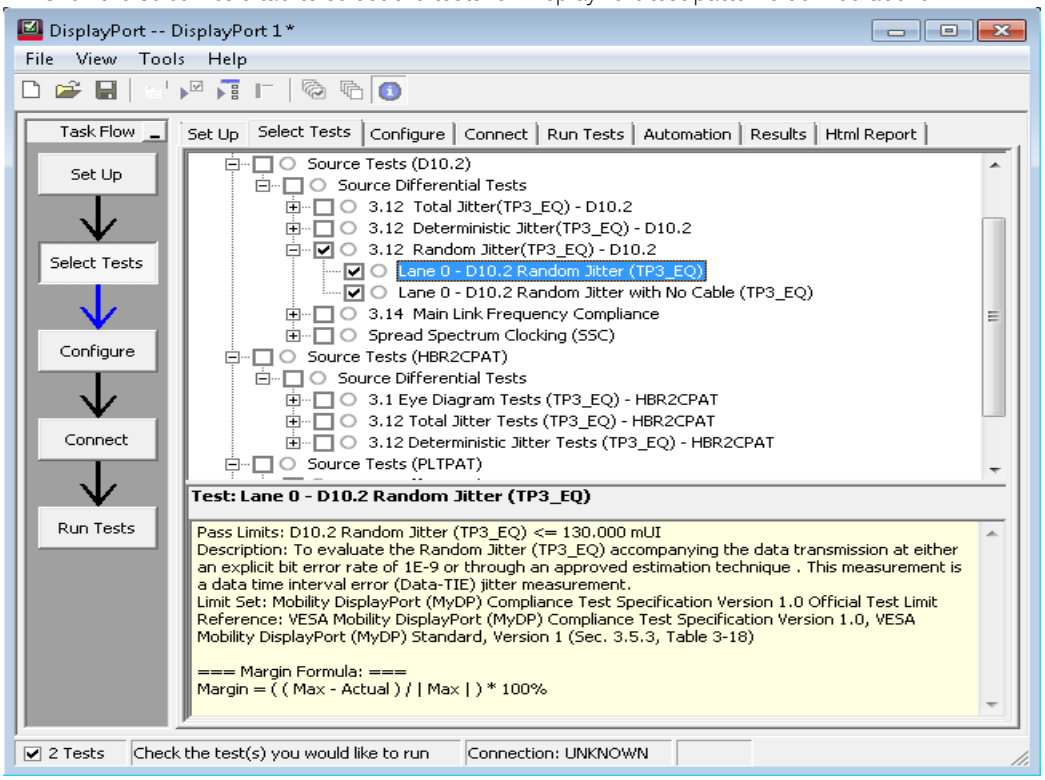


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 111 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.23 UI

UI is Unit Interval.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AC Common Mode Test (Informative)

Test ID

12110001 – AC Common Mode Test (Informative)

Test Overview

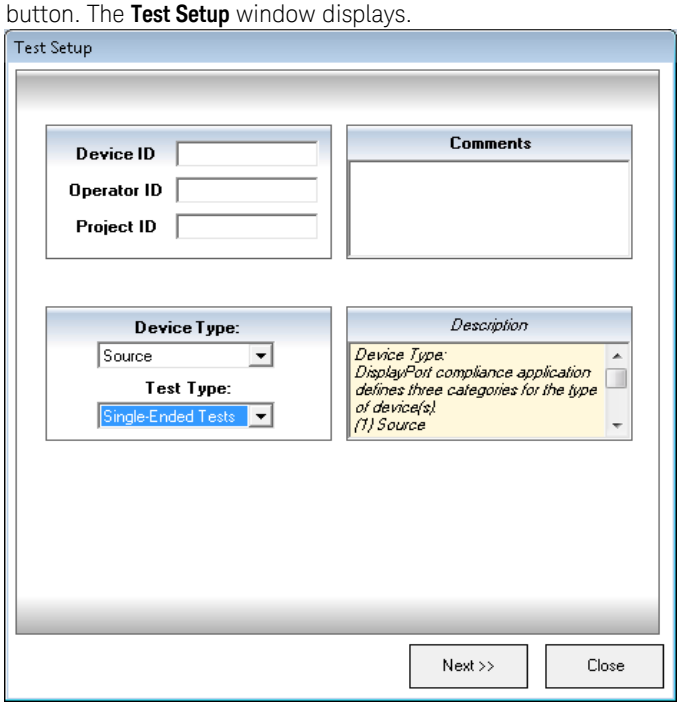
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates are supported (RBR, HBR, HBR2)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis level supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



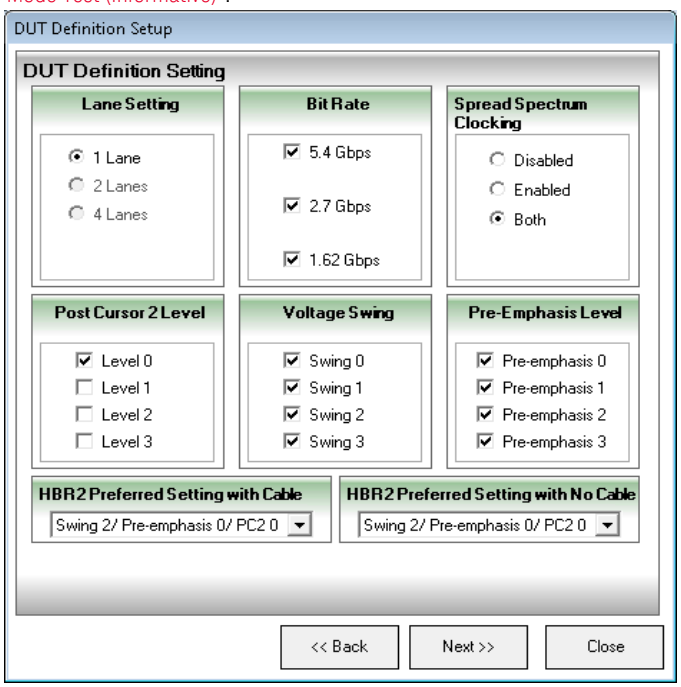
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

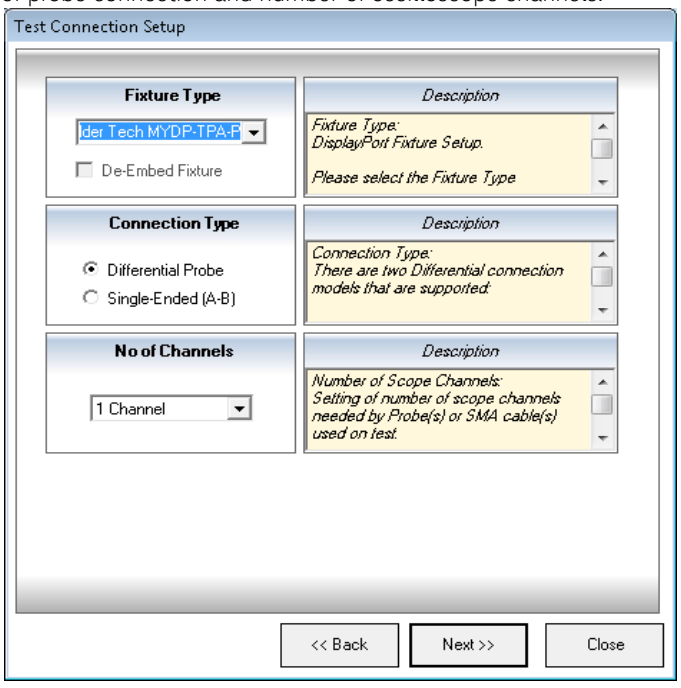
b Select **Device Type:** as **Source**, **Test Type:** as **Single-Ended Tests**.

c Click **Next**.

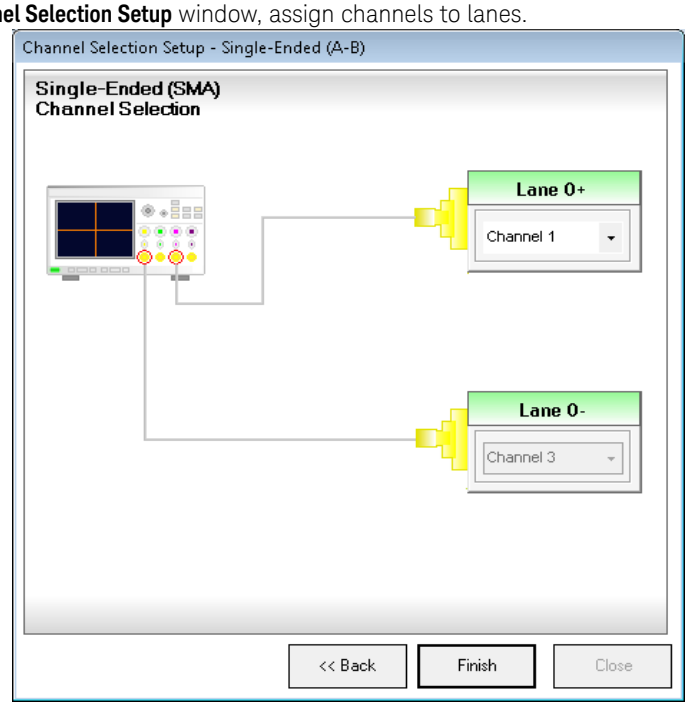
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for AC Common Mode Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

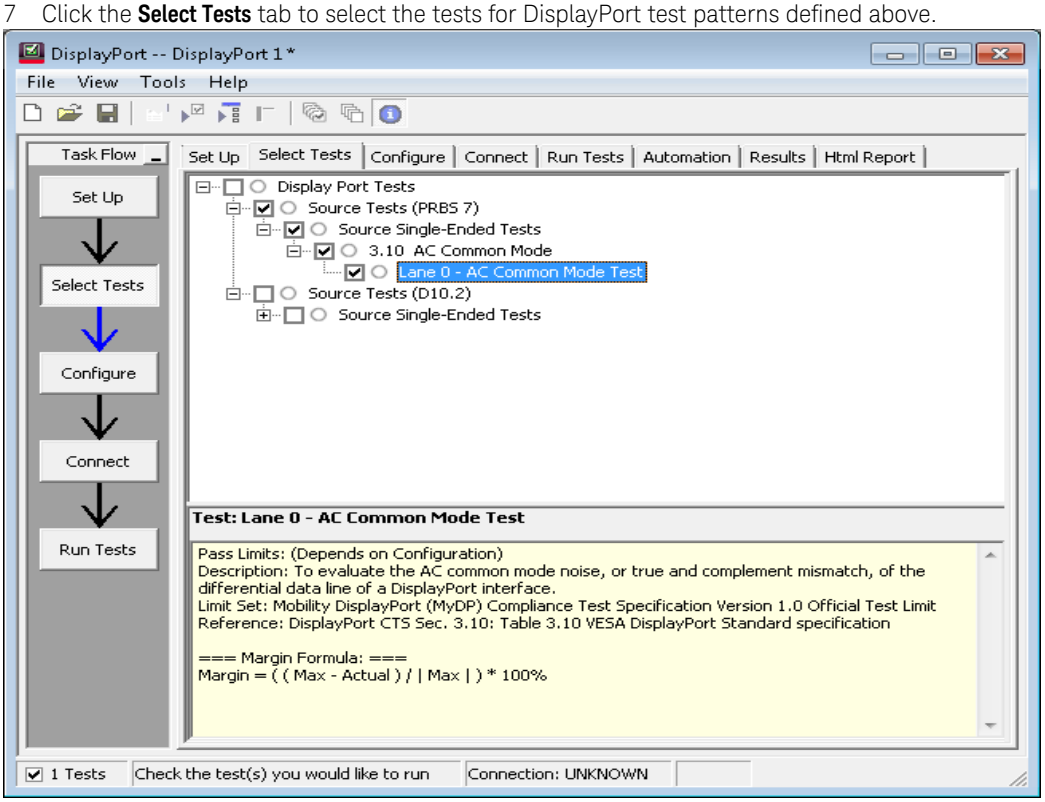


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled ["Filter" configuration variable set to "High Pass Filter", "Low Pass Filter" or "None" (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.
8 Get the mean for the V_{rms} measurement.
9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.10*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 9.2, Table 9-6*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

Intra-Pair Skew Test (Informative)

Test ID

12100001 — Intra-Pair Skew Test (Informative)

Test Overview

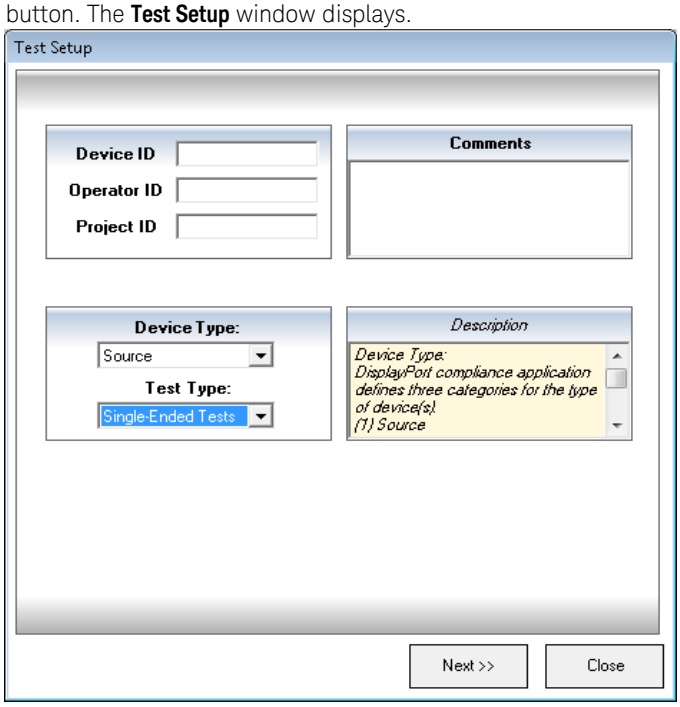
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR or HBR2)
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0 (Lane 0+ to Lane 0-)
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



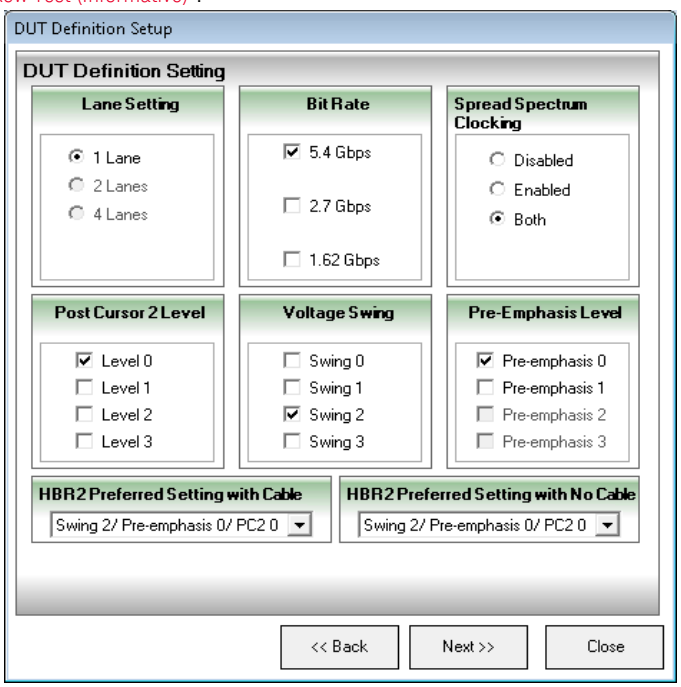
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

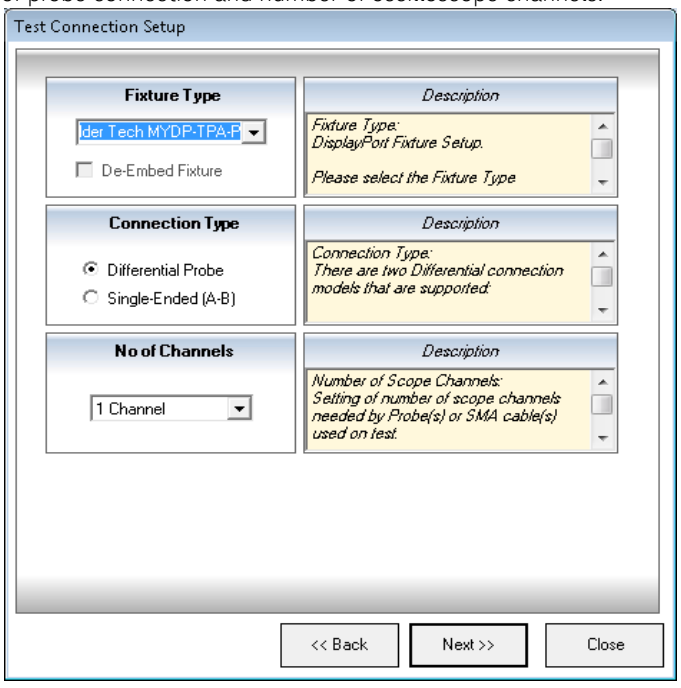
b Select **Device Type:** as **Source**, **Test Type:** as **Single-Ended Tests**.

c Click **Next**.

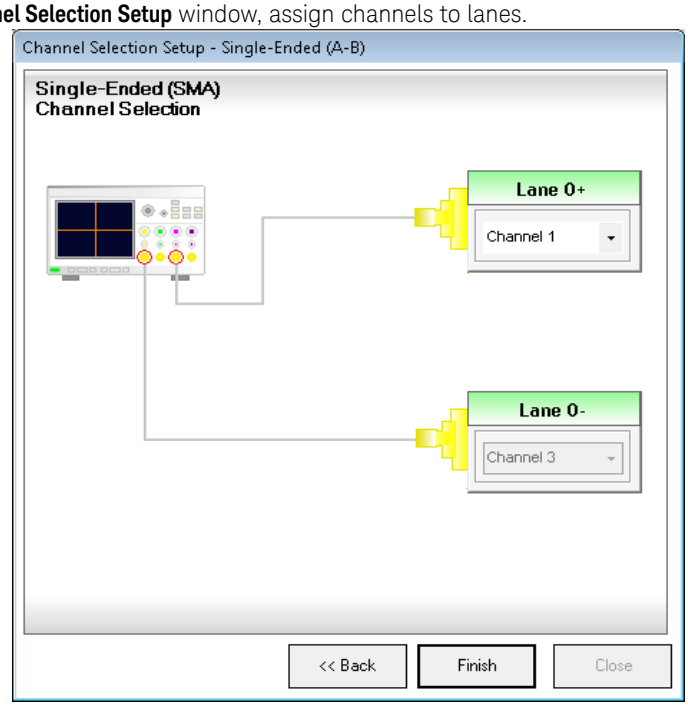
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Intra-Pair Skew Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

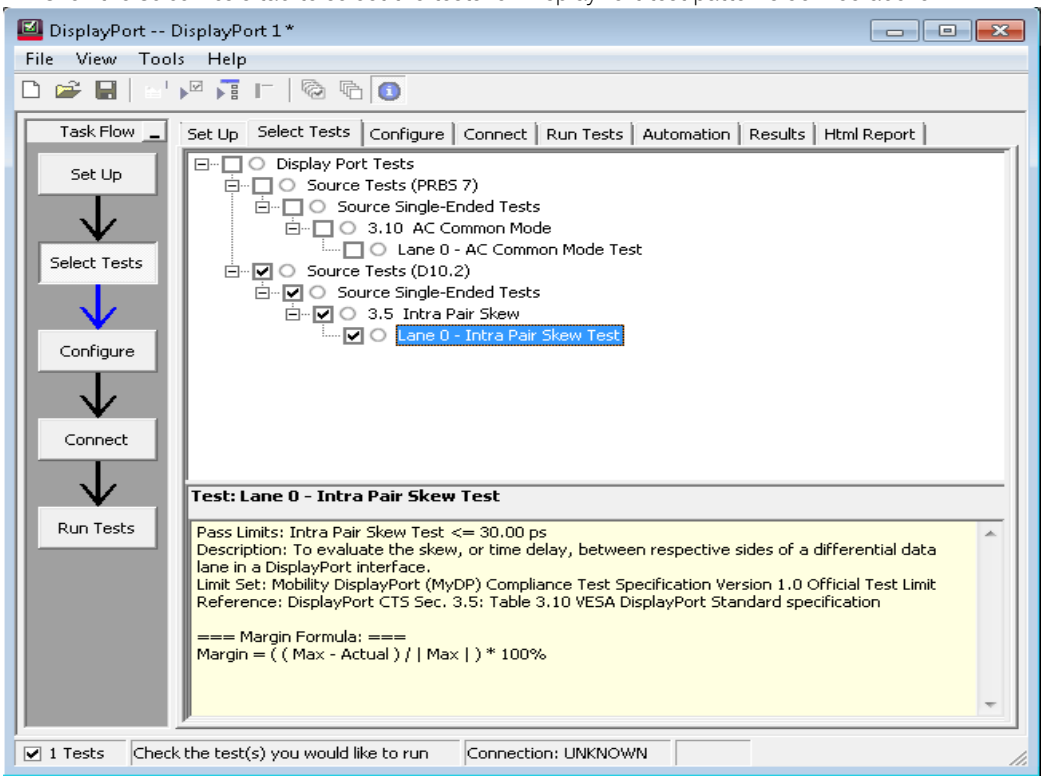


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for DisplayPort MyDP 1.0 Source Tests" on page 513 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find V_{HIGH} by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find V_{LOW} by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:
   a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.
   b Set up InfiniiScan to trigger on the desired pattern.
   c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

   d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

   e Acquire the signal until you measure 100 edges.
   f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra-Pair Skew ≤ 30 ps

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.5*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

16 MyDP 1.0 Sink Tests

Overview

Test Point Definition for DisplayPort MyDP 1.0 Sink Tests

NOTE Sink Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Sink DUT at Test Point 3(TP3) as shown in Figure 115. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

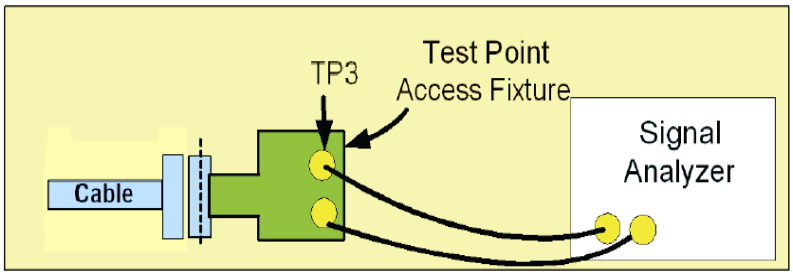


Figure 115 Test Point 3 Connection for MyDP 1.0 Sink Tests

Table 112 defines the test point fixtures and instruments used for MyDP 1.0 Sink Tests:

Table 112 Test Point Fixtures and Instruments for MyDP 1.0 Sink Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Calibration of Stress Signal

For the calibration of the stress signal, you must test the stress signal in the manner shown in the Figure 116 for RBR and Figure 117 for HBR and HBR2.

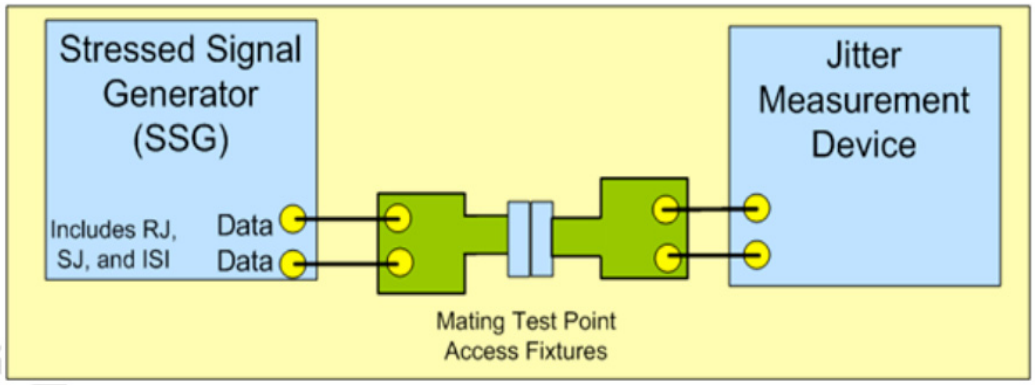


Figure 116 Test Point 3 Connection for Stress Signal Calibration of RBR

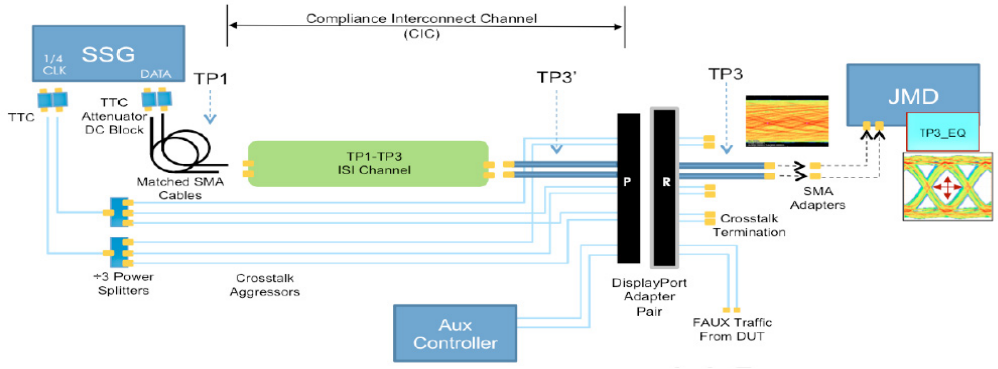


Figure 117 Test Point 3 Connection for Stress Signal Calibration of HBR and HBR2

Table 113 defines the Test Point 3 Connections for Stress Signal Calibration:

Table 113 Test Point Connections for Stress Signal Calibration

Test Requirement	Device Used
Stress Signal Generator (SSG)	Bit Error Rate Tester ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Jitter Measurement Device (JMD)	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Sink Tests

Perform the following steps before you run the compliance tests on the sink device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 118).

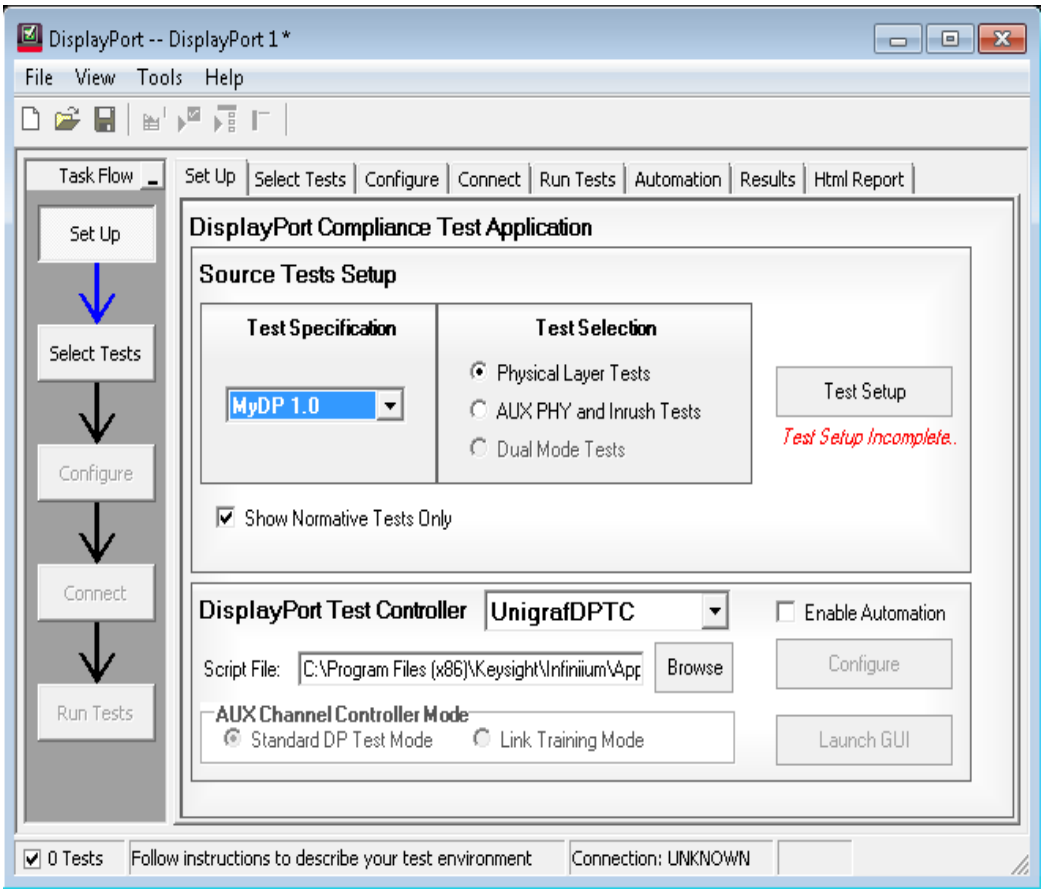


Figure 118 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with Mobility DisplayPort 1.0 Standards, select **MyDP 1.0** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for MyDP 1.0 Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

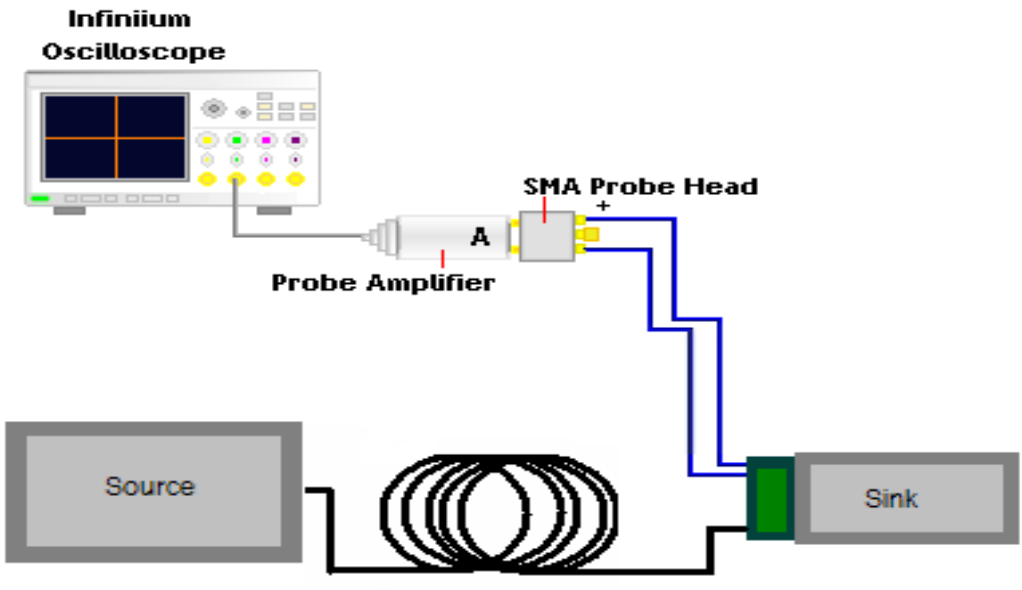


Figure 119 Sample connection diagram for MyDP 1.0 Sink Tests

Sink Eye Diagram Test

Test ID

12140001 — Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a

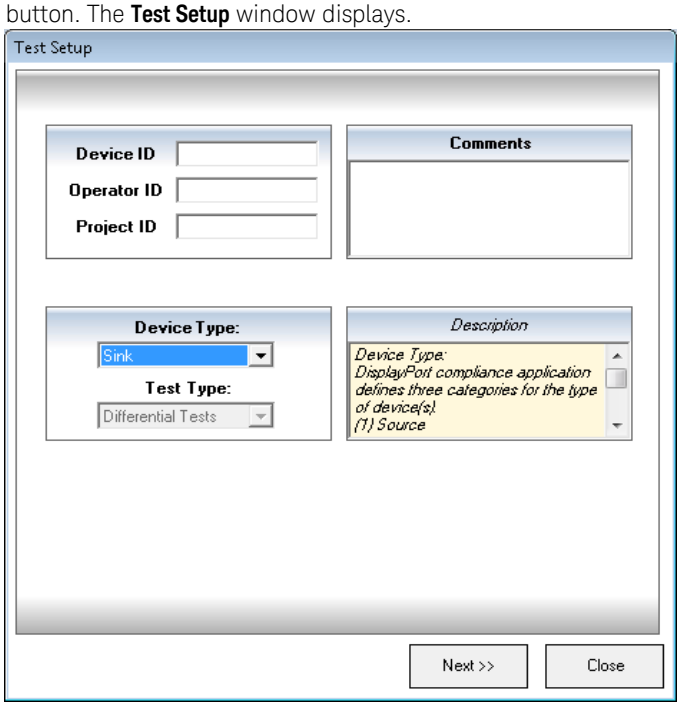
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



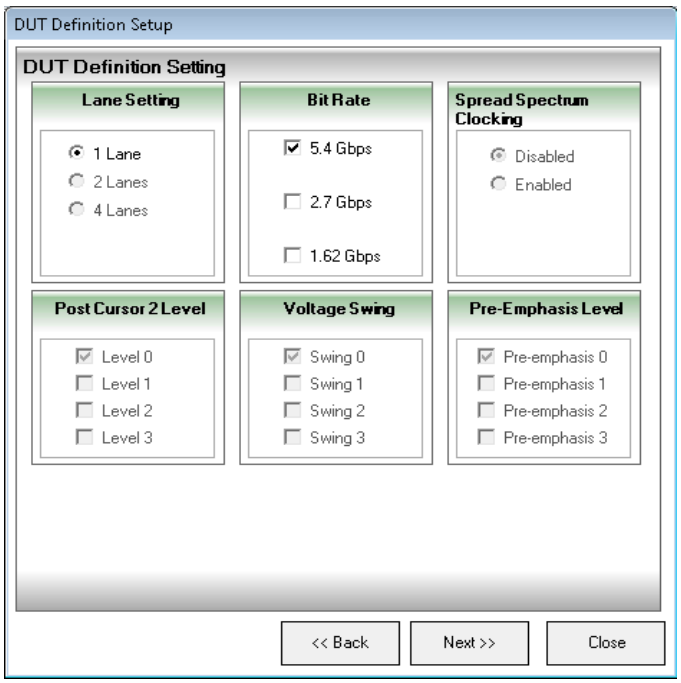
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

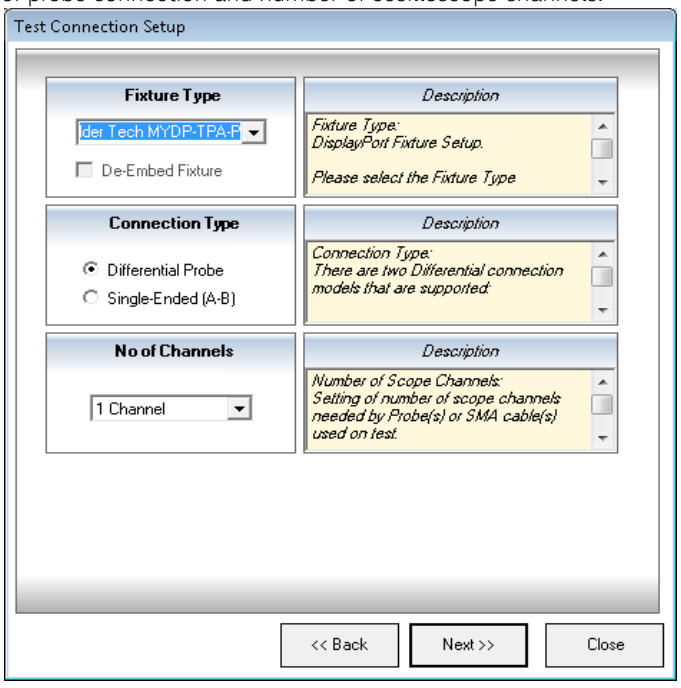
b Select **Device Type:** as **Sink**, **Test Type:** automatically grays out.

c Click **Next**.

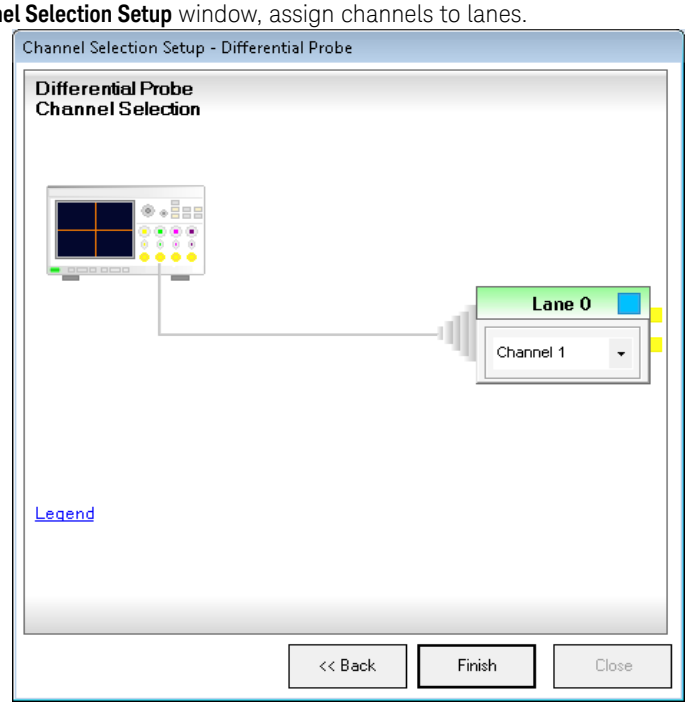
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

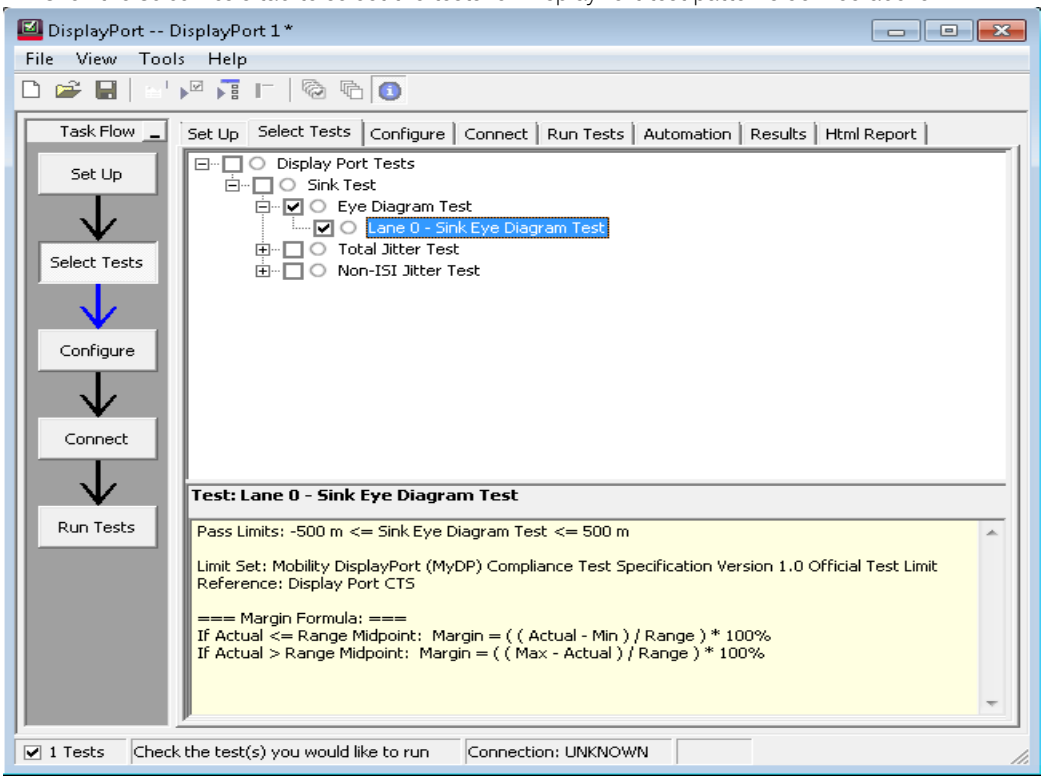


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Sink Tests" on page 632 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 114 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 114 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

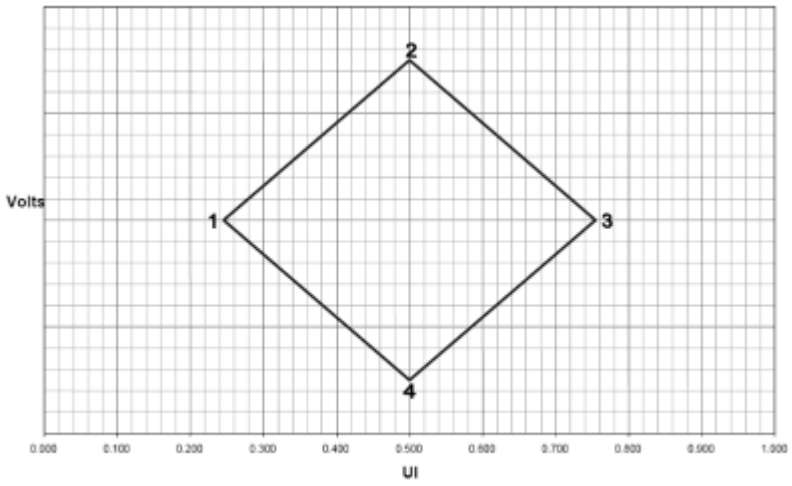


Figure 120 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 115 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045

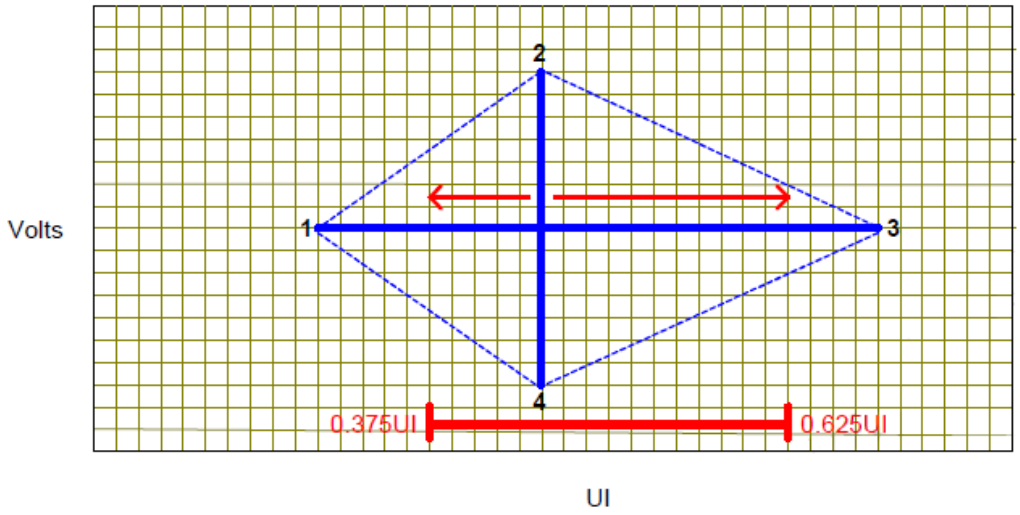


Figure 121 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

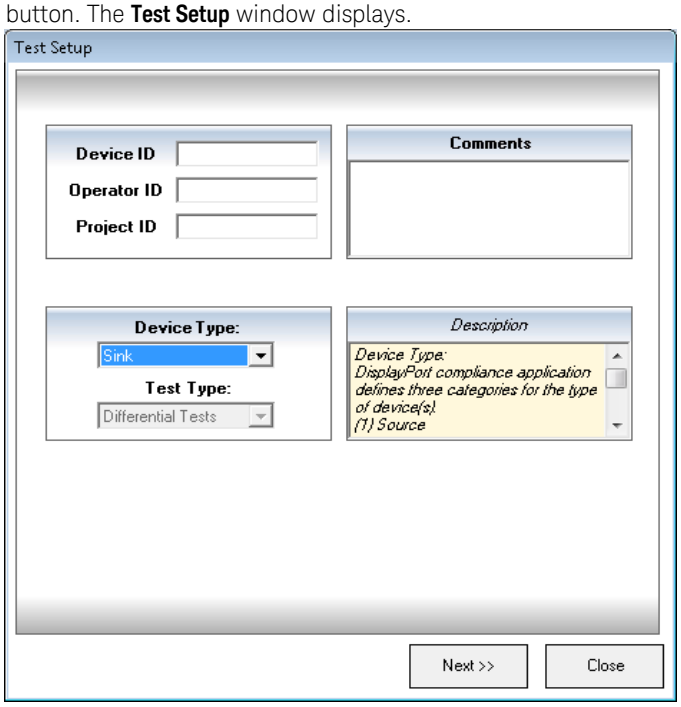
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



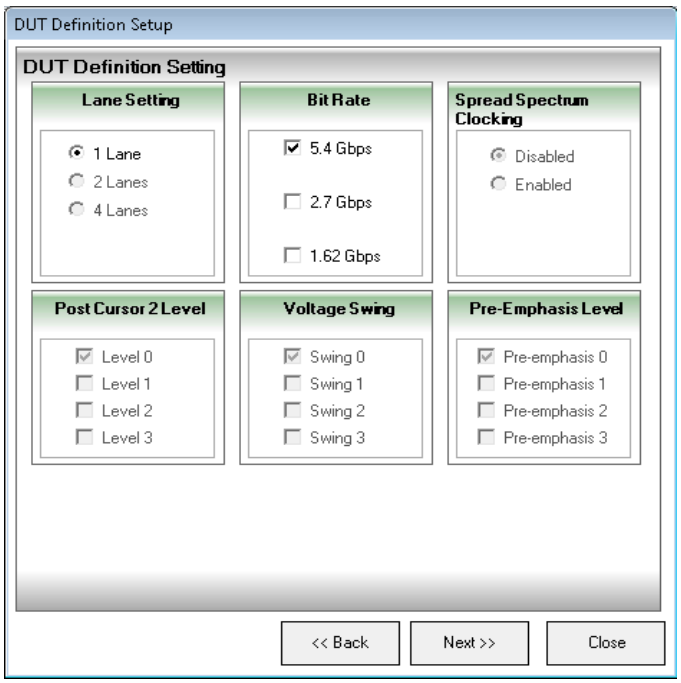
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

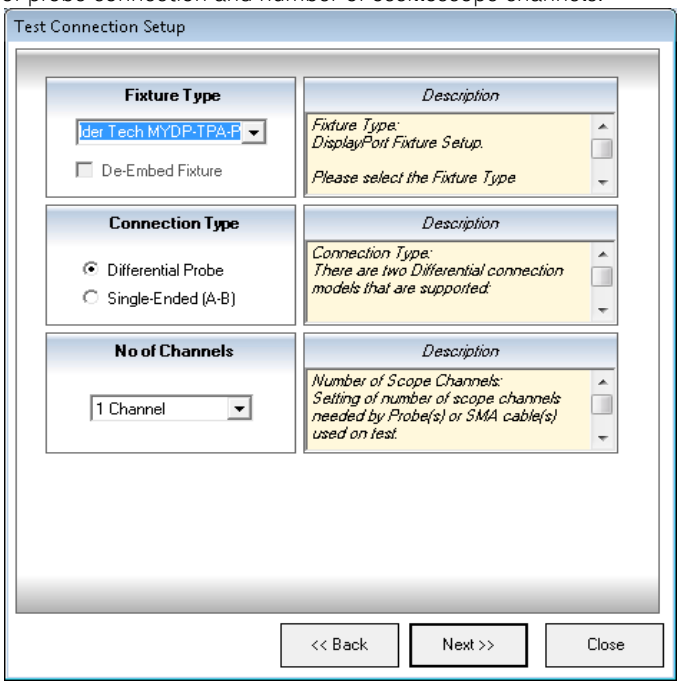
b Select **Device Type:** as **Sink**, **Test Type:** automatically grays out.

c Click **Next**.

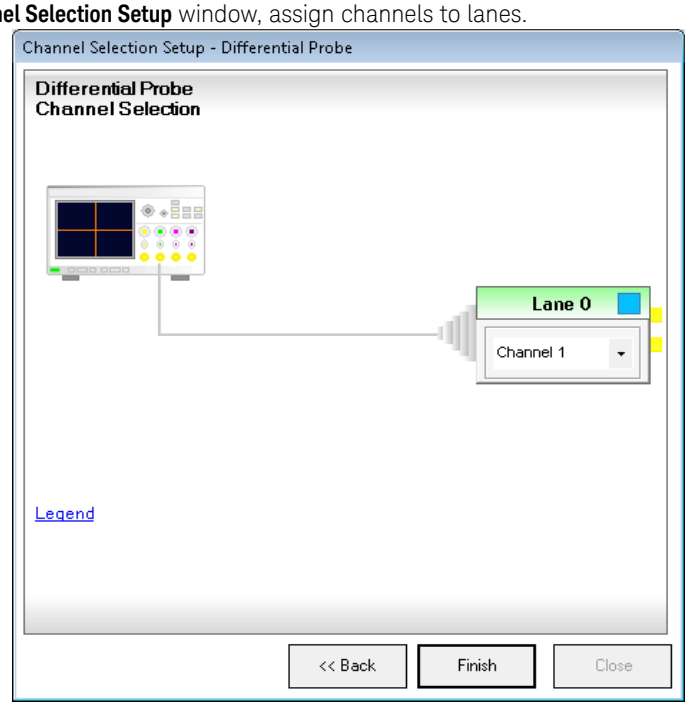
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

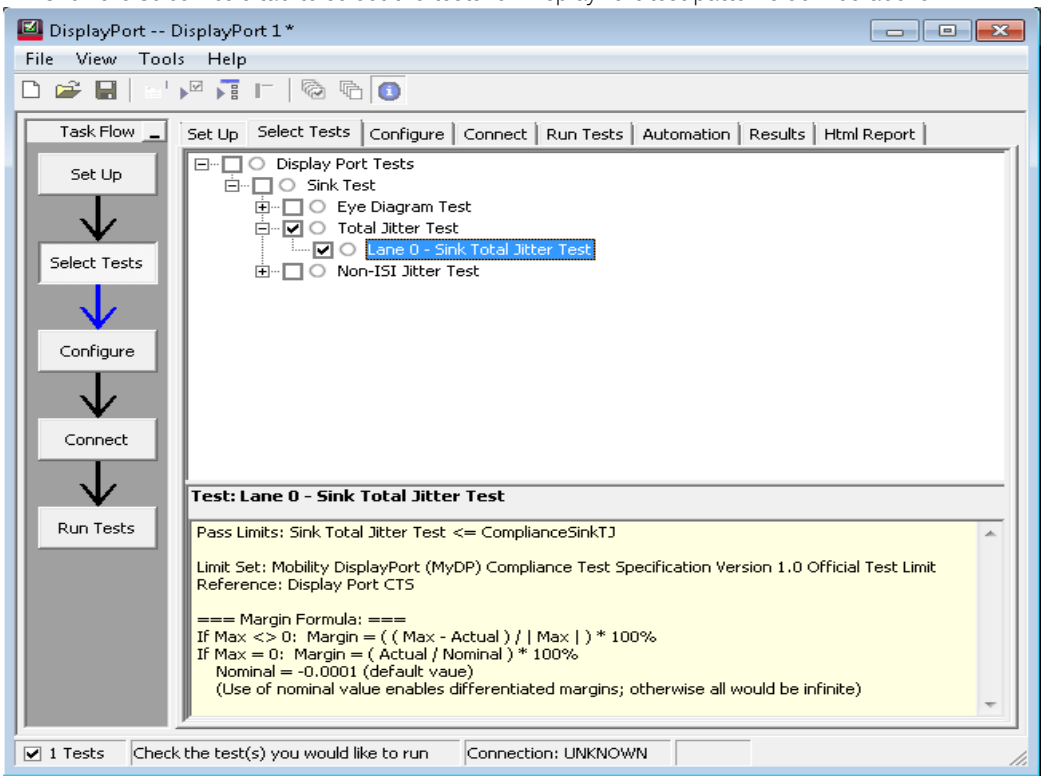


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Sink Tests" on page 632 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 116 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 117 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Tests

Test ID

12220001 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Calculate Non-ISI Jitter using the following equation:

$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

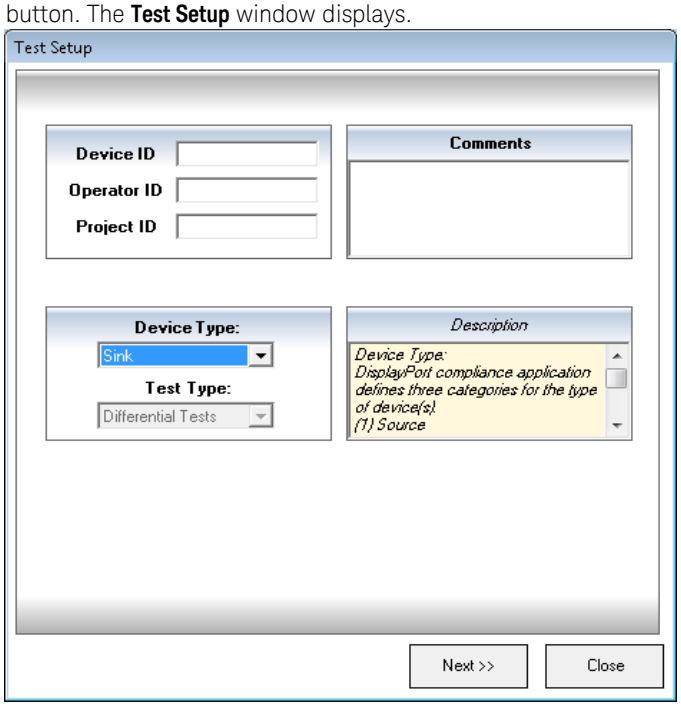
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR and HBR2)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



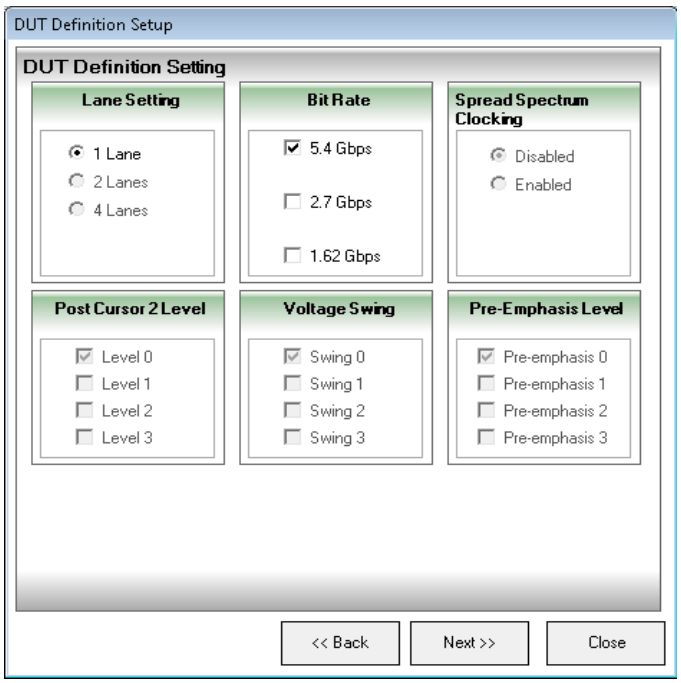
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

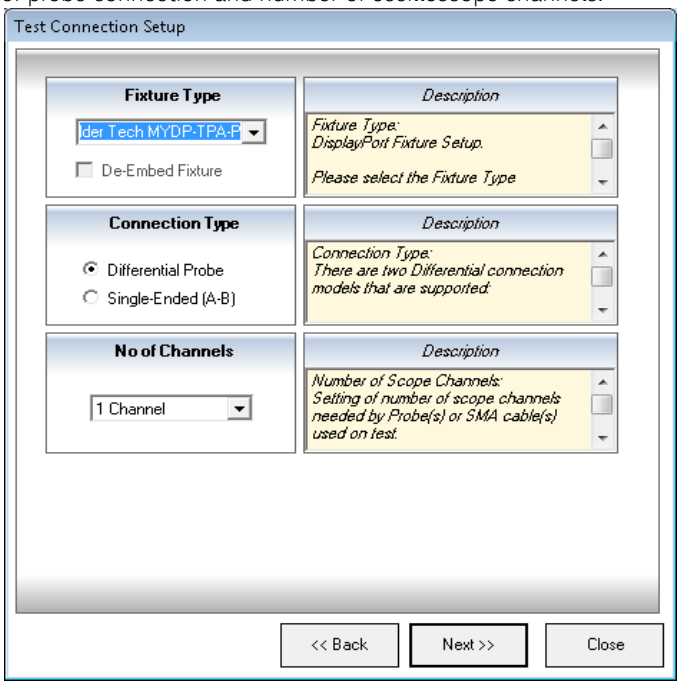
b Select **Device Type:** as **Sink**, **Test Type:** automatically grays out.

c Click **Next**.

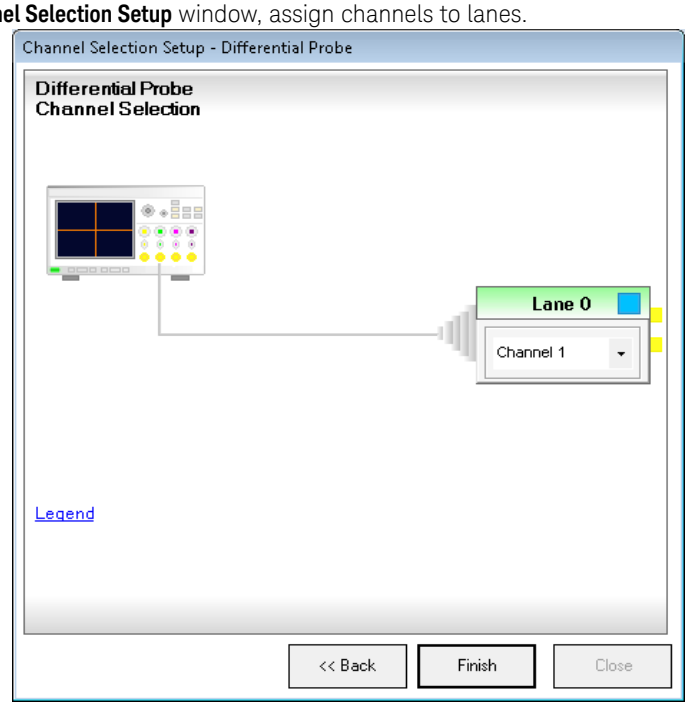
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

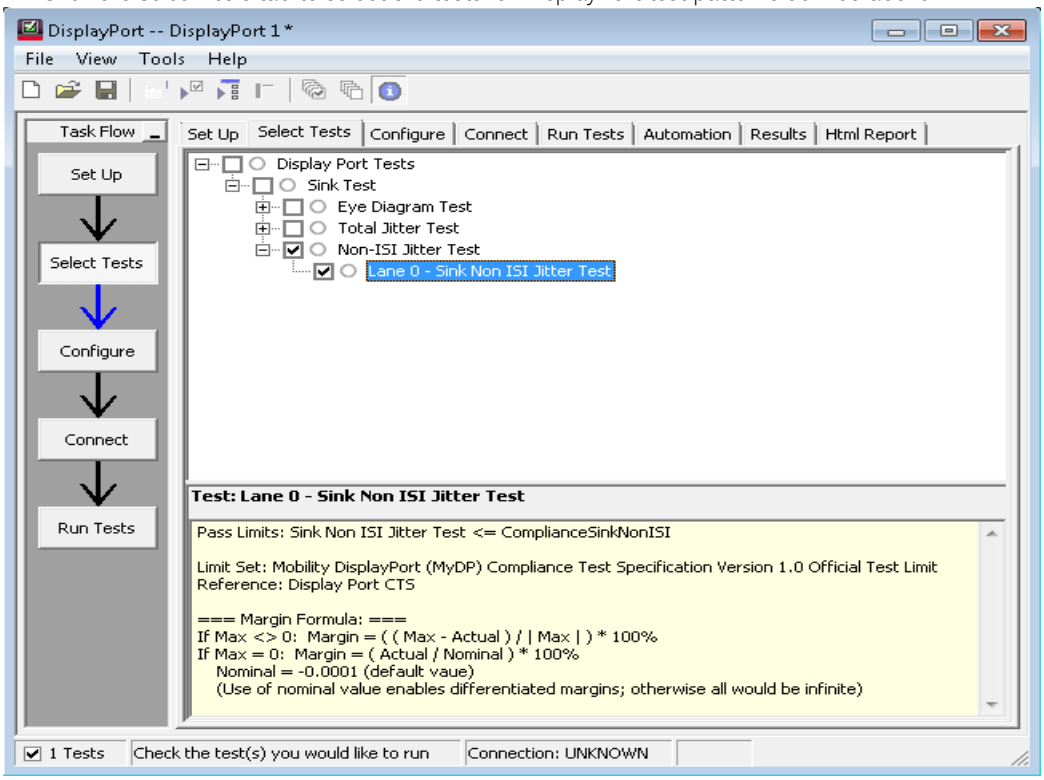


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Sink Tests" on page 632 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 118 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 119 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

17 MyDP 1.0 Cable Tests

Overview

Test Point Definition for MyDP 1.0 Cable Tests

NOTE Cable Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Cable DUT at Test Point 3 (TP3) as shown in Figure 122. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

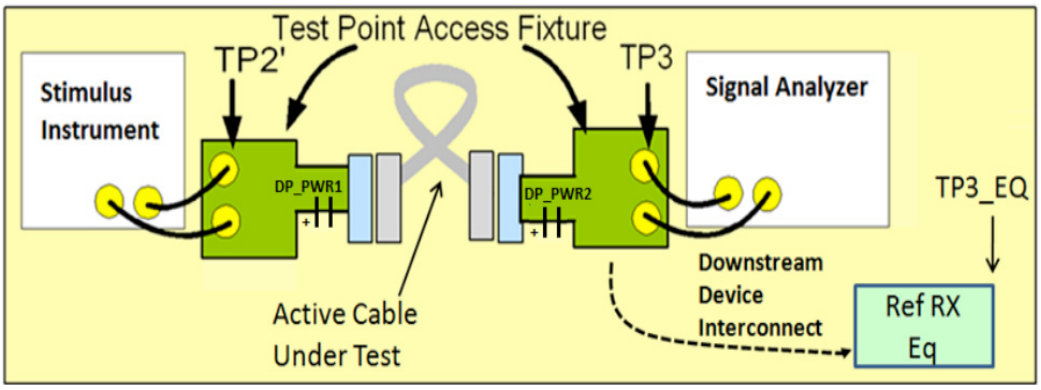


Figure 122 Test Point 3 Connection for MyDP 1.0 Cable Tests

Table 120 defines the test point fixtures and instruments used for MyDP 1.0 Cable Tests:

Table 120 Test Point Fixtures and Instruments for MyDP 1.0 Cable Tests

Test Requirement	Device Used
Stimulus Instrument	Pulse Pattern Generator ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Table 121 defines the input signal parameters applied by the stimulus instrument at TP2:

Table 121 Input Signal Parameters by Stimulus Instrument

RBR	▪ Reference Table 3-22 and Table 3-24, DP 1.2a ▪ Edge Rate (20-80): 155-165ps (260mUI) ▪ Eye Height: 400mV ▪ Total Jitter: 270mUI ▪ ISI: 100mUI ▪ Random Jitter (rms): 7.9mUI ▪ Sinusoidal Jitter: ~75mUI at 20MHz (Adjust to achieve Total Jitter)
HBR	▪ Reference Table 3-22 and Table 3-23, DP 1.2a ▪ Edge Rate (20-80): 90-100ps (260mUI) ▪ Eye Height: 350mV ▪ Total Jitter: 420mUI ▪ ISI: 144mUI ▪ Random Jitter (rms): 13.2mUI ▪ Sinusoidal Jitter: ~117mUI at 20MHz (Adjust to achieve Total Jitter)

Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Cable Tests

Perform the following steps before you run the compliance tests on the cable device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Table 123).

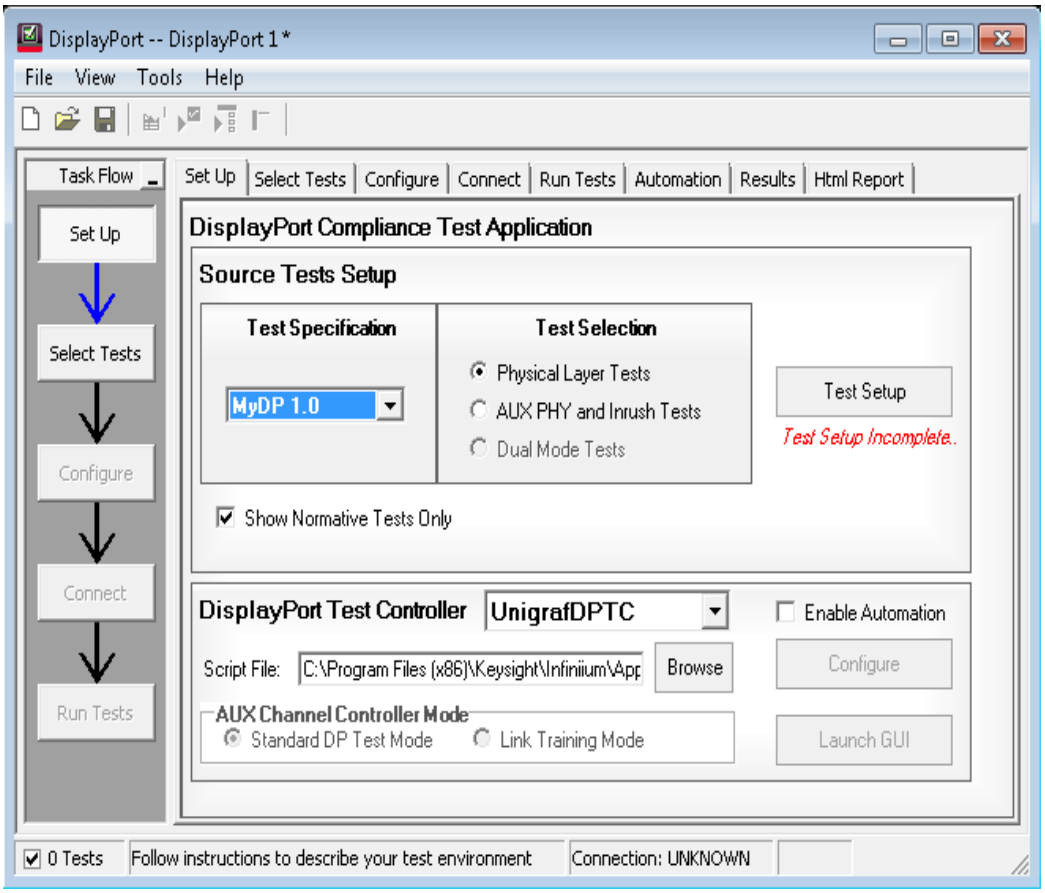


Figure 123 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with Mobility DisplayPort 1.0 Standards, select **MyDP 1.0** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for MyDP 1.0 Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

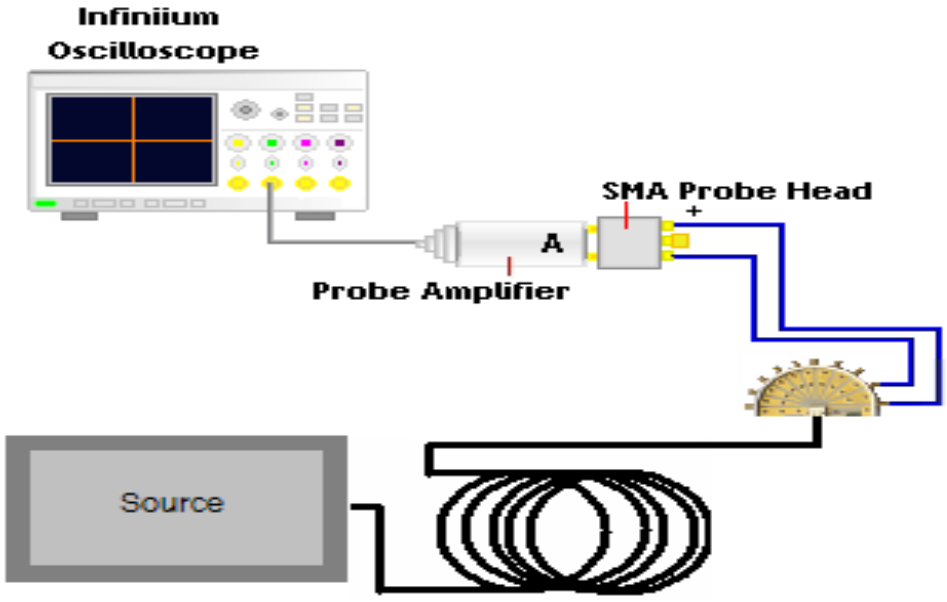


Figure 124 Sample connection diagram for MyDP 1.0 Cable Tests

Cable Eye Diagram Test

Test ID

12150001 – Eye Diagram Test

Test Overview

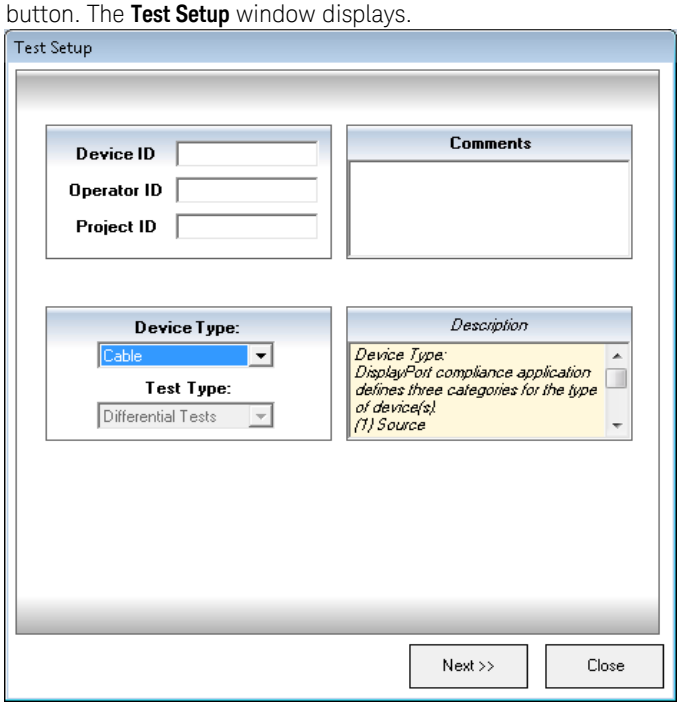
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 121
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



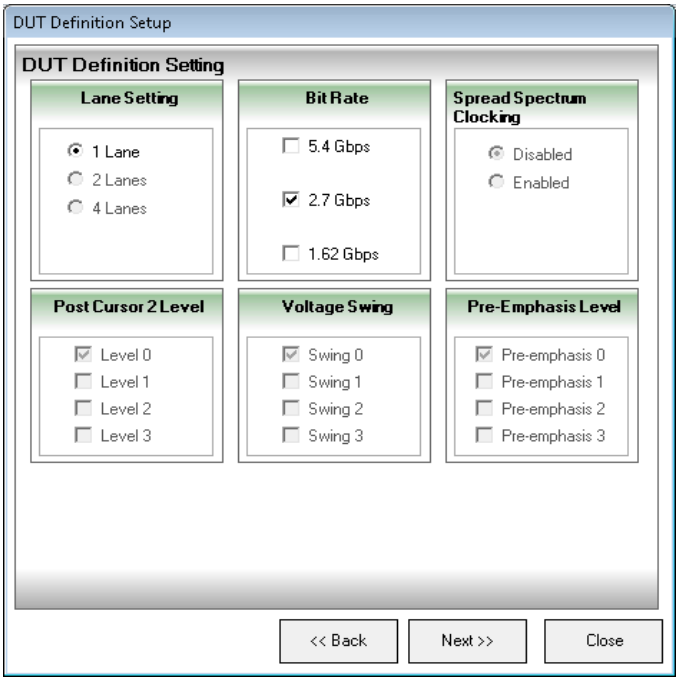
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

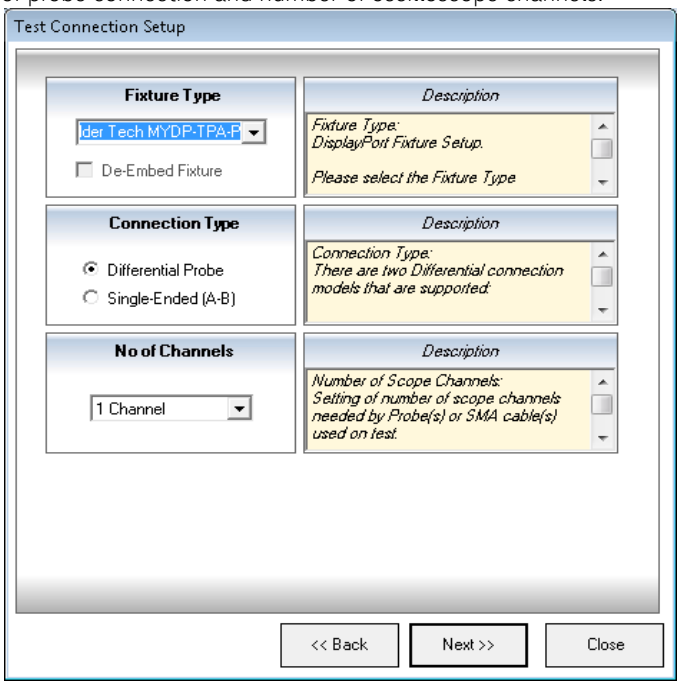
b Select **Device Type:** as **Cable**, **Test Type:** automatically grays out.

c Click **Next**.

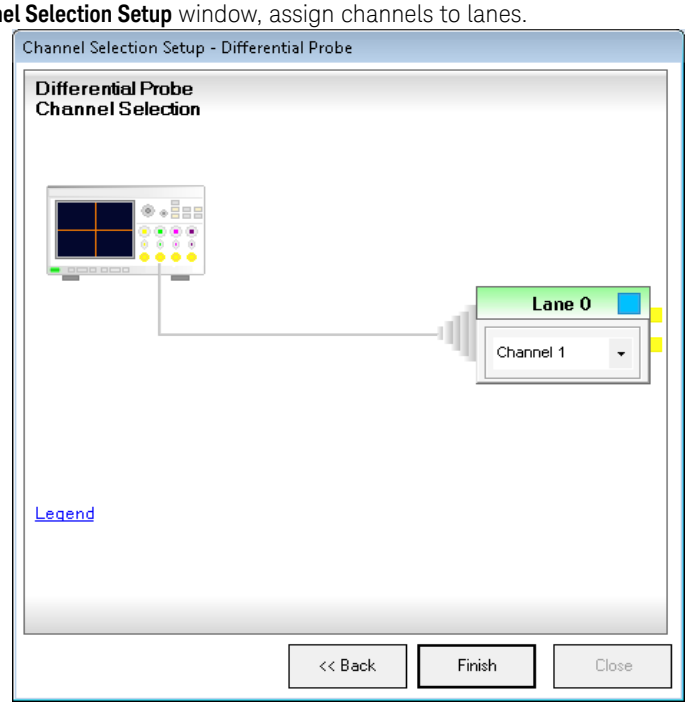
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

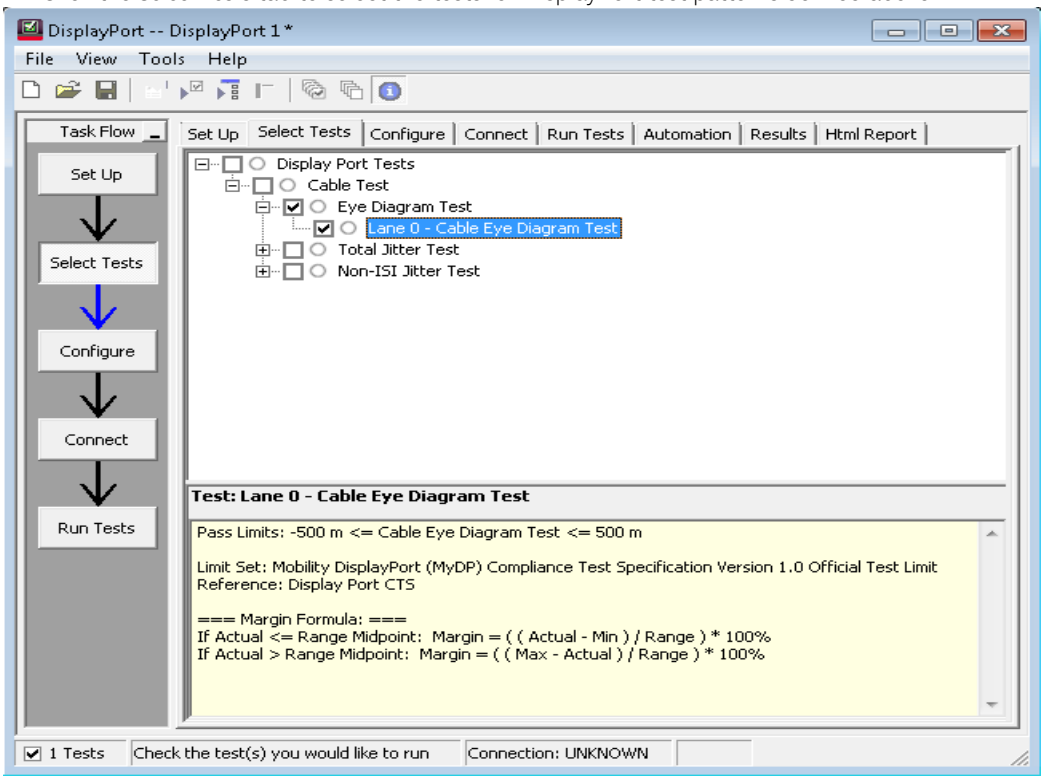


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Cable Tests" on page 656 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1. Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2. Acquire and verify the input signal.
   a. Verify the trigger and the amplitude of the input signal.
   b. Scale the vertical display of the input signal to the optimum value.
   c. Measure V_{TOP} and V_{BASE} of the input signal.
3. Create FUNC3 signal, which is the magnify signal of the input signal.
4. Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a. Scale the vertical display of the equalized signal to the optimum value.
   b. Measure V_{TOP} and V_{BASE} of the equalized signal.
   c. Measure the data rate of the equalized signal.
5. Set up the parameter of the measurement:
   a. Enable measurement of all edges to obtain a statistical value of the measurement.
   b. Set up the measurement threshold.
   c. Set up the Clock Recovery as described in the section “Clock Recovery”.
6. Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7. Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8. Set up the parameter for the Mask Test.
   a. Load the eye mask based on the settings in the Configuration Variable.
   b. Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c. Run the eye mask until 1,000,000 UI are folded.
9. Measure the jitter of the eye diagram using the Histogram.
10. Check for any signal trajectories that may have entered into the mask.
11. Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 122 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 122 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

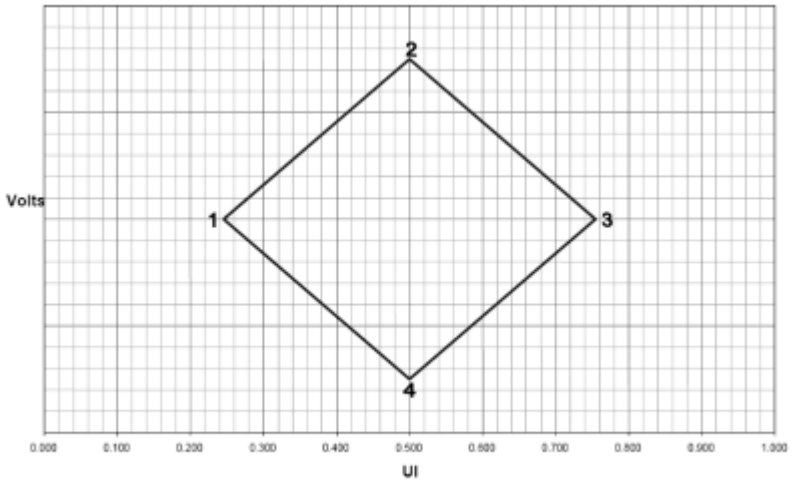


Figure 125 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

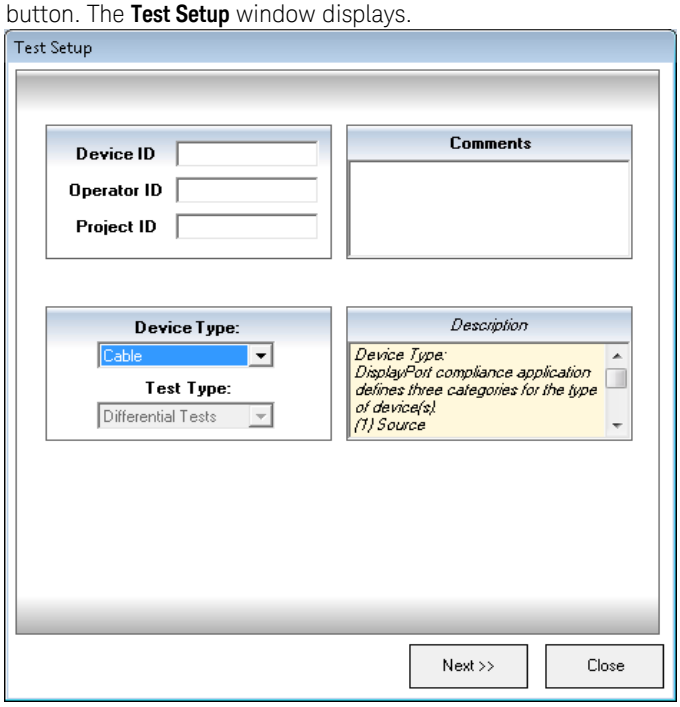
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 121

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



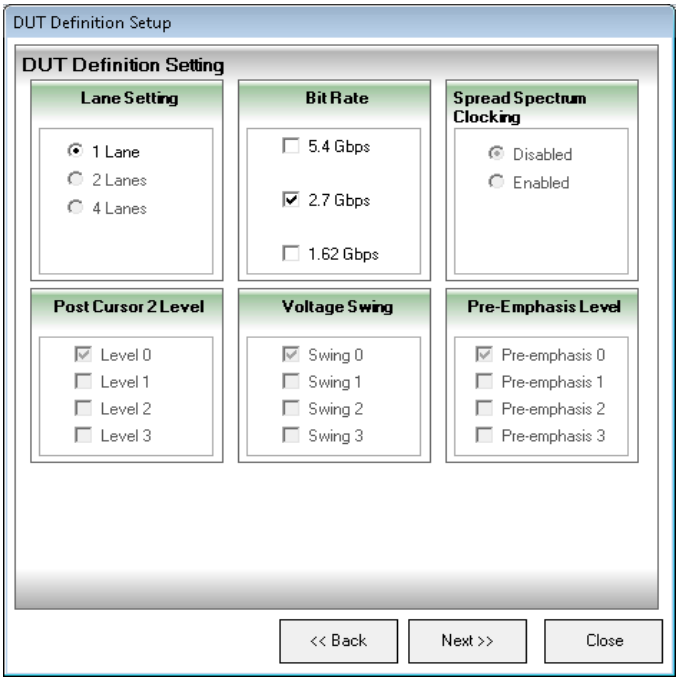
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

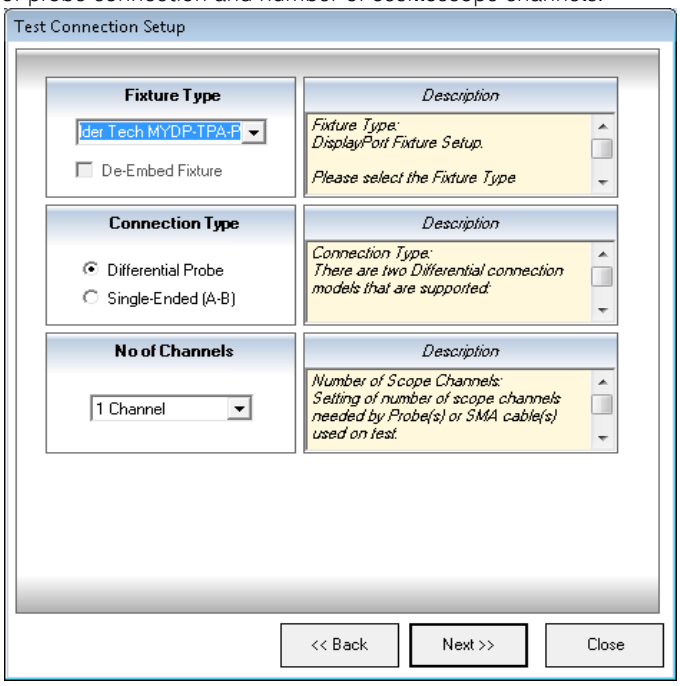
b Select **Device Type:** as **Cable**, **Test Type:** automatically grays out.

c Click **Next**.

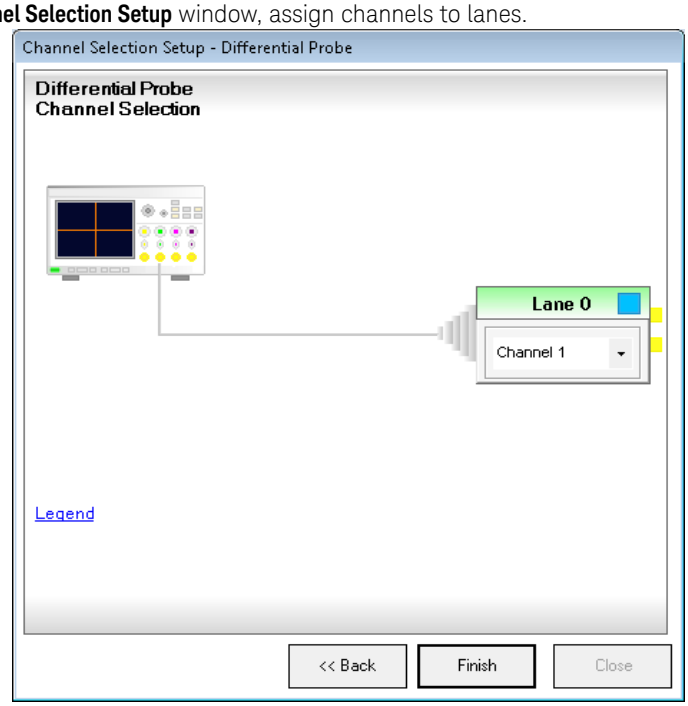
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

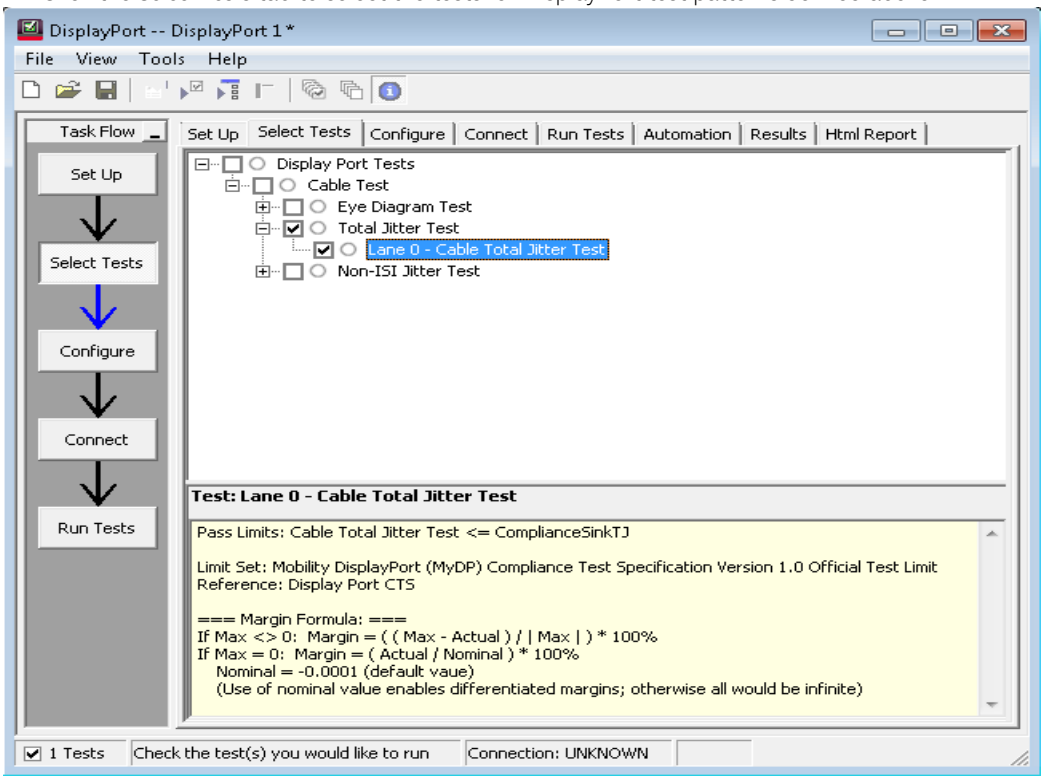


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Cable Tests" on page 656 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 123 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Calculate Non-ISI Jitter using the following equation:

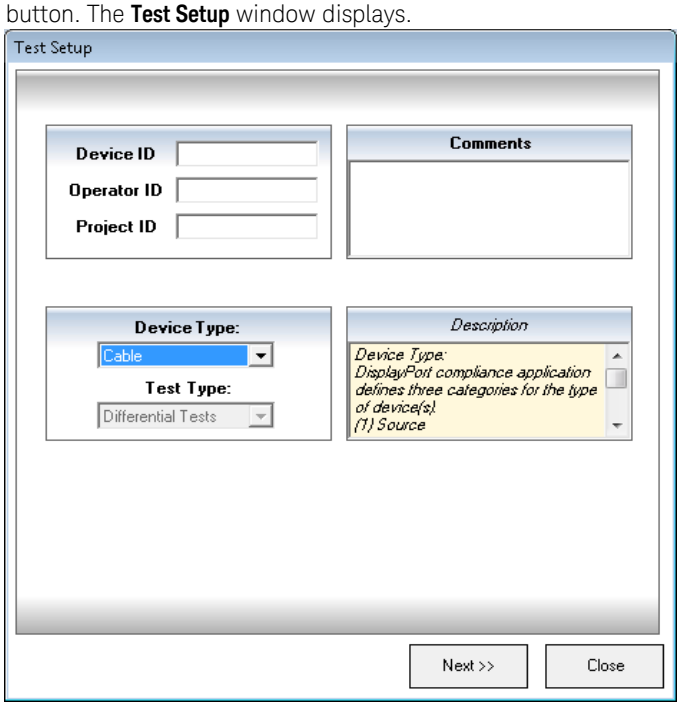
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 121

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



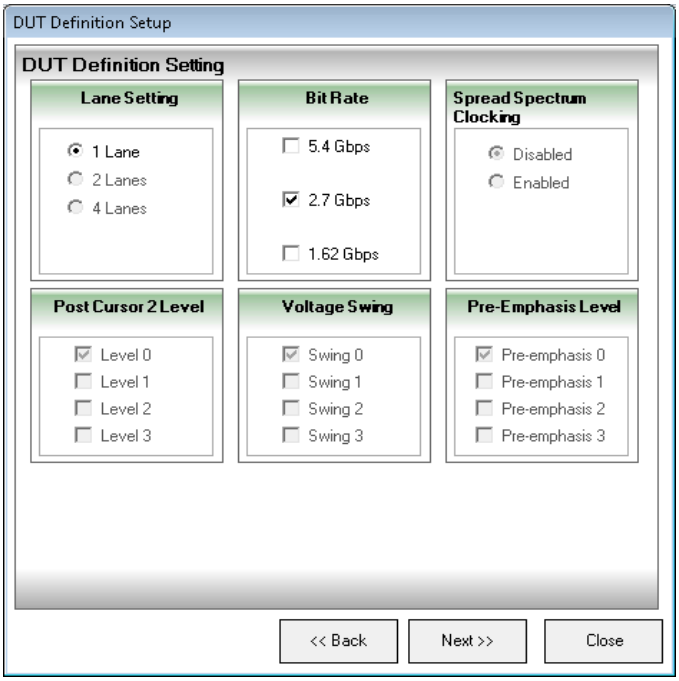
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

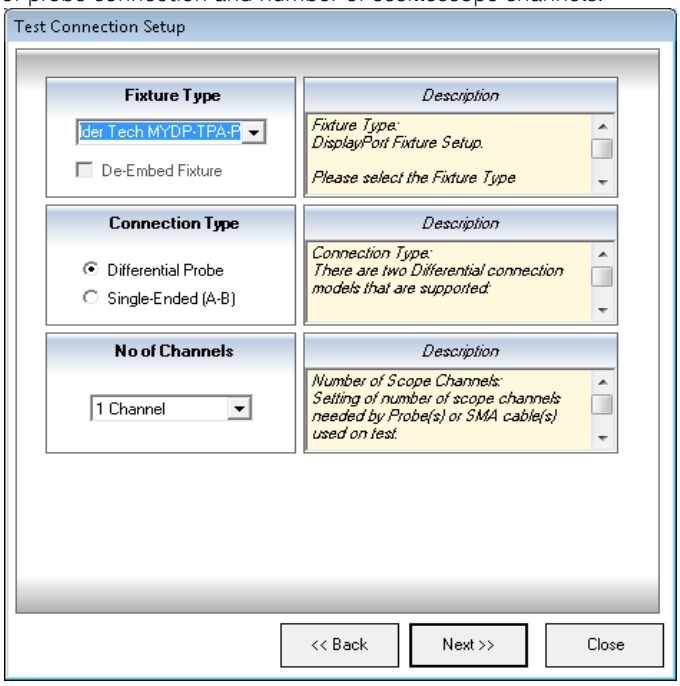
b Select **Device Type:** as **Cable**, **Test Type:** automatically grays out.

c Click **Next**.

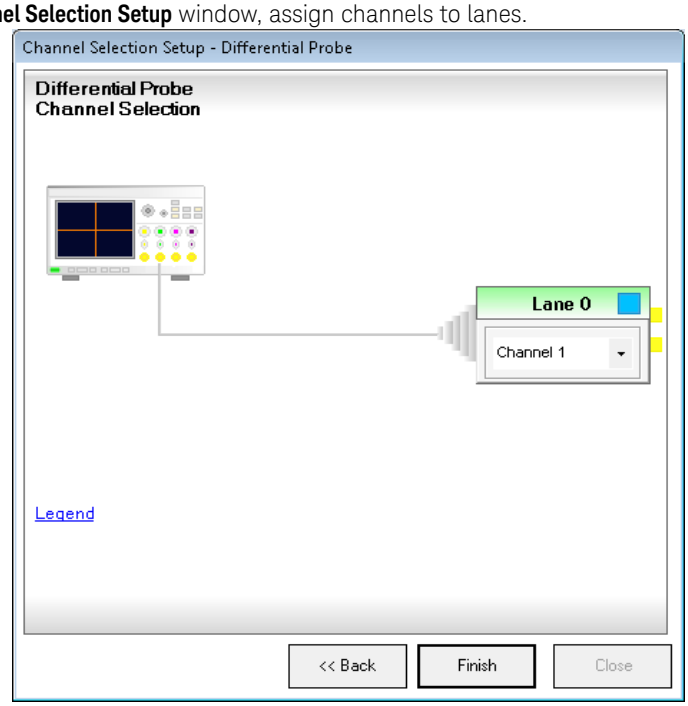
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

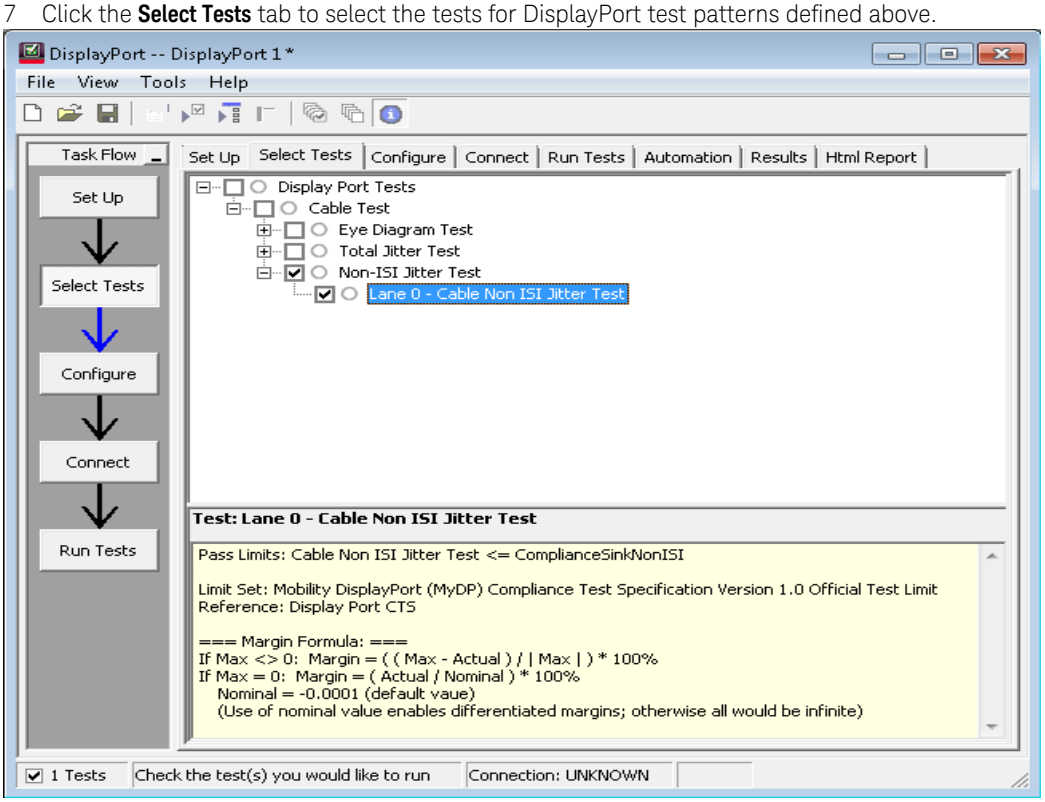


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Cable Tests" on page 656 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PPASS Condition

Table 124 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

18 MyDP 1.0 AUX Channel Tests

Overview

Test Point for MyDP 1.0 AUX Channel Tests

You must test the Source devices at Test Point 2 (TP2) while the Sink devices must be tested at Test Point 3 (TP3). See Figure 126.

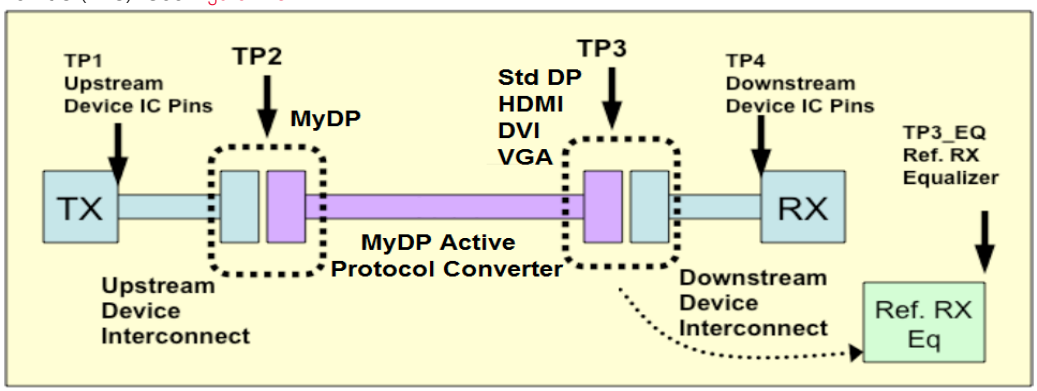


Figure 126 Test Points for MyDP 1.0 AUX Channel Tests

Table 125 defines the test point fixtures and instruments used for MyDP 1.0 AUX Channel Tests:

Table 125 Test Point Fixtures and Instruments for MyDP 1.0 AUX Channel Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope
Stimulus	Stimulus must be applied to the DUT to cause AUX Channel transactions to occur. This stimulus shall not be included in or affect the measurements. Reference Sink needed as stimulus for the Source DUT: ▪ Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Reference Source needed as stimulus for the Sink DUT: ▪ Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 AUX Channel Tests

Perform the following steps before you run the compliance tests on the AUX channel device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 126).

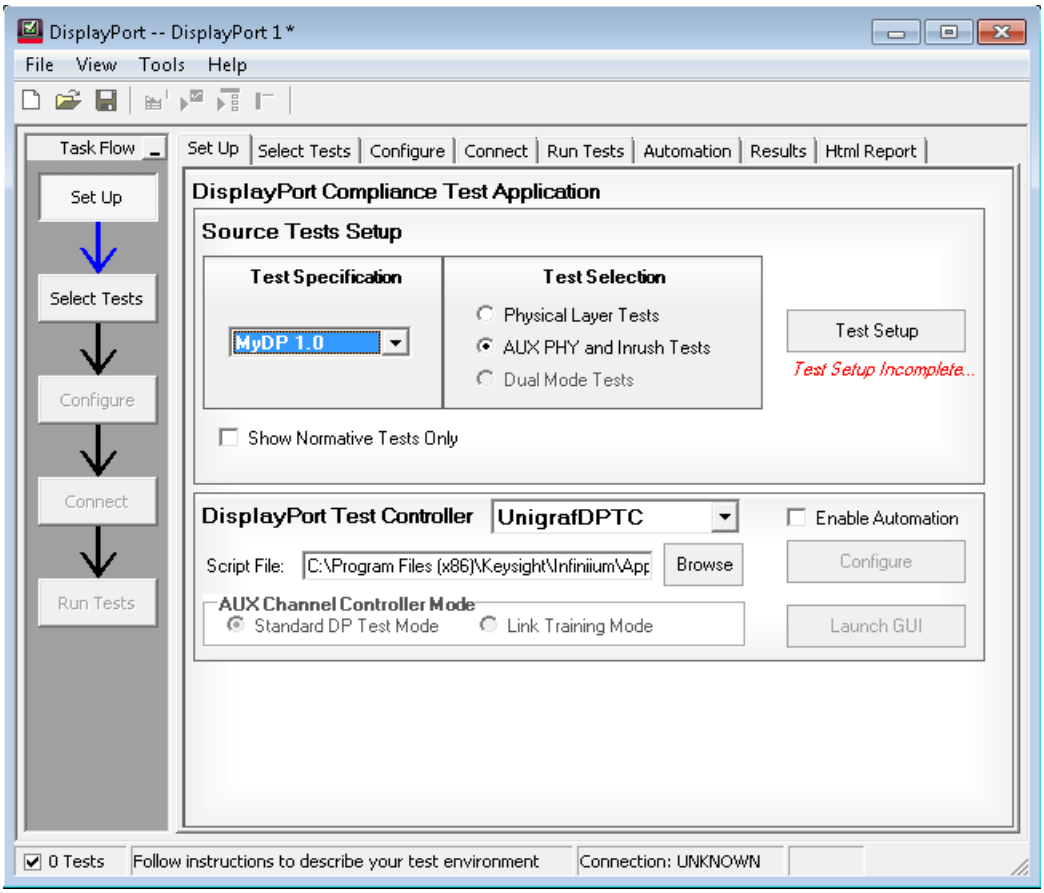


Figure 127 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with Mobility DisplayPort 1.0 Standards, select **MyDP 1.0** from the drop-down options in the **Test Specification** area and select **AUX PHY and Inrush Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

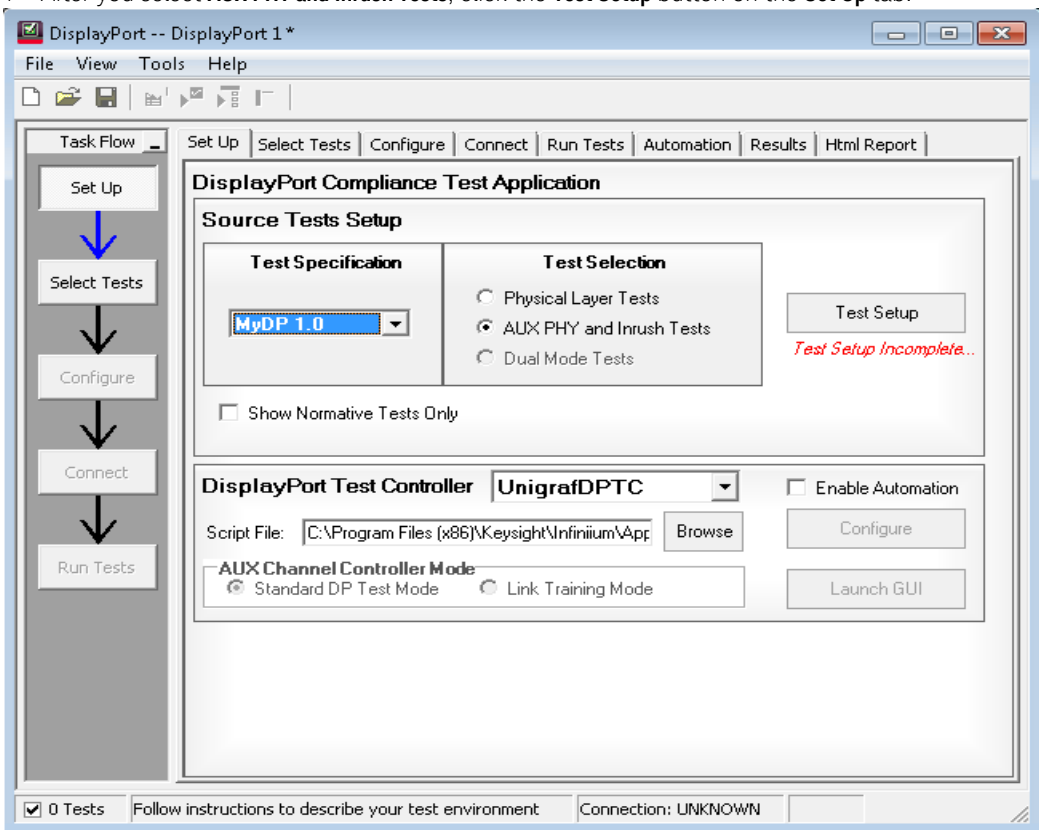
10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

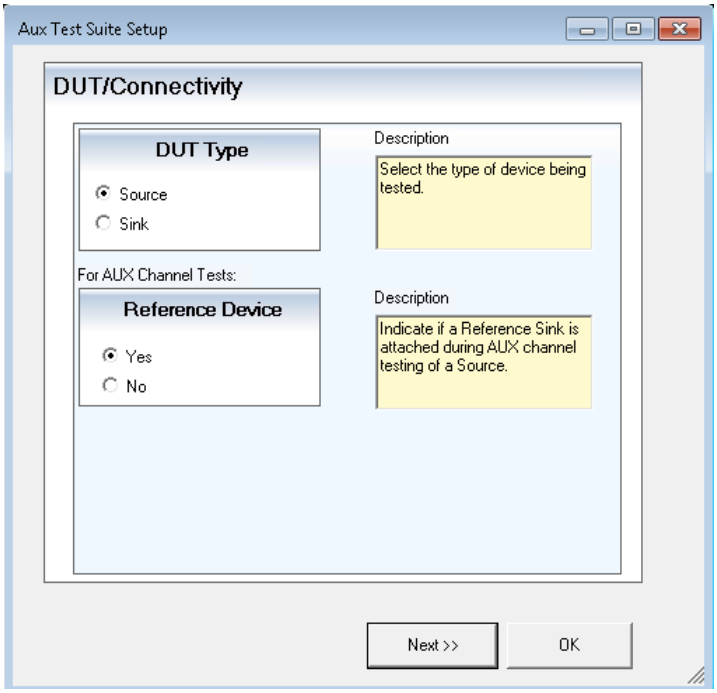
Setting Up for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

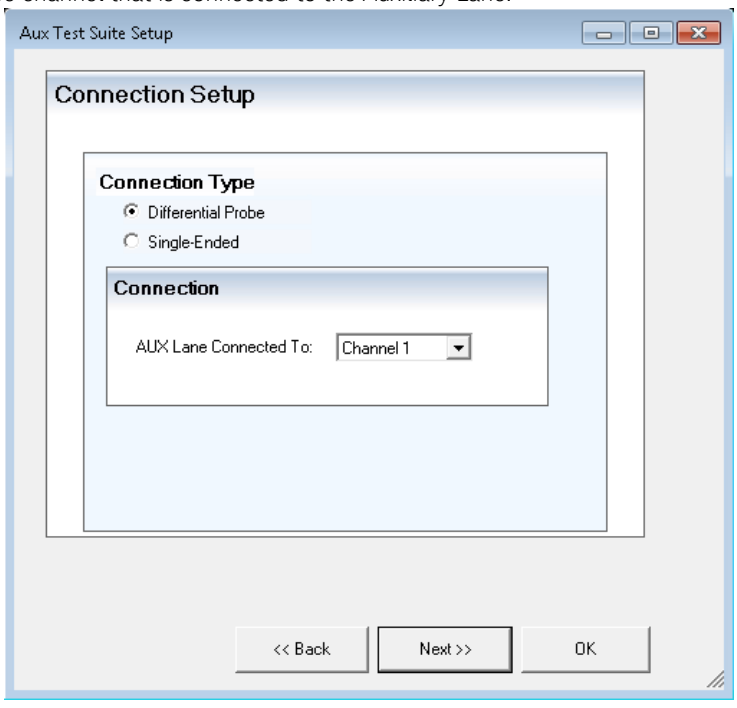
1 After you select **AUX PHY and Inrush Tests**, click the **Test Setup** button on the **Set Up** tab.



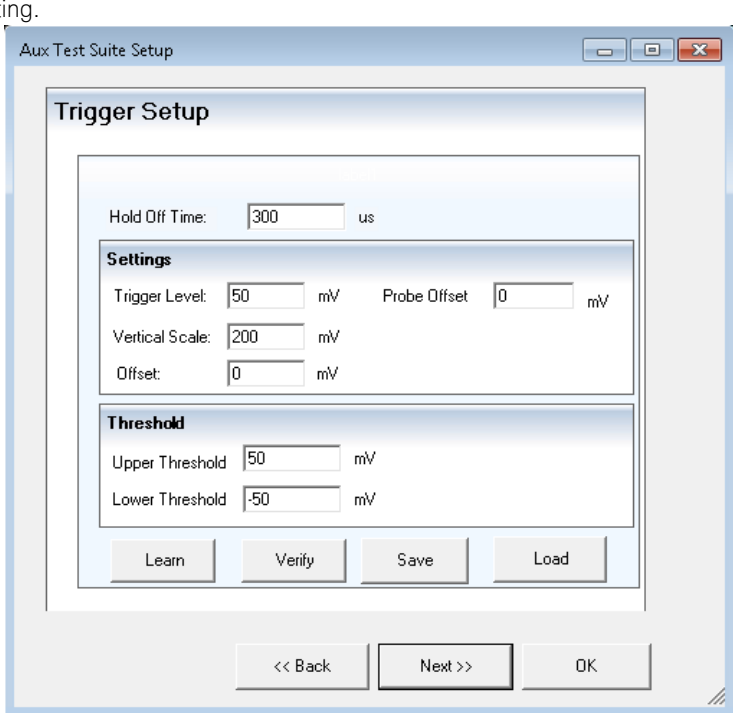
2 On the **DUT/Connectivity** page, select **Source** or **Sink** in the **DUT Type** area. In the **Reference Device** area, select **Yes** if a reference sink/source is attached to device under test during testing. Click **Next**.



3 On the **Connection Setup** page, depending on the probe connection you are using, select either **Differential Probe** or **Single-Ended** in the **Connection Type** area and in the **Connection** area, select the oscilloscope channel that is connected to the Auxiliary Lane.



4 On the **Trigger Setup** page, define the oscilloscope parameters to trigger on an Auxiliary signal during testing.



Hold Off Time – The oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each AUX transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.

Trigger Level – The AUX channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure shows correct and incorrect trigger levels.

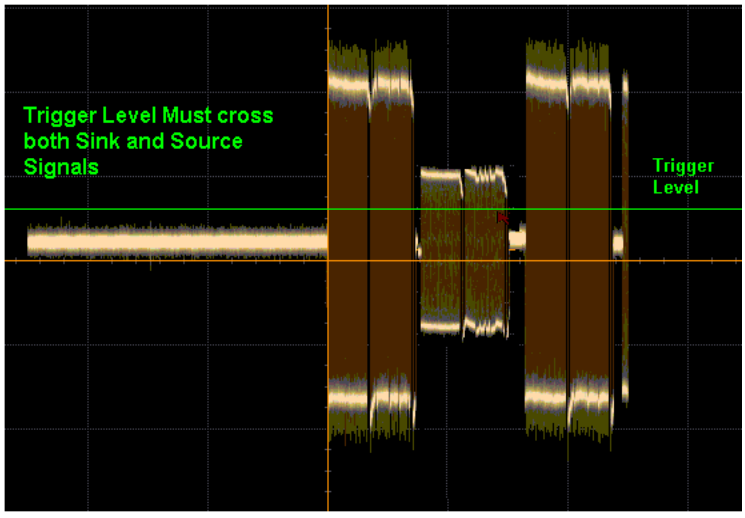


Figure 128 Correct Trigger Level

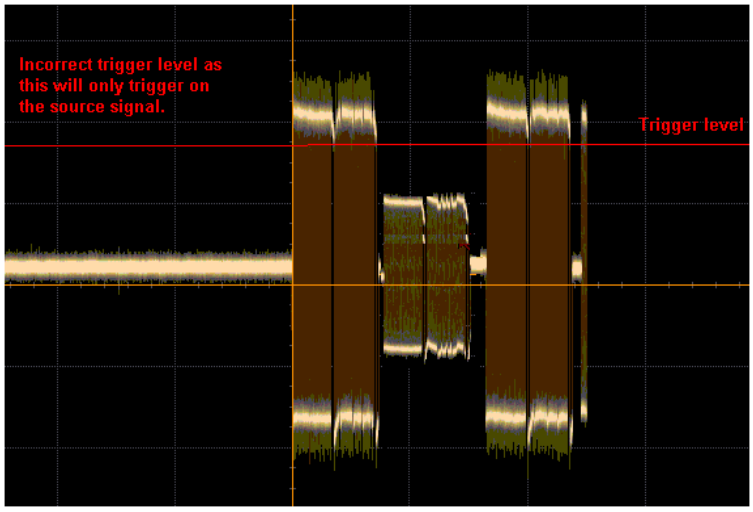


Figure 129 Incorrect Trigger Level

Vertical Scale – The oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.

Offset – Set the offset so that the center point is aligned with the center of the oscilloscope display.

Upper Threshold/Lower Threshold – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply.

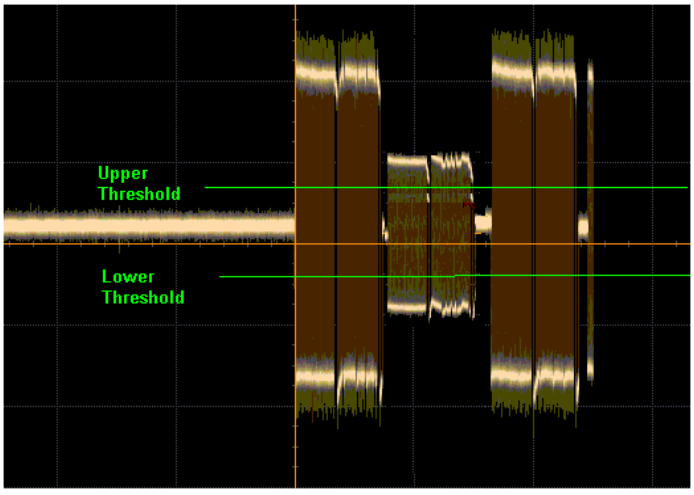


Figure 130 Correct Threshold set

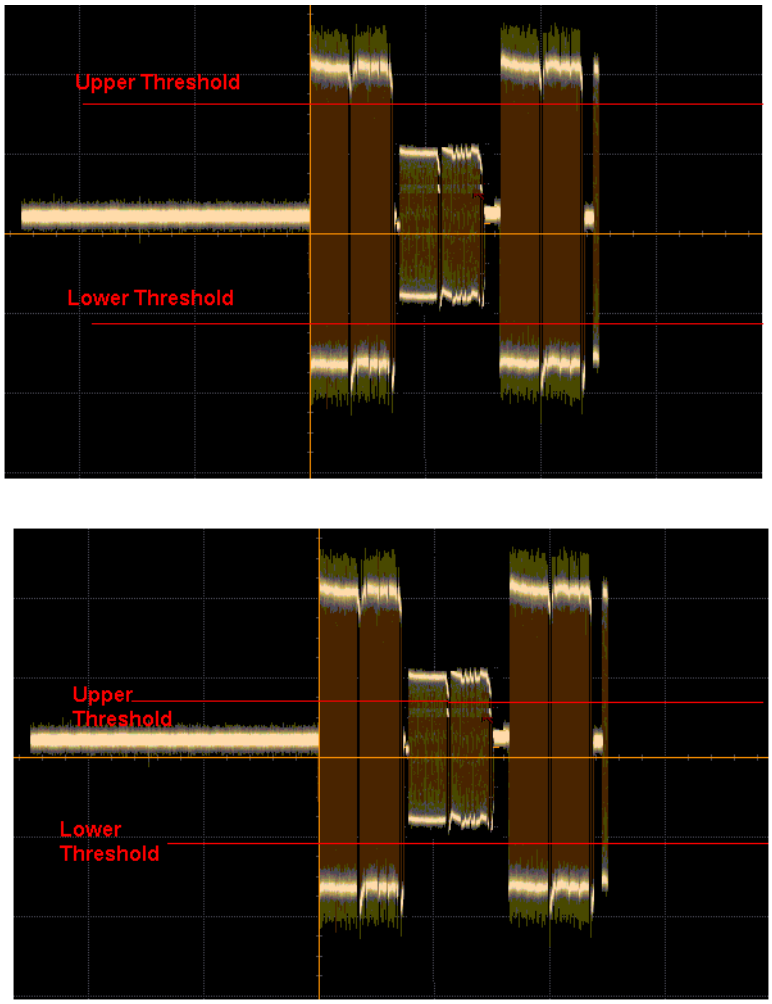


Figure 131 Wrong Thresholds set

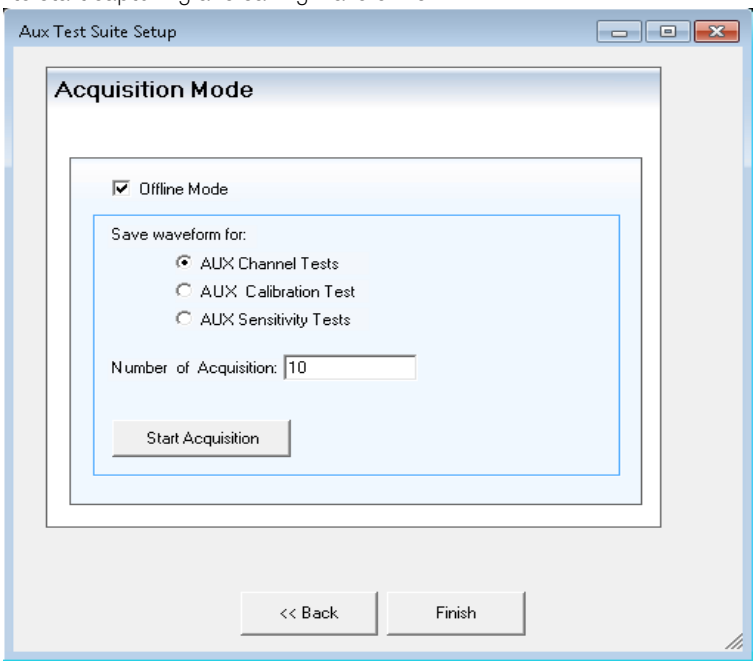
c On the **Trigger Setup** page, you may click the **Learn** button, which guides you through getting the trigger setup parameters. However, please note that the learning guide may not necessarily work many a times because the actual Auxiliary signals may vary for different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.

d Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.

e You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

5 On the **Acquisition Mode** page, either **Finish** the setup wizard or enable **Offline Mode**, which is de-selected, by default. Offline Mode lets you save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.

6 If you enable **Offline Mode**, define the number of waveforms to be saved. If required, click **Start Acquisition** to start capturing and saving waveforms.



7 Click **Finish** to close the setup wizard. The **Set Up** tab displays.

8 Click the **Select Tests** tab and select the AUX Channel tests you want to run.

Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

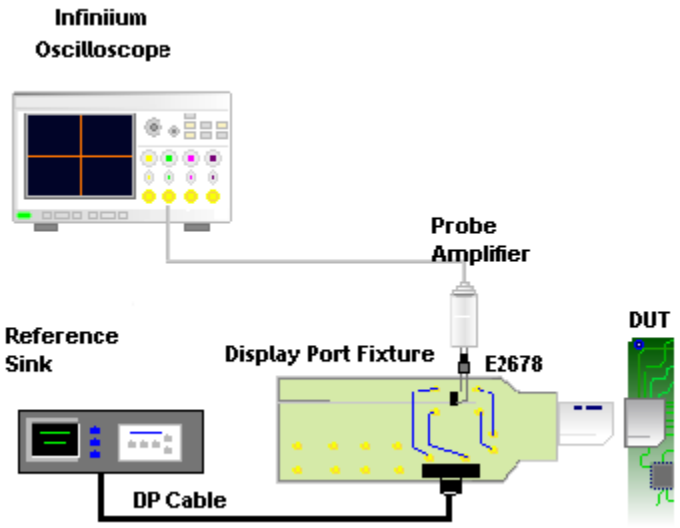


Figure 132 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

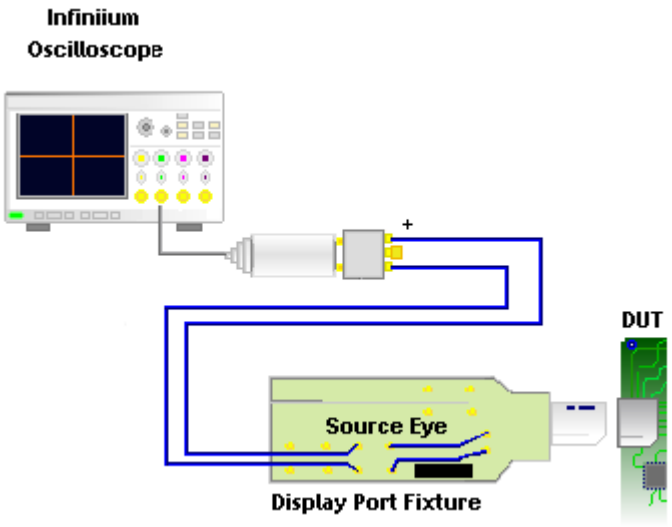


Figure 133 Sample connection diagram for source AUX channel tests without connecting to a reference sink

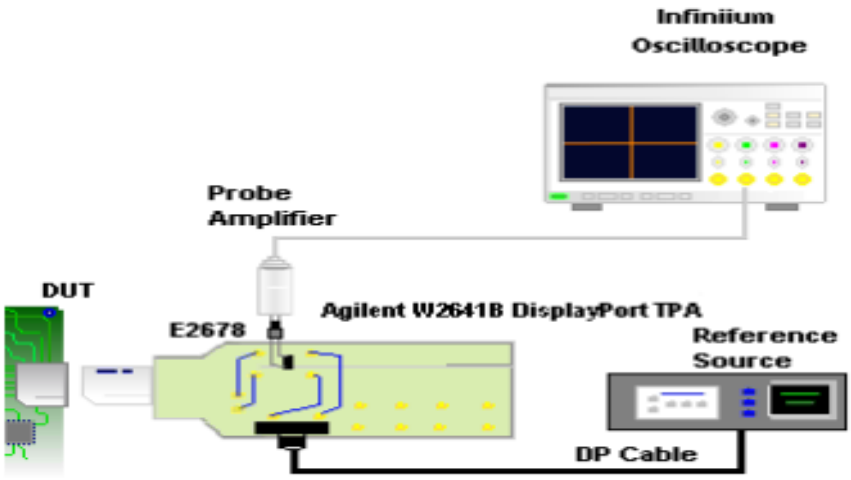


Figure 134 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-2*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

9 Check for any signal trajectories entering into the mask.

10 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 126 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

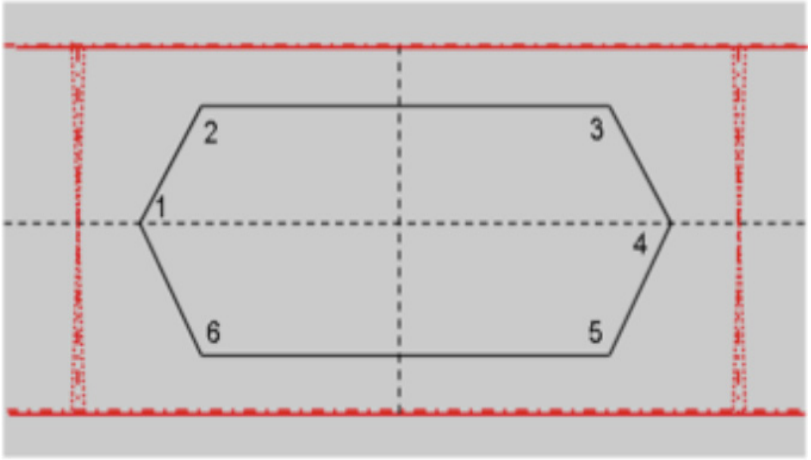


Figure 135 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-1 and Table 2-2*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2.6, Figure 3-29 and Table 3-8*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:

   a Set up the parameter of the Mask Test:

      i Load the eye mask based on the settings in the Configuration Variable.

      ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

      iii Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

   b Check for any signal trajectories entering into the mask.

9 Report the measurement results.

PASS Condition

Table 127 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 128 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.1 and Section 7.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

19 MyDP 1.0 Inrush Tests

Overview

This section describes the normative and informative inrush tests for compliance verification of Mobility DisplayPort source and sink, which is a power consumer.

Test Point for MyDP 1.0 Inrush Tests

The test fixture for inrush tests implements the schematic shown in Figure 136.

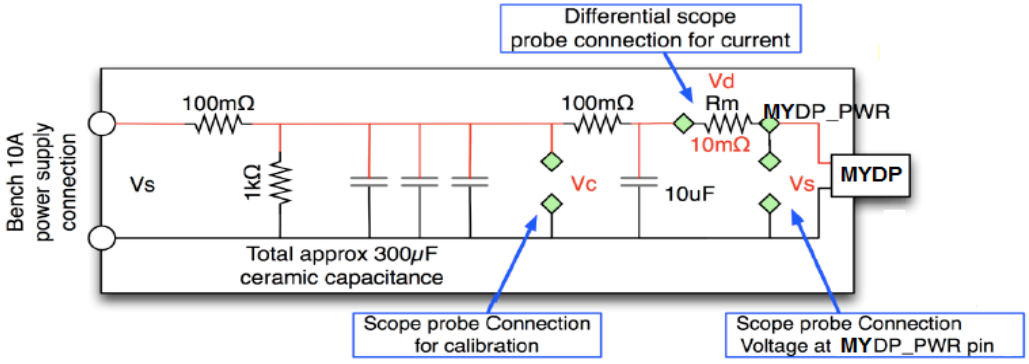


Figure 136 Schematics for testing a Power Consumer Device

The test fixture must be designed and used according to the following guidelines:

- A high gate voltage FET on the MyDP_PWR line is recommended to allow a fast connect capability, which allows a single connection event for testing. Without such an arrangement, multiple connections will be required to obtain a reasonable “worst-case” attachment event.
- Connection length between the power supply and the test fixture must be minimized. A maximum of four inches is recommended.
- The power supply must have enough outrush capability as to not negatively affect the test fixture’s outrush capability.
- The power supply must be run at 5.5V (5.0V + 10%) read across V_C.

Any Power Consumer test fixture must be calibrated using the Power User test fixture, as shown in Figure. Testing with the two fixtures combined should result in the approximate values given below. If required, the component values on the Power Consumer test fixture should be adjusted to match the expected results.

For Source:

- V_C steady before connection = 5.5V
- Inrush Current = ~9.0A

For Sink:

- V_C steady before connection = 3.6V
- Inrush Current = ~13.0A

Setting Up the DisplayPort Compliance Test Application for MyDP 1.0 Inrush Tests

Perform the following steps before you run the compliance tests on the DUT:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 137).

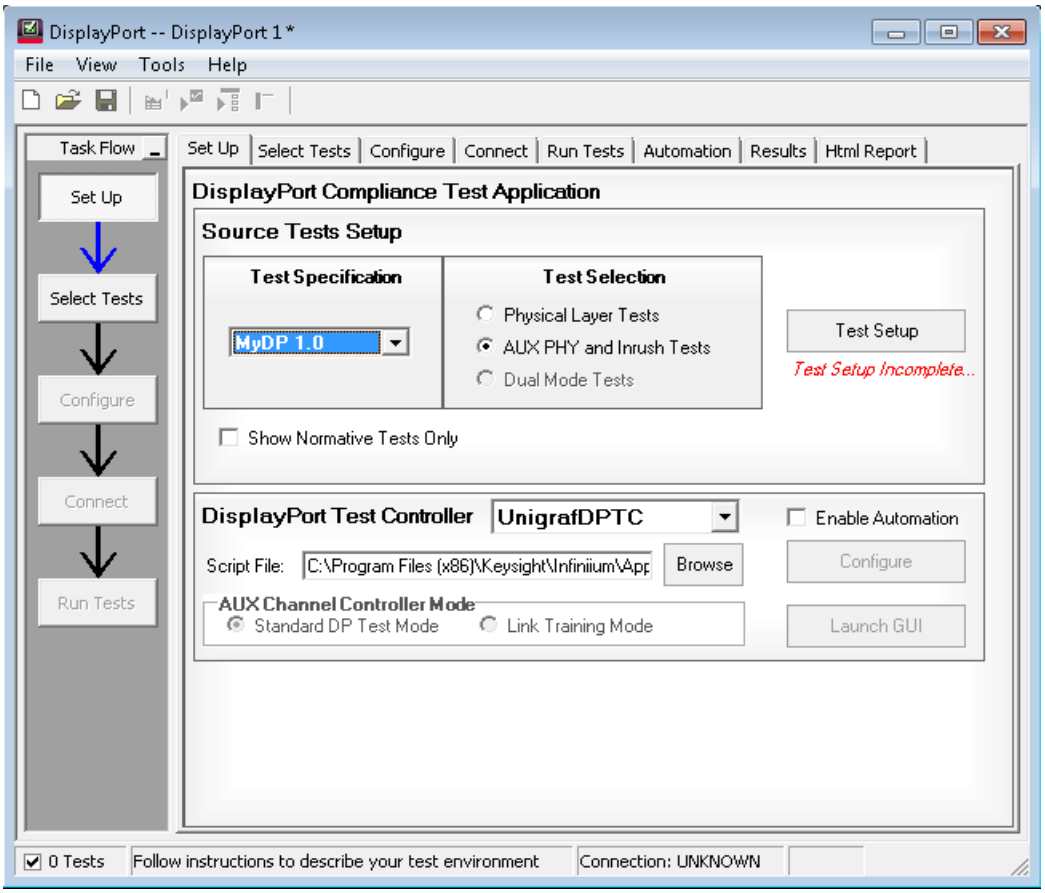


Figure 137 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with Mobility DisplayPort 1.0 Standards, select **MyDP 1.0** from the drop-down options in the **Test Specification** area and select **AUX PHY and Inrush Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests. Refer to "Setting Up for AUX PHY and Inrush Tests" on page 679 to know in detail how to set up the DUT for Inrush Tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make

changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Current $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 9$ Amps

Test References

See:

For Source:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.5*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

For Sink:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 3.4*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 – Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Current $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 9$ Amps

Test References

See:

For Source:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.5*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

For Sink:

- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 3.4*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

20 SlimPort Source Tests

Overview

This section describes the normative and informative tests for compliance verification of SlimPort source, sink and cable DUTs.

Test Point Definition for SlimPort

Five different test points are identified for the physical layer measurement. See Figure 138.

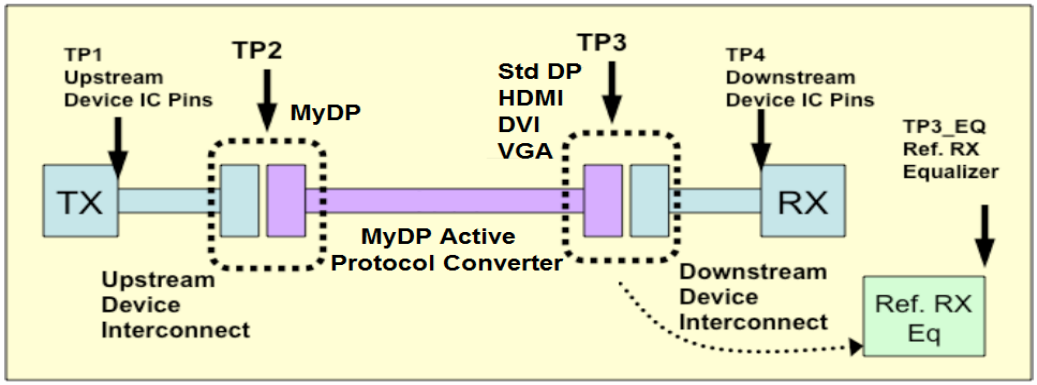


Figure 138 Test Points in a DisplayPort InterConnect System

Table 129 defines the Test Points used for SlimPort Tests:

Table 129 Test Points for DisplayPort Tests

Test Point	Description
TP1	At the pins of the Transmitter Device
TP2	At the test interface on a test access fixture as close as possible to the DP mated connection to a Source device
TP3	At the test interface on a test access fixture as close as possible to the DP mated connection to a Sink device
TP3_EQ	At TP3, when a defined cable model with equalizer is applied. There are two defined cable models: ▪ Worst Cable Model as defined in VESA DisplayPort 1.2a Standard, ▪ Zero length, zero loss cable. The equalizer is also defined in VESA DisplayPort 1.2a Standard
TP4	At the pins of a receiving device

Cable Models

The two cable models defined in VESA DisplayPort 1.2a Standard are:

1 Worst Case Cable Model—To achieve the TP3_EQ signal with the worst case cable model:

- Acquire the signal at TP2.
- Embed the TP2 signal with a “worst case” HBR cable model using an InfiniiSim Waveform Transformation Toolset software to emulate the insertion loss as defined in Figure 4-10 of the VESA DisplayPort 1.2a Standard.
  - For the DisplayPort Compliance Test Application, the “*CIC_rev0p6.s4p*” cable model transfer function is used.

- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

2 Zero Length Cable Model—To achieve the TP3_EQ signal with the zero length cable model:

- Acquire the signal at TP2.
- No cable model is embedded for the Zero Length cable model.
- Finally, apply the HBR or HBR2 equalization using the Serial Data Equalization software as defined in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

Equalization

When equalization is required, use the CTLE (Continuous Time Linear Equalization) transfer function, as given in Figure 3-40 (for HBR) and Figure 3-41 (for HBR2) of the VESA DisplayPort 1.2a Standard.

For main link, use the CTLE model with the following transfer function for HBR (2.7 Gbps):

The HBR Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{s + \omega_z}{(s + \omega_{p1})(s + \omega_{p2})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}}{\omega_z} \cdot \frac{\sqrt{\omega^2 + \omega_z^2}}{\sqrt{\omega^2 + \omega_{p1}^2} \cdot \sqrt{\omega^2 + \omega_{p2}^2}}$$

where

$$\omega_z = 2\pi(0.725 \times 10^9)$$
$$\omega_{p1} = 2\pi(1.35 \times 10^9)$$
$$\omega_{p2} = 2\pi(2.5 \times 10^9)$$

Figure 139 Transfer Function of the CTLE model for HBR

Table 130 CTLE Model for HBR

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.725 GHz	0.725 GHz
Pole 1 Frequency	1.35 GHz	1.35 GHz
Pole 2 Frequency	2.5 GHz	2.5 GHz

For main link, use the CTLE model with the following transfer function for HBR2 (5.4 Gbps):

The HBR2 Reference Equalizer transfer function is given by

$$H(s) = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{s+\omega_z}{(s+\omega_{p1})(s+\omega_{p2})(s+\omega_{p3})}$$

which has magnitude given by

$$|H(j\omega)| = \frac{\omega_{p1}\omega_{p2}\omega_{p3}}{\omega_z} \cdot \frac{\sqrt{\omega^2+\omega_z^2}}{\sqrt{\omega^2+\omega_{p1}^2}\cdot\sqrt{\omega^2+\omega_{p2}^2}\cdot\sqrt{\omega^2+\omega_{p3}^2}}$$

where

$\omega z = 2\pi\ (0.64 \times 10^9)$ for upstream device compliance

and

$\omega p1 = 2\pi\ (2.7 \times 10^9)$

$\omega p2 = 2\pi\ (4.5 \times 10^9)$

$\omega p3 = 2\pi\ (13.5 \times 10^9)$

Figure 140 Transfer Function of the CTLE model for HBR2

Table 131 CTLE Model for HBR2

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	0.64 GHz	0.64 GHz
Pole 1 Frequency	2.7 GHz	2.7 GHz
Pole 2 Frequency	4.5 GHz	4.5 GHz
Pole 3 Frequency	13.5 GHz	13.5 GHz

For main link, use the following CTLE parameters for HBR25 (6.75 Gbps):

- DC-Gain = 1.0
- Zero = 1 GHz
- Pole1 = 3.75 GHz
- Pole2 = 13.5 GHz
- Pole3 $\geq$ 13.5 GHz

Table 132 CTLE Model for HBR25

CTLE Parameter	Worst Case Cable Model	Zero Length Cable Model
Gain	1.0	1.0
Zero Frequency	1.0 GHz	2.0 GHz
Pole 1 Frequency	5.625 GHz	3.375 GHz
Pole 2 Frequency	13.5 GHz	5.625 GHz
Pole 3 Frequency	13.5 GHz	16.875 GHz

Clock Recovery

When Clock Recovery is required, the clock recovery technique follows the definition of the receiver PLL as defined in Section 3.5.3.5 of the VESA DisplayPort 1.2a Standard. For main link, use the second-order clock recovery function with a closed loop tracking bandwidth and damping factor, with respect to the PRBS7 pattern, as shown in Table 133:

Table 133 Main Link Second-Order Clock Recovery Function

Bit Rate	Band wid th	Damping Factor
HBR25 (6.75 Gbps)	10 MHZ	1.00
HBR2 (5.4 Gbps)	10 MHz	1.00
HBR (2.7 Gbps)	10 MHz	1.51
RBR (1.62 Gbps)	5.4 MHz	1.51

Test Point Definition for SlimPort Source Tests

Test the Source DUT at Test Point 2 (TP2) as shown in Figure 141.

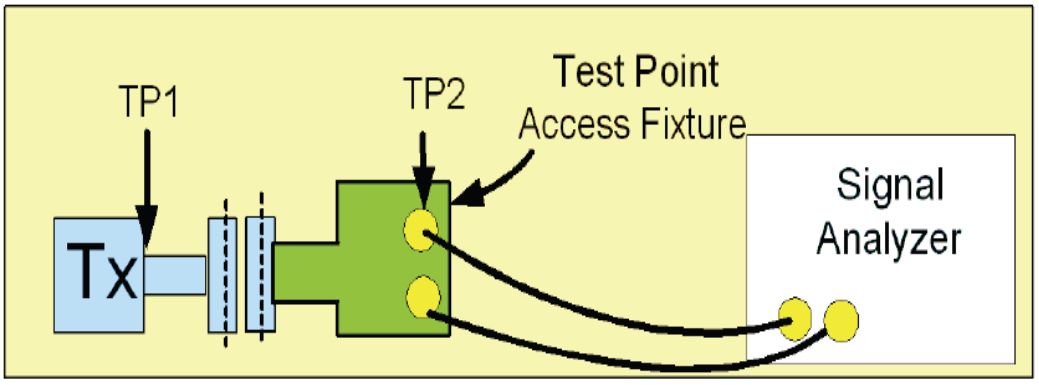


Figure 141 Test Point 2 Connection for SlimPort Source Tests

Use MyDP Test Fixtures (MyDP-to-DP type or MyDP-to-SMA type) to perform PHY compliance tests specific to SlimPort. Figure 142 shows the layout of a MyDP passive cable adapter or a MyDP protocol converter:

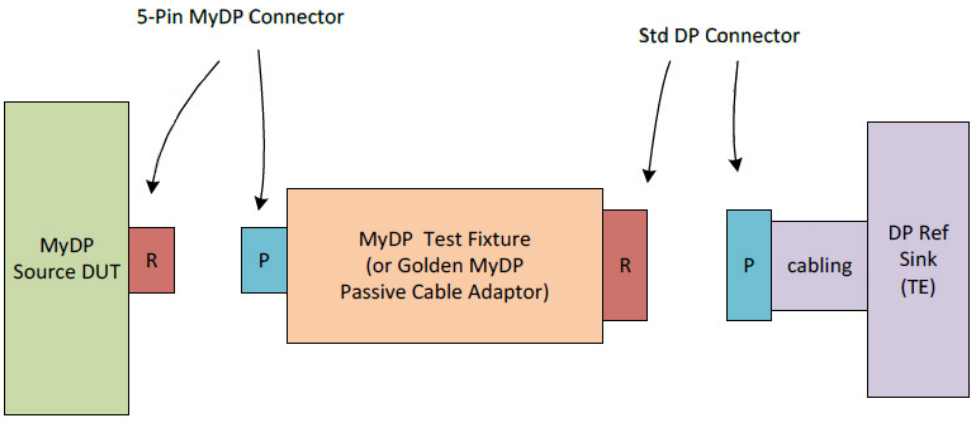


Figure 142 Schematics of SlimPort to SMA Test Fixtures used for PHY Compliance Tests

Table 134 defines the test point fixtures and instruments used for SlimPort (MyDP HBR25) Source Tests:

Table 134 Test Point Fixtures and Instruments for SlimPort (MyDP HBR25) Source Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests

Perform the following steps before you run the compliance tests on the source device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 143).

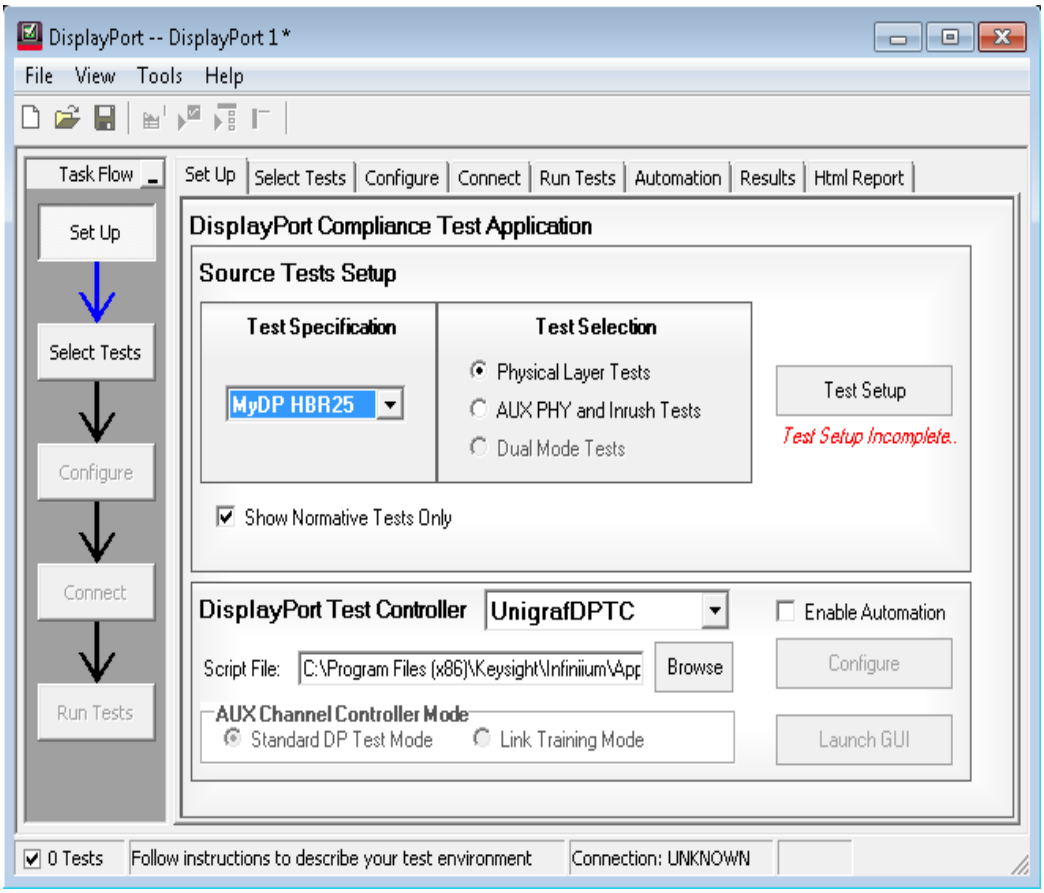


Figure 143 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with SlimPort Standards, select **MyDP HBR25** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for SlimPort Source Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

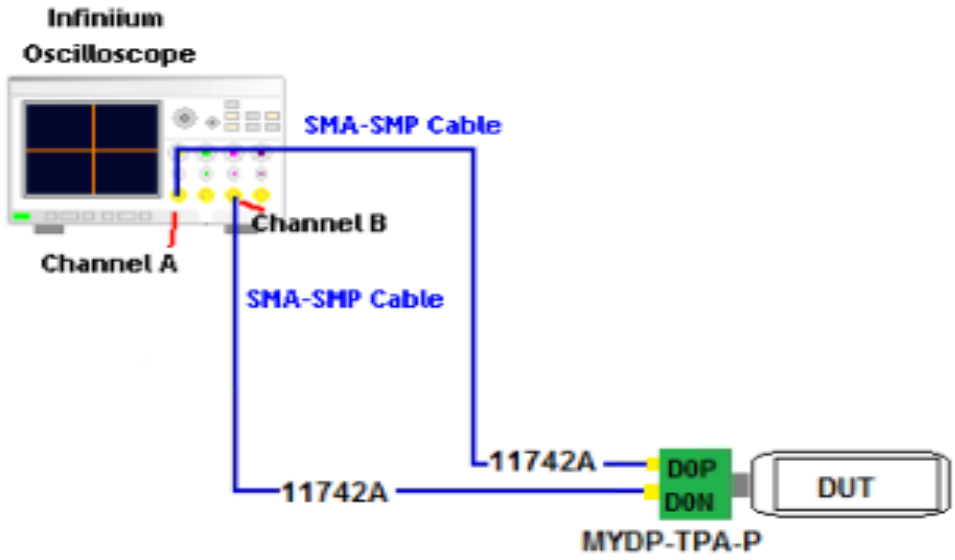


Figure 144 Sample connection diagram for SlimPort Source Tests

Source Eye Diagram Test

Test ID

1210001 – Eye Diagram Test

Test Overview

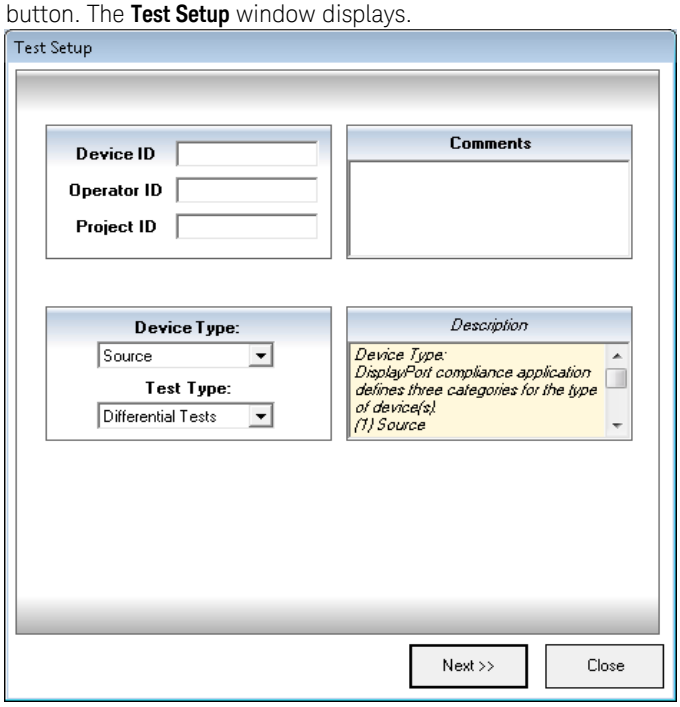
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



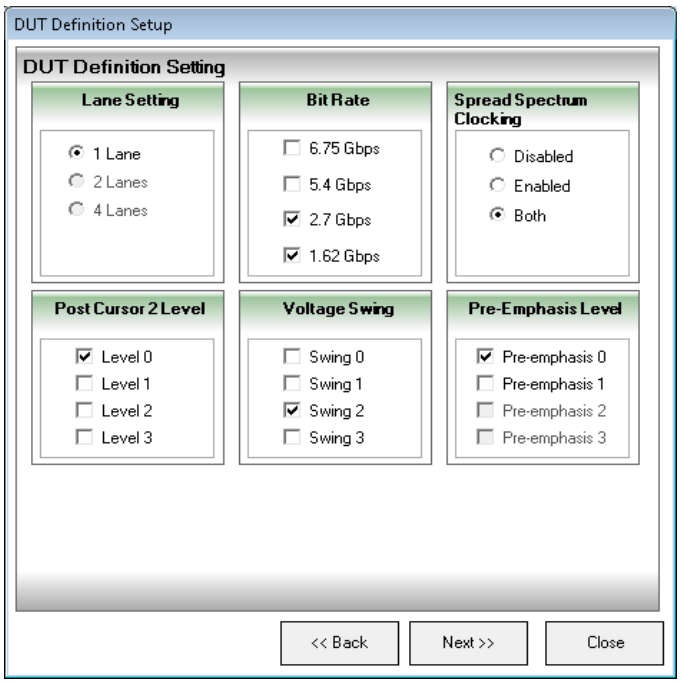
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

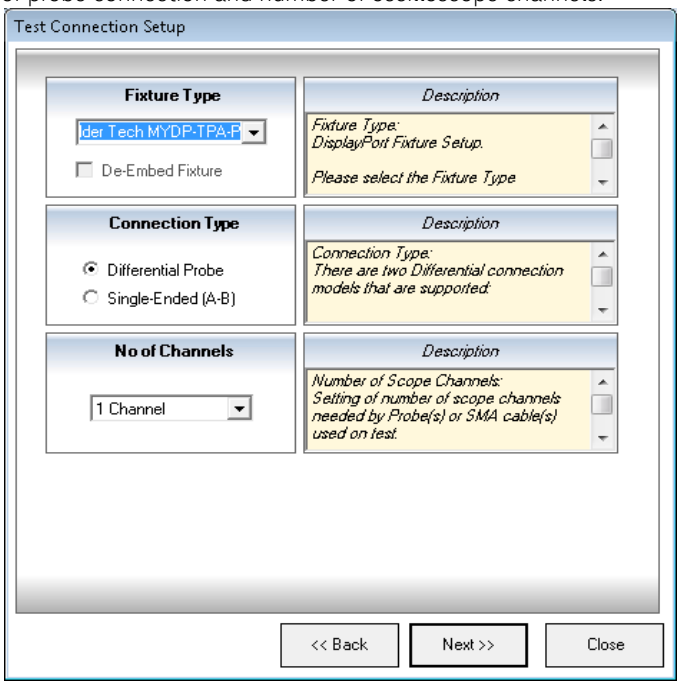
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

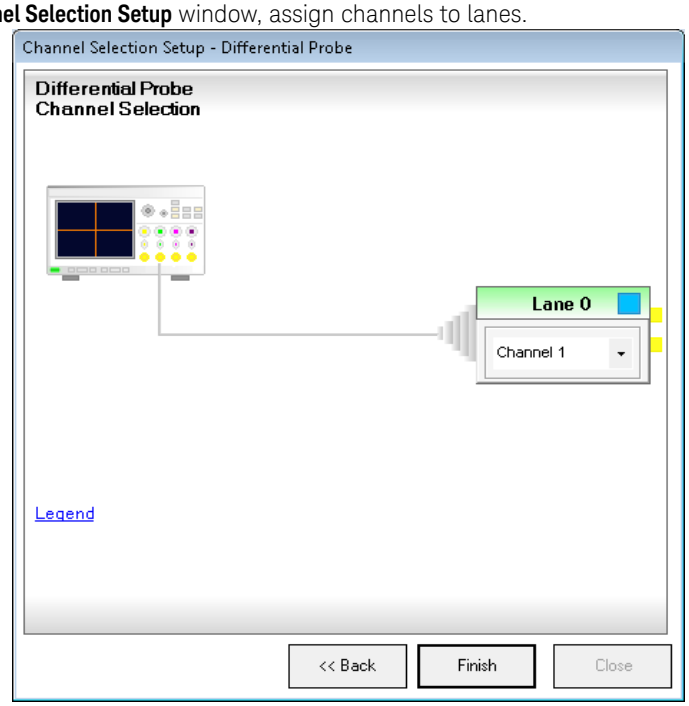
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

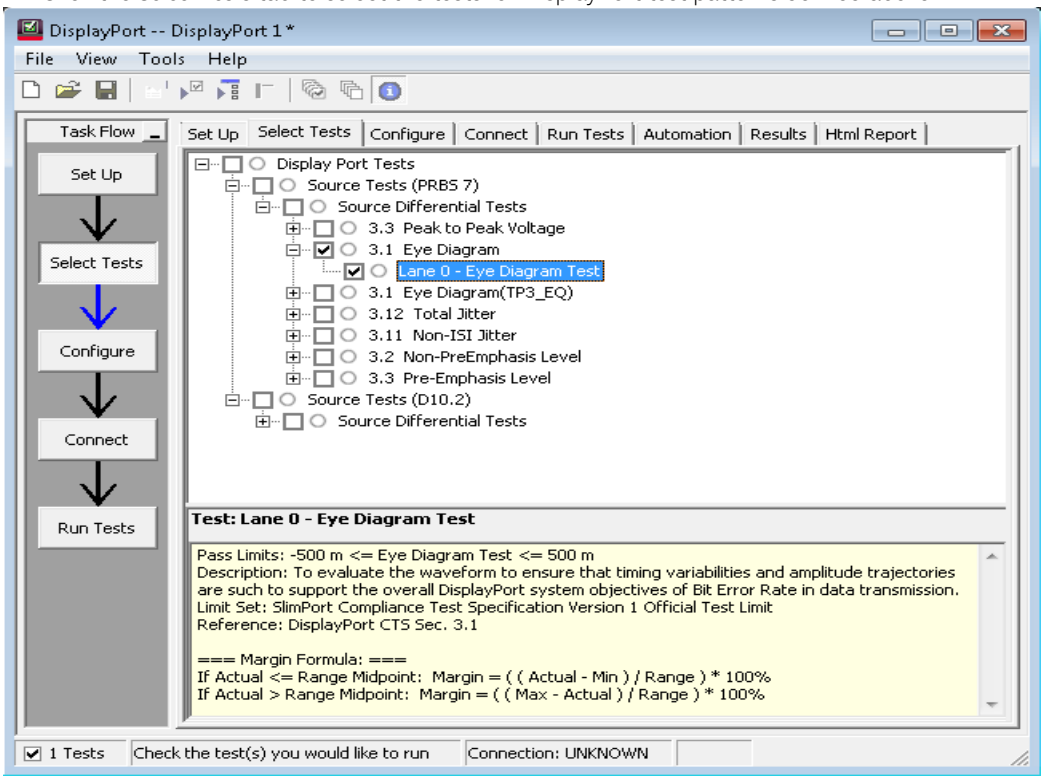


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure V_{TOP} and V_{BASE} of the input signal using the pattern folding.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the input signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the eye height of the eye diagram using the Histogram.
9 Measure the jitter of the eye diagram using the Histogram.
10 Calculate the eye width based on the measured jitter of the eye diagram.
11 Check for any signal trajectories that may have entered into the mask.
12 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 135 shows the voltage and time coordinates for the mask used in the eye diagram.

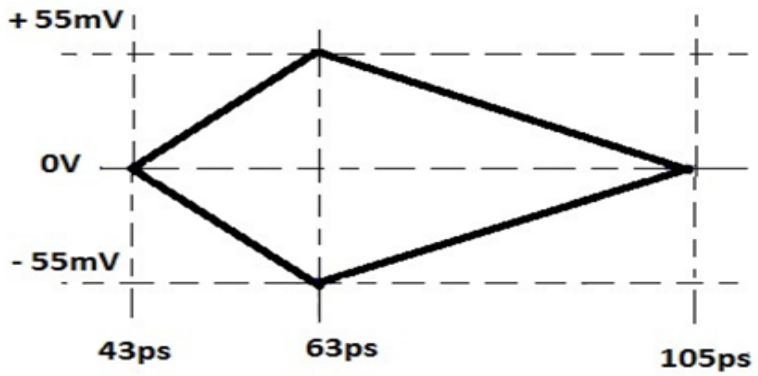


Figure 145 Eye Mask of Source at 6.75G

Table 135 Eye Diagram Mask Coordinates

Mask Point	Bit Rate	
	Reduced (1.62 Gb/s)	High (2.7 Gb/s)
1	0.127, 0.000	0.210, 0.000
2	0.291, 0.160	0.355, 0.140
3	0.500, 0.200	0.500, 0.175
4	0.709, 0.200	0.645, 0.175
5	0.873, 0.000	0.790, 0.000
6	0.709,-0.200	0.645,-0.175
7	0.500,-0.200	0.500,-0.175
8	0.291,-0.160	0.355,-0.140

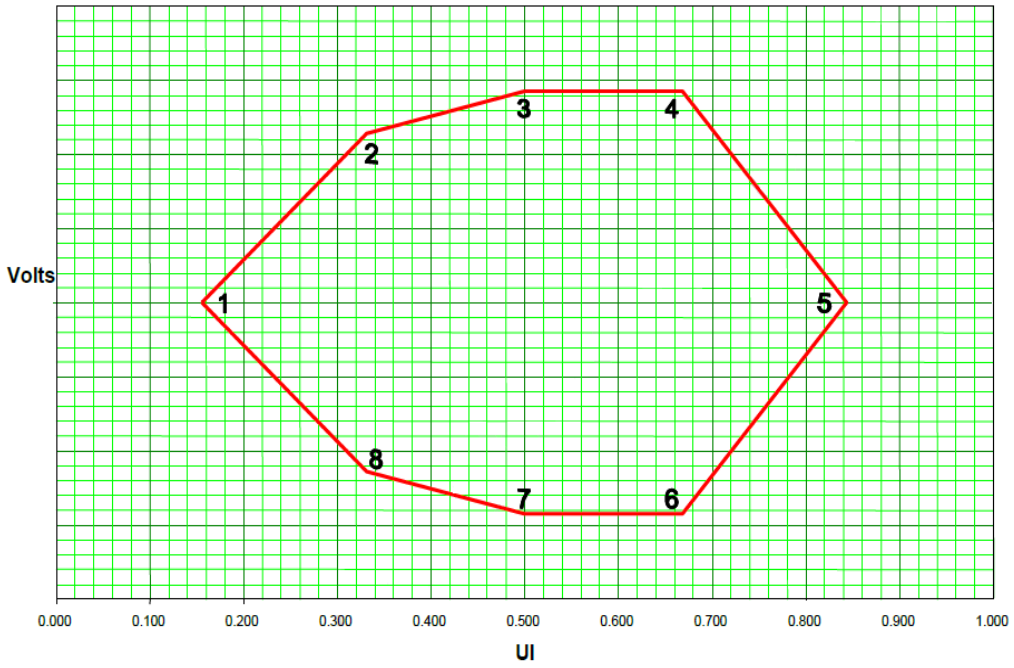


Figure 146 The Source Eye Mask

Mask Test: Zero mask failures.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-24 for RBR and Table 3-23 for HBR*

Expected/Observable Results

The measured eye diagram for the source degraded signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Source Total Jitter Test

Test ID

1220001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

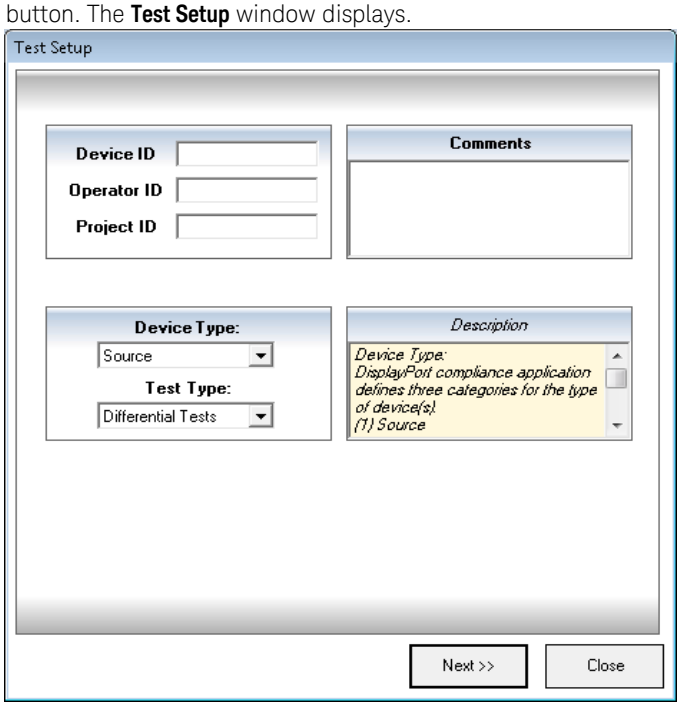
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



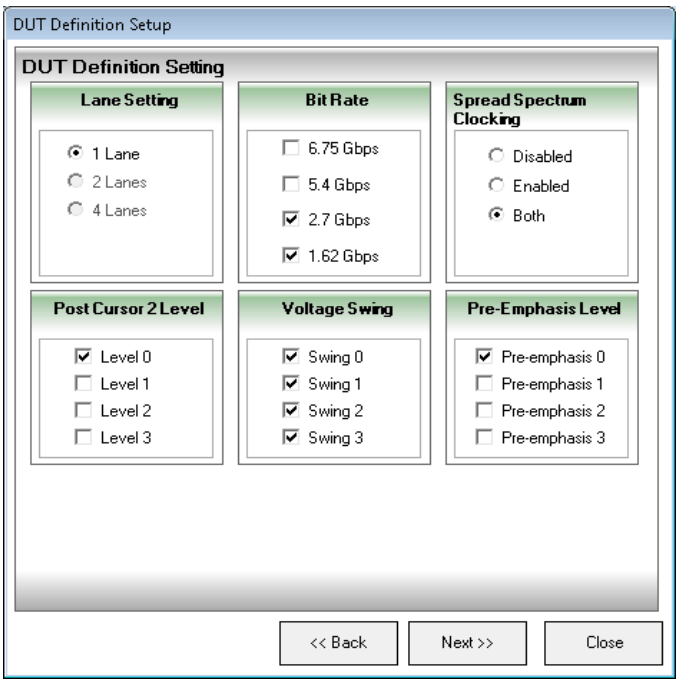
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

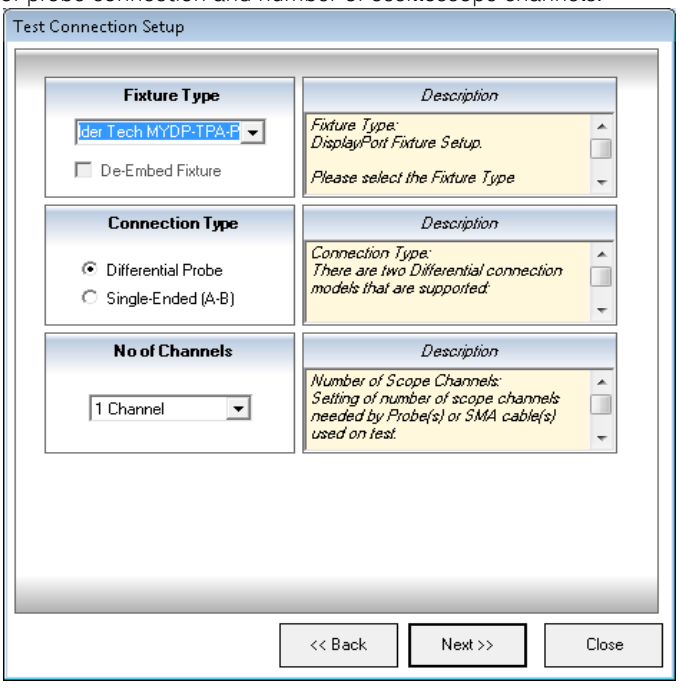
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

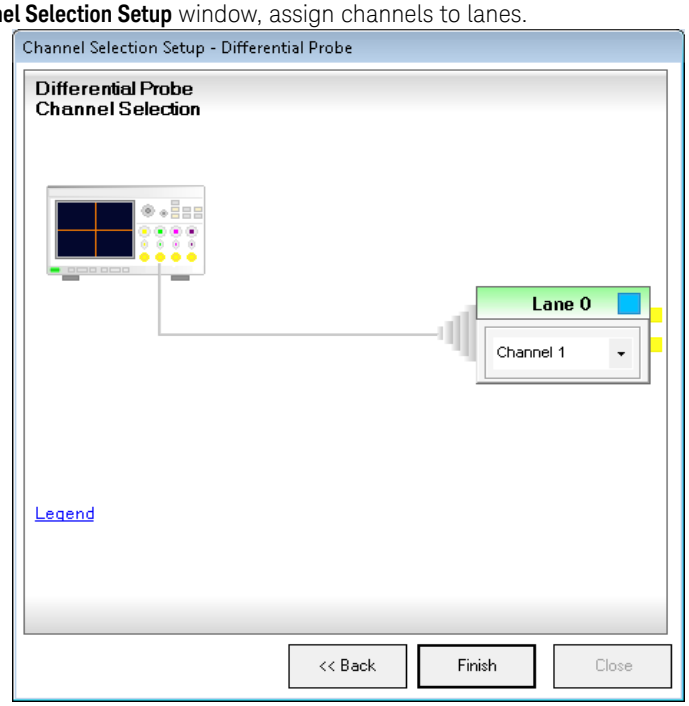
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

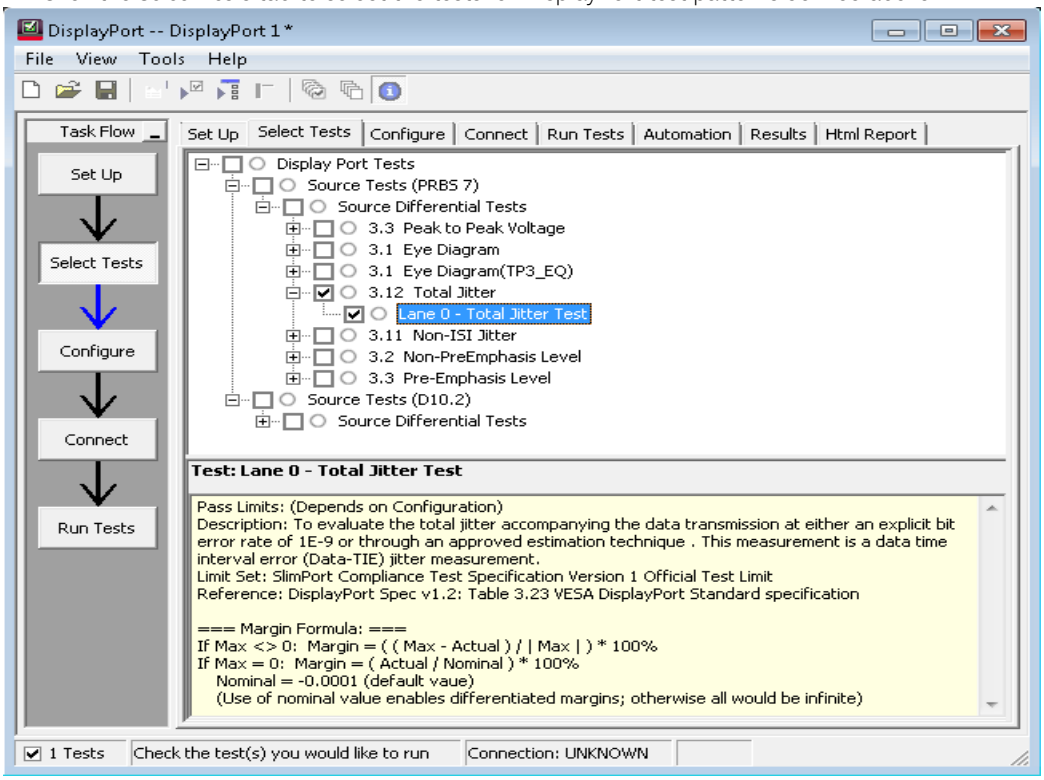


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Report the measurement results.

PASS Condition

Table 136 Total Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
Ap-p	0.294 UI	0.420 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
Ap-p	0.180 UI	0.270 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non-ISI Jitter Test

Test ID

1230001 – Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the amount of Non ISI jitter accompanying the data transmission.

The jitter is separated into each jitter components based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

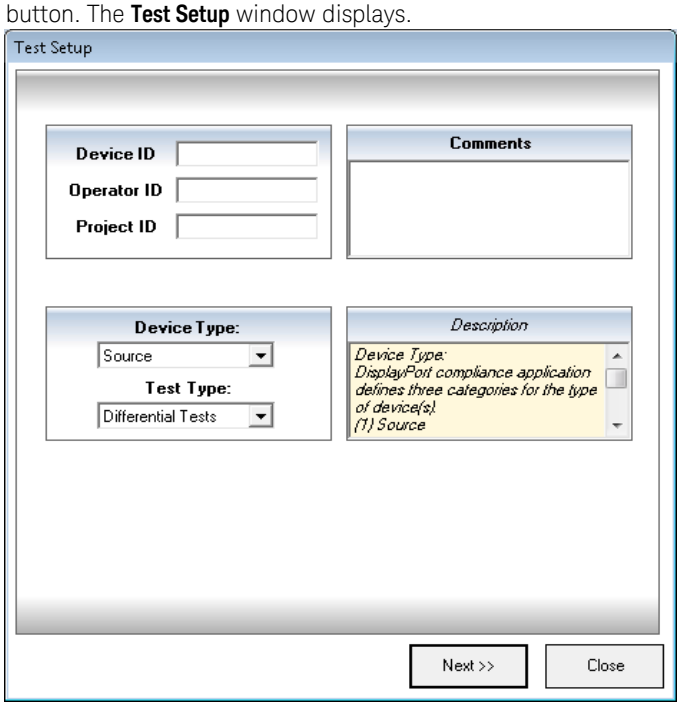
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	RBR, HBR
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All Voltage Levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



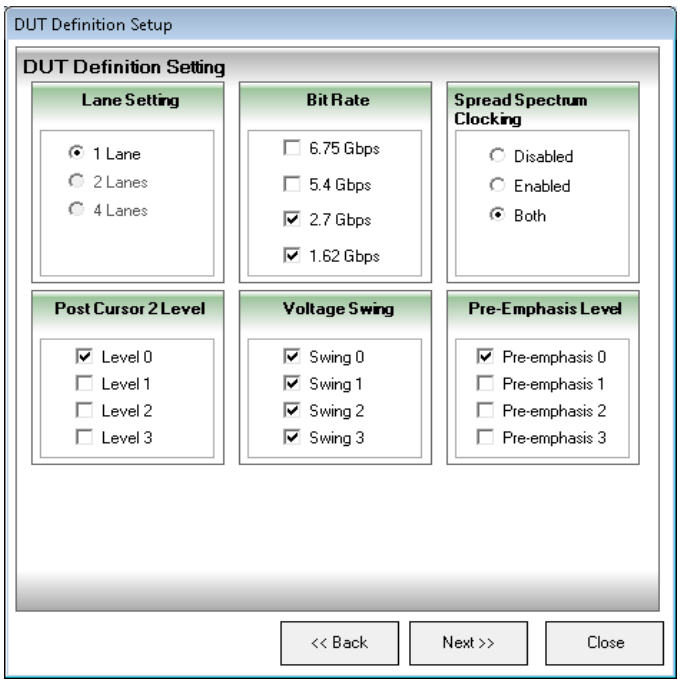
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

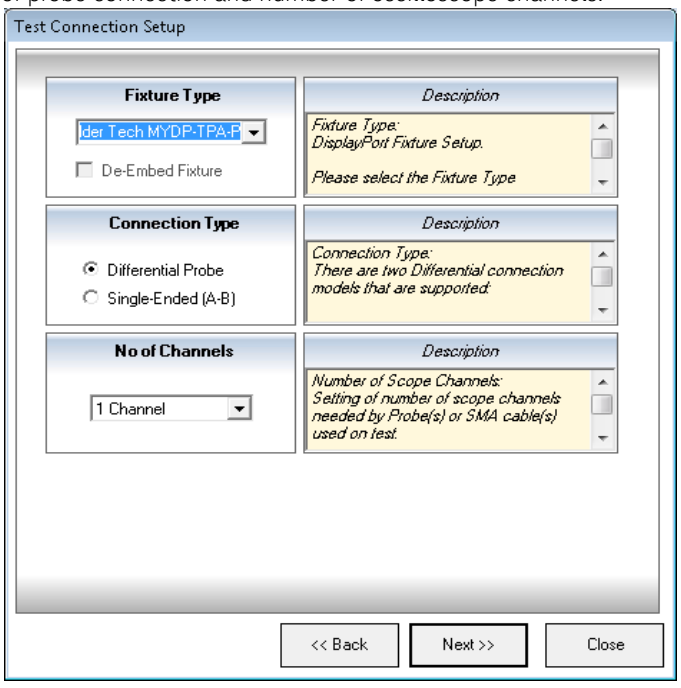
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

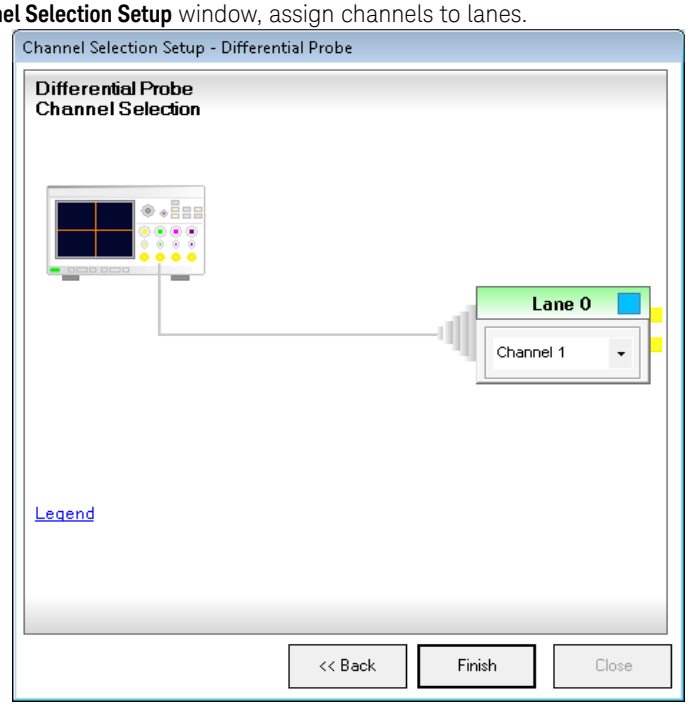
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

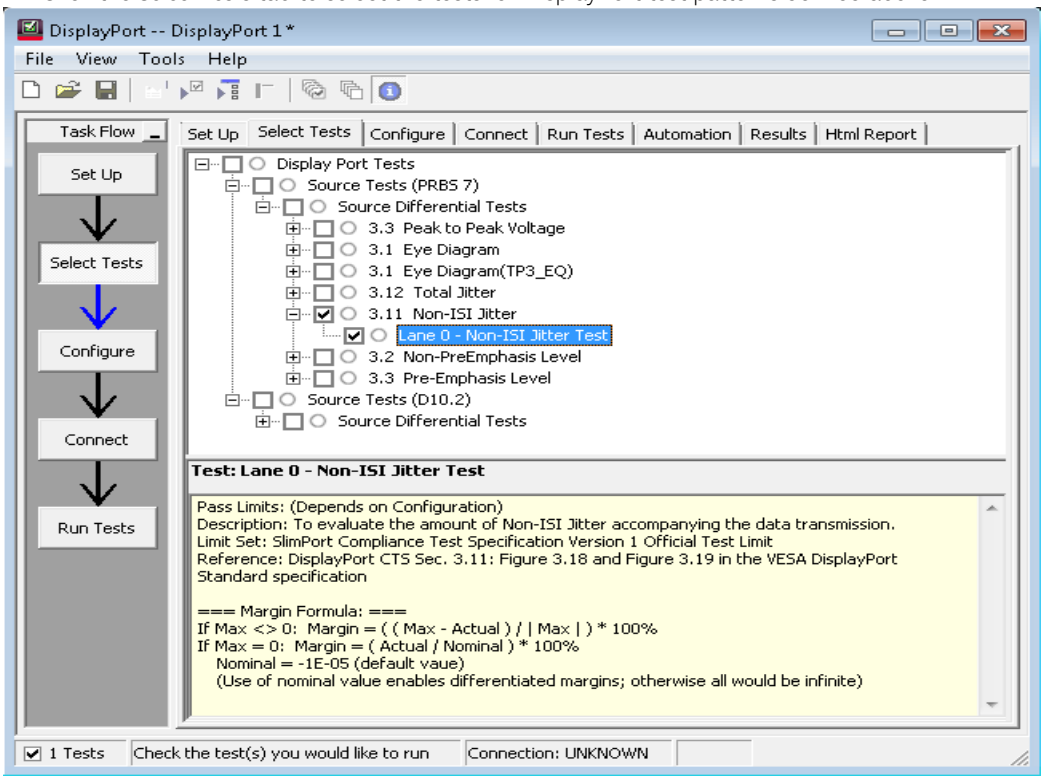


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
5 Note the jitter component value from the EZJIT Plus/Complete Software.
6 Calculate the Non ISI jitter using the following equation:

$$\text{Non ISI Jitter} = TJ - ISI$$

7 Report the measurement results.

PASS Condition

Table 137 Non-ISI Jitter at Internal and Compliance Points.

	Transmitter package pin	Transmitter Connector (TP2)
High-bit Rate (2.7 Gb/s per lane)		
A_{p-p}	0.260 UI	0.276 UI
Reduced-bit Rate (1.62 Gb/s per lane)		
A_{p-p}	0.160 UI	0.210 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.11*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1261001 – Non Pre-Emphasis Level Test (Swing 1/Swing 0)
- 1262001 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263001 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

For HBR2 and HBR25:

- 1264101 – Non Pre-Emphasis Level Test (Swing 2/Swing 0)
- 1262101 – Non Pre-Emphasis Level Test (Swing 2/Swing 1)
- 1263101 – Non Pre-Emphasis Level Test (Swing 3/Swing 2)

Test Overview

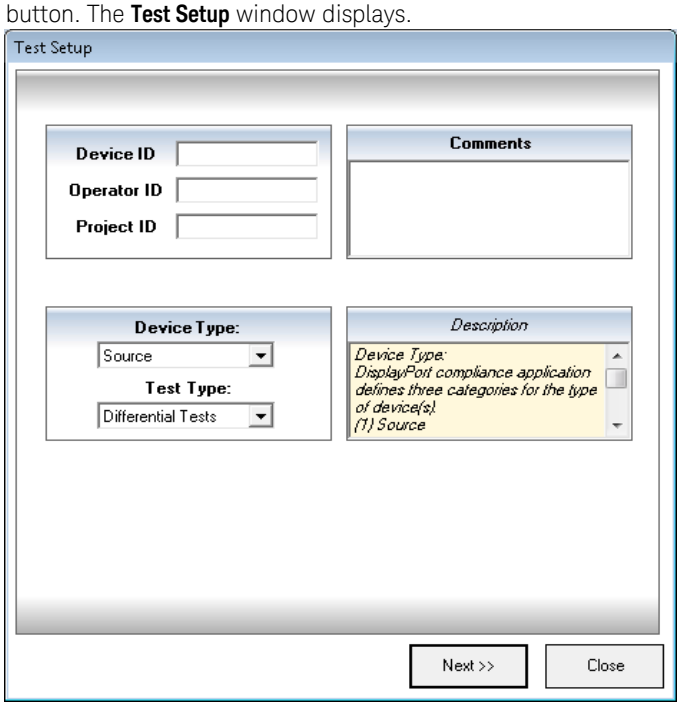
The objective of this test is to ensure that the system budget elements are obeyed and to ensure that the level settings are monotonic so that the sink relies on the source to incrementally increase upon request by the sink.

Test Conditions for Non Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions are supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2 and HBR25 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



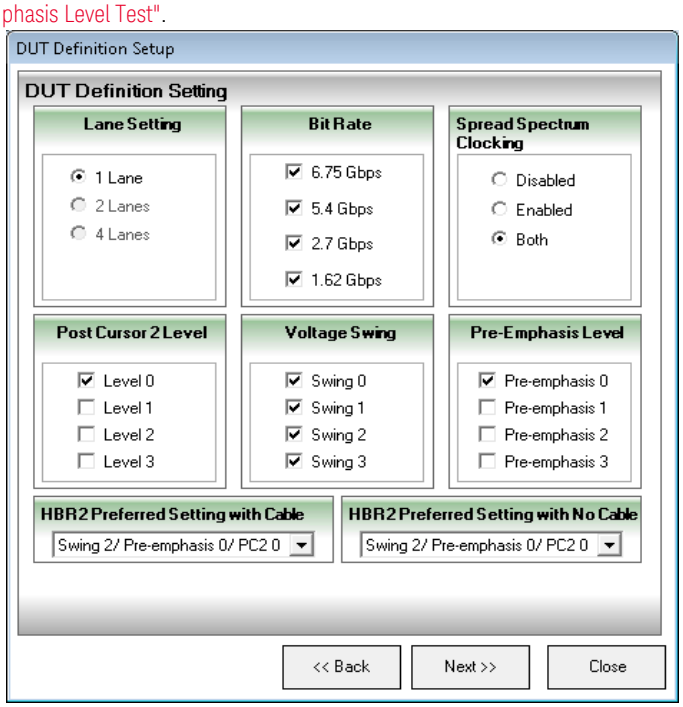
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

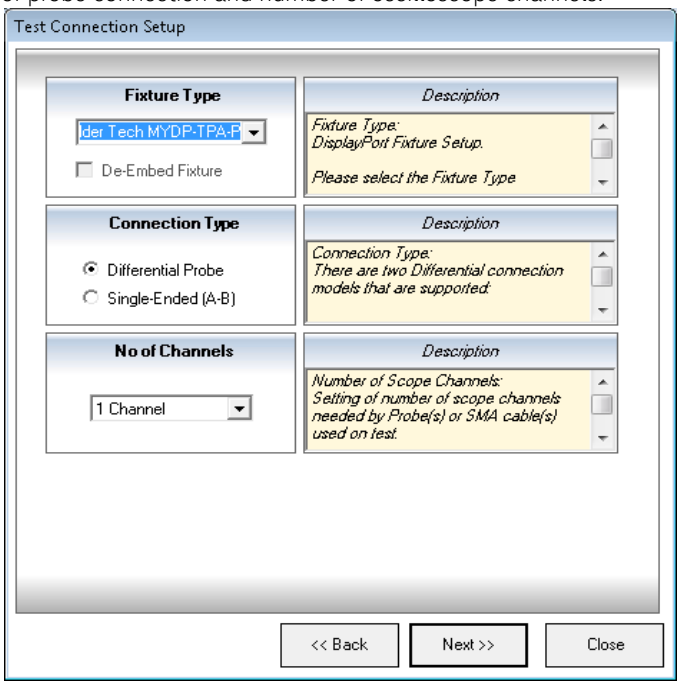
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

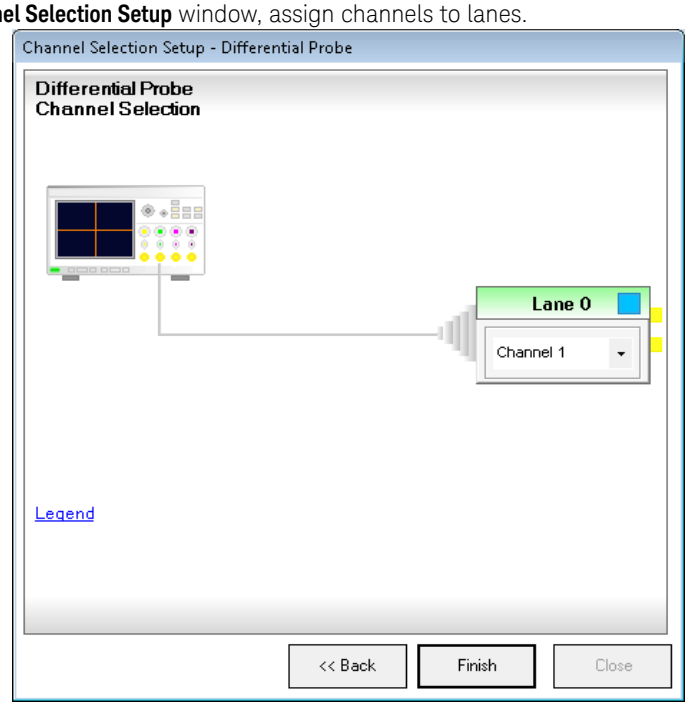
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non Pre-Emphasis Level Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

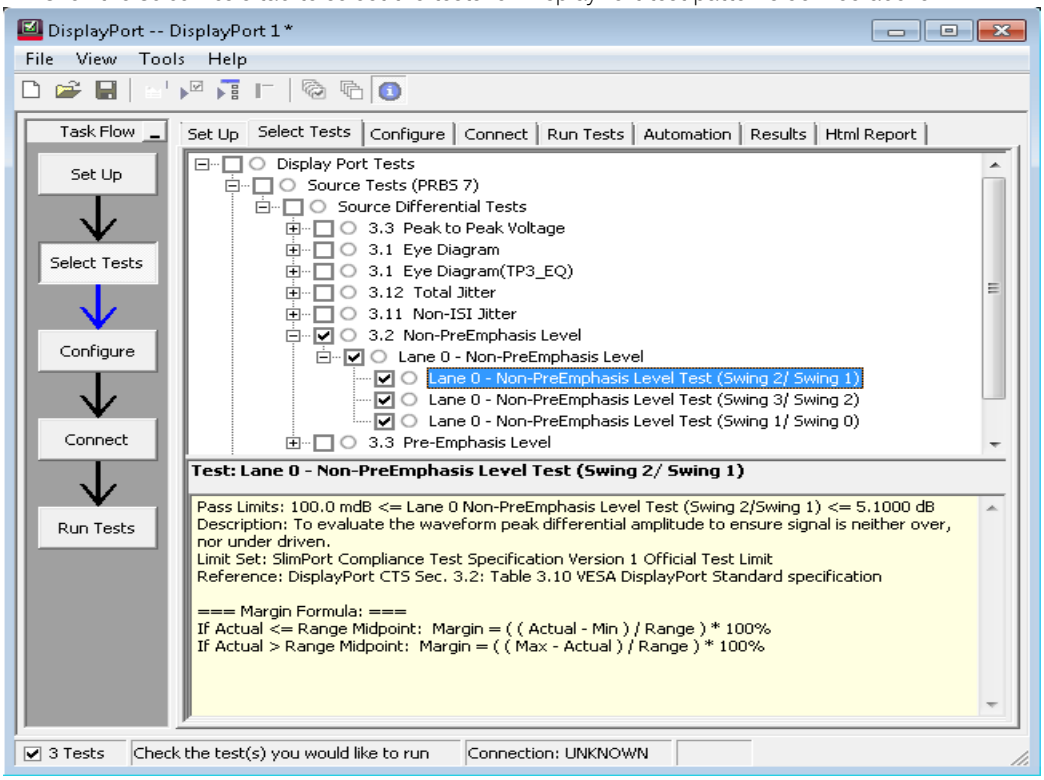


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For Voltage Level A with no pre-emphasis level:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

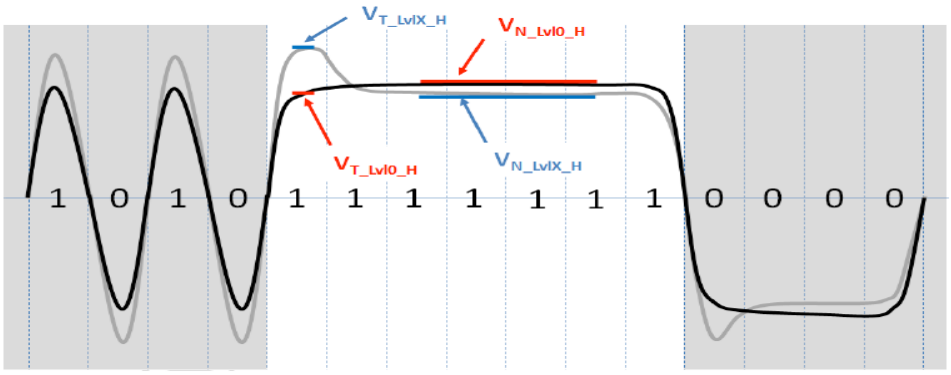


Figure 147 High Voltage measurement for RBR and HBR

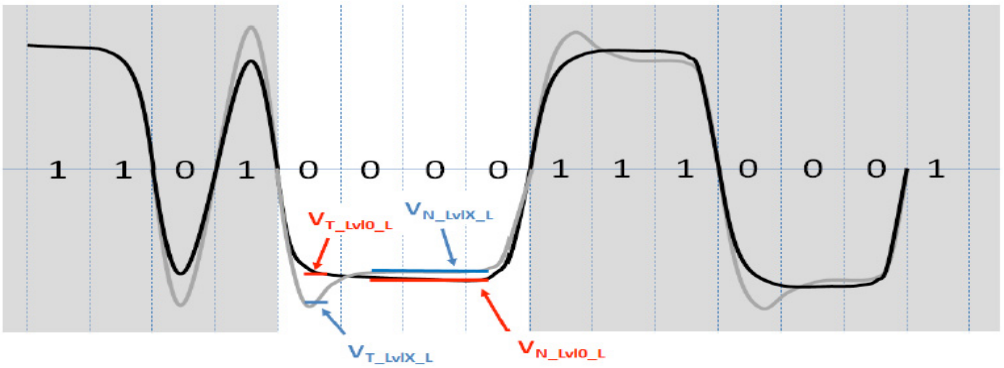


Figure 148 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR25 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level 0 (non pre-emphasis level):

- The transition voltage measurement, $V_{T\_Lvl0\_H}$ and $V_{T\_Lvl0\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_Lvl0\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_Lvl0\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

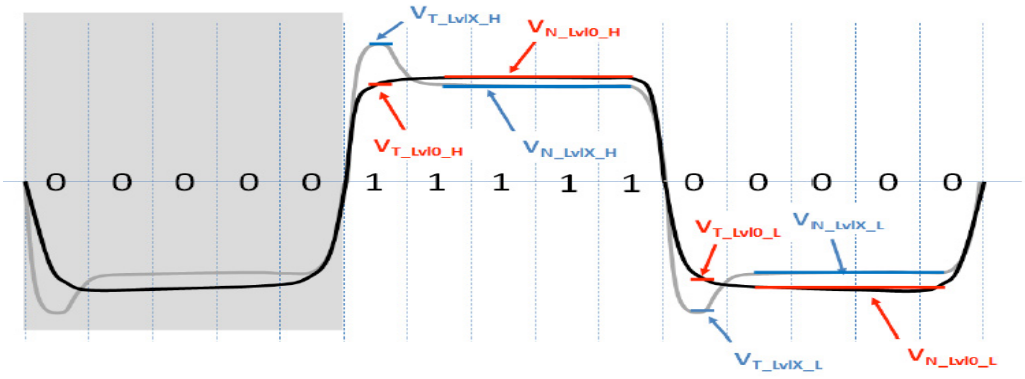


Figure 149 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_Lvl0\_PP} = V_{T\_Lvl0\_H} - V_{T\_Lvl0\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_Lvl0\_PP} = V_{N\_Lvl0\_H} - V_{N\_Lvl0\_L}$$

2 Repeat Step 1 for Voltage Level B with no pre-emphasis level.

3 Calculate the non pre-emphasis level output voltage ratio using the equation:

Non Pre-Emphasis Level = $20 * Log_{10}[\text{Voltage Level A } V_{N\_Lvl0\_PP} / \text{Voltage Level B } V_{N\_Lvl0\_PP}]$

4 Report the measurement results.

PASS Condition

For each level setting testes, the following equation should be used:

Resultant = $20 * Log_{10}[\text{Voltage}_{\text{Peak-Peak\_LevelA}} / \text{Voltage}_{\text{Peak-Peak\_LevelB}}]$

Table 138 Compared Levels

Measurement#	$\text{Voltage}_{\text{Peak-Peak\_LevelA}}$	$\text{Voltage}_{\text{Peak-Peak\_LevelB}}$
RBR & HBR		
1	Level 1 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
2	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
3*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
HBR2 and HBR25		
4	Level 2 (0 dB Pre-emphasis nominal)	Level 0 (0 dB Pre-emphasis nominal)
5	Level 2 (0 dB Pre-emphasis nominal)	Level 1 (0 dB Pre-emphasis nominal)
6*	Level 3 (0 dB Pre-emphasis nominal)	Level 2 (0 dB Pre-emphasis nominal)
* if device optionally capable of Level 3		

The resultants specifications are as identified below:

Measurement 1: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 2: 0.1 dB ≤ Resultant ≤ 5.1 dB

Measurement 3: 0.8 dB ≤ Resultant ≤ 6.0 dB

Measurement 4: 5.2 dB ≤ Resultant ≤ 6.9 dB

Measurement 5: 1.6 dB ≤ Resultant ≤ 3.5 dB

Measurement 6: 1 dB ≤ Resultant ≤ 4.4 dB

Table 139 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX\text{-}OUTPUT\text{-}RATIO\_RBR\_HBR}$	Ratio of Output Voltage Level 1/Level 0	0.8	-	6.0	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	0.1	-	5.1	dB	
	Ratio of Output Voltage Level 3/Level 2	0.8	-	6.0	dB	
$V_{TX\text{-}OUTPUT\text{-}RATIO\_HBR2}$	Ratio of Output Voltage Level 2/Level 0	5.2	-	6.9	dB	Measured on non-transition bits at Pre-emphasis level 0 setting
	Ratio of Output Voltage Level 2/Level 1	1.6	-	3.5	dB	
	Ratio of Output Voltage Level 3/Level 2	1	-	4.4	dB	

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level ratio of the non pre-emphasis level test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Pre-Emphasis Level Test

Test ID

For RBR and HBR:

- 1270001 — Pre-Emphasis Level Test

For HBR2 and HBR25:

- 1270501 — Pre-Emphasis Level Test

Test Overview

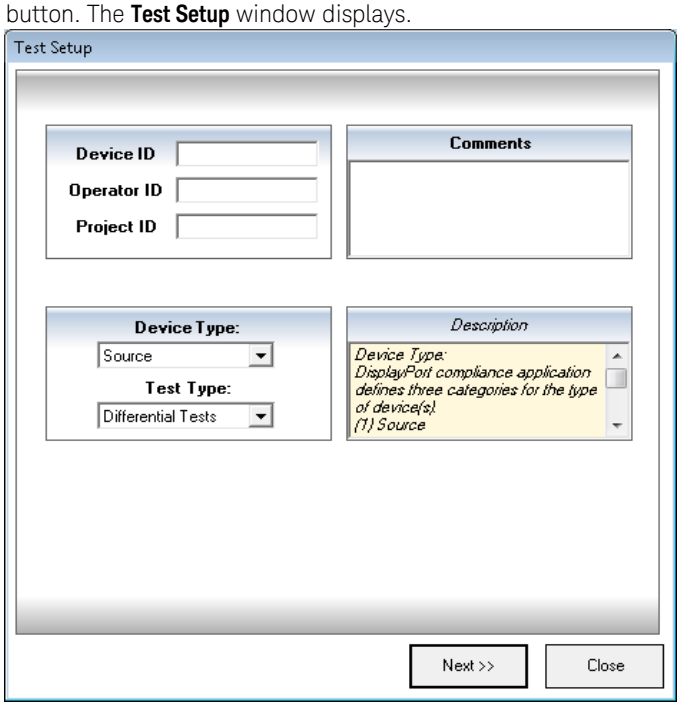
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings.

Test Conditions for Pre-Emphasis Level Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR25 – PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



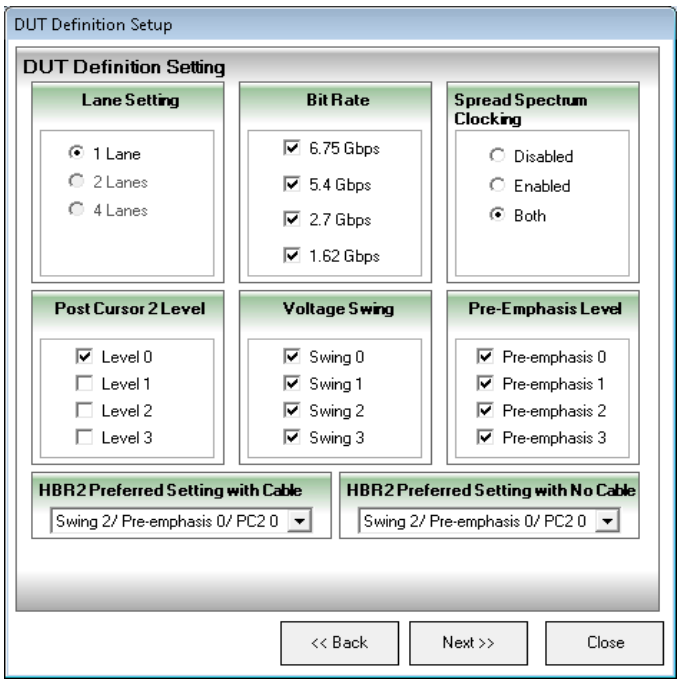
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

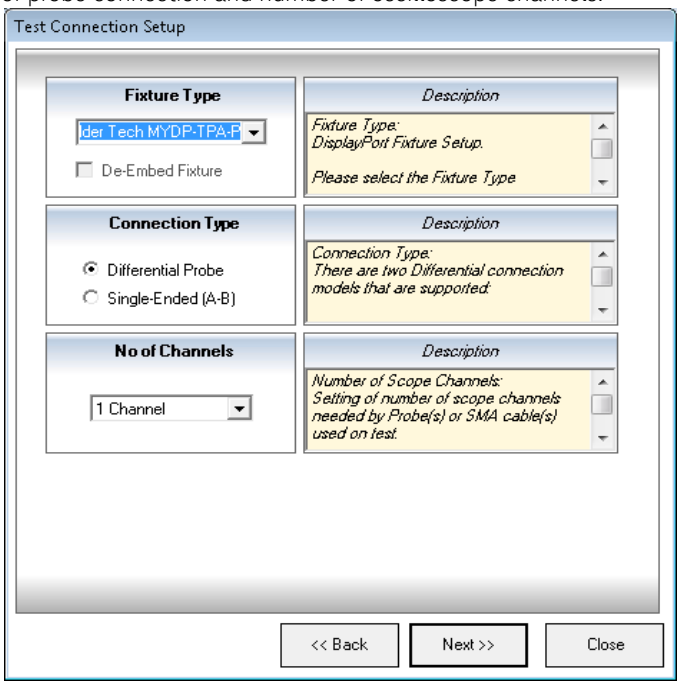
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

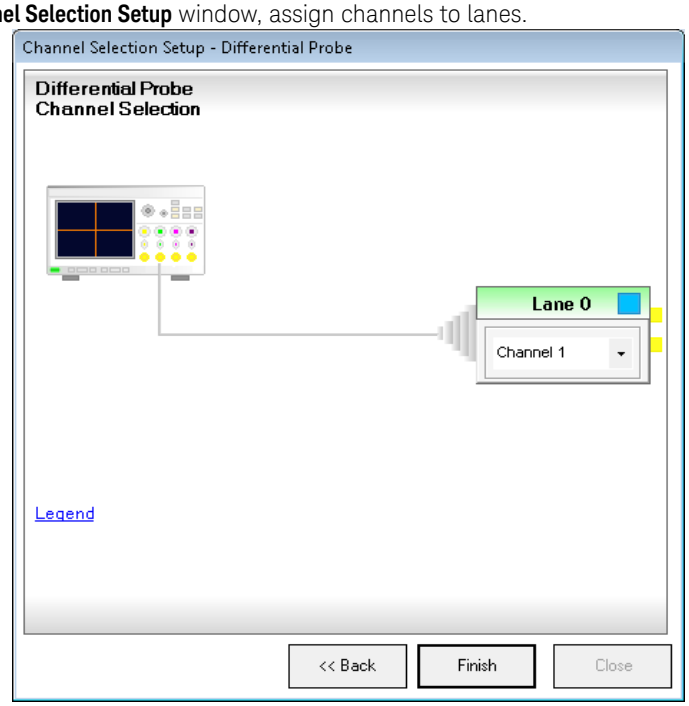
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Pre-Emphasis Level Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

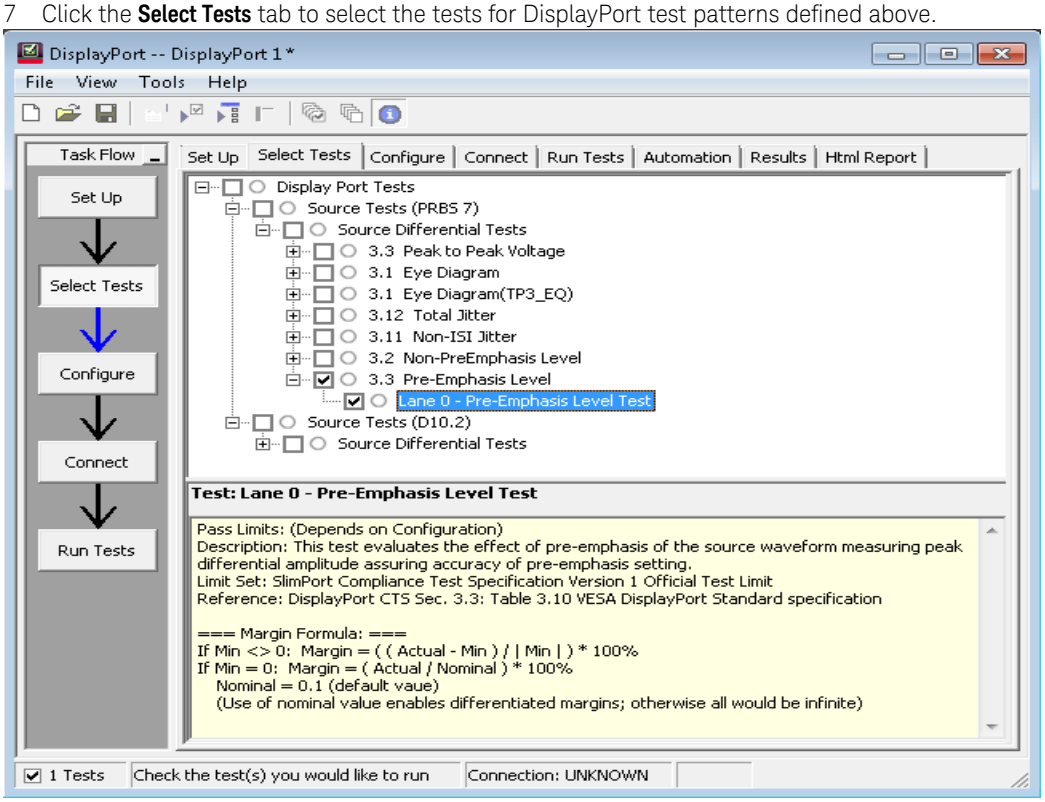


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level and a Pre-Emphasis Level X:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

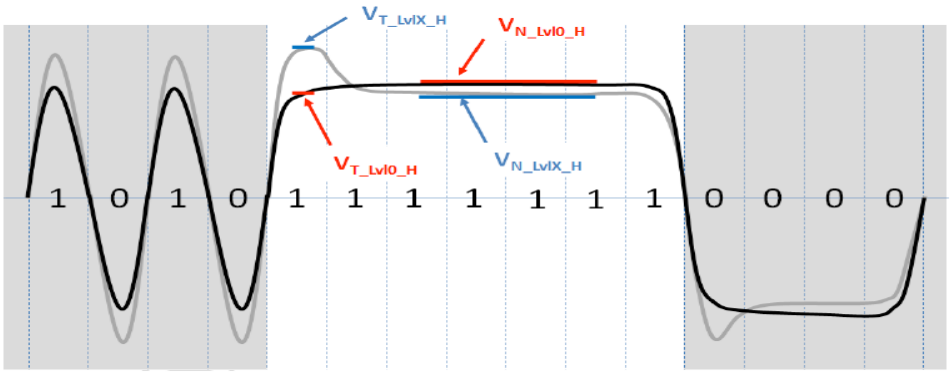


Figure 150 High Voltage measurement for RBR and HBR

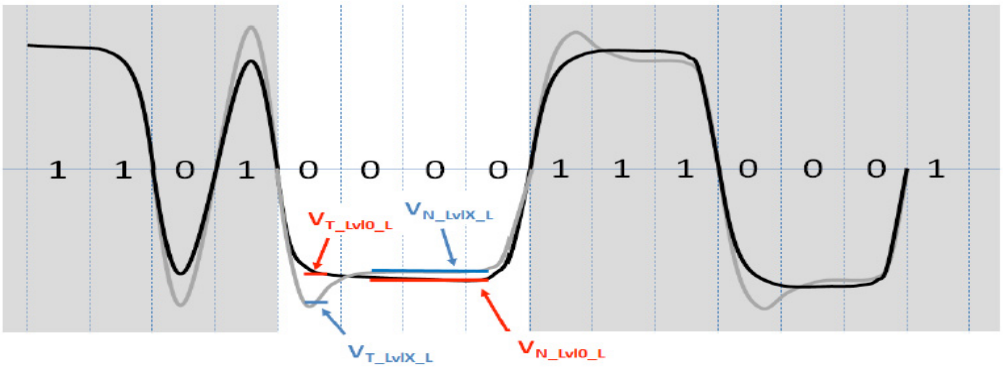


Figure 151 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR25 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

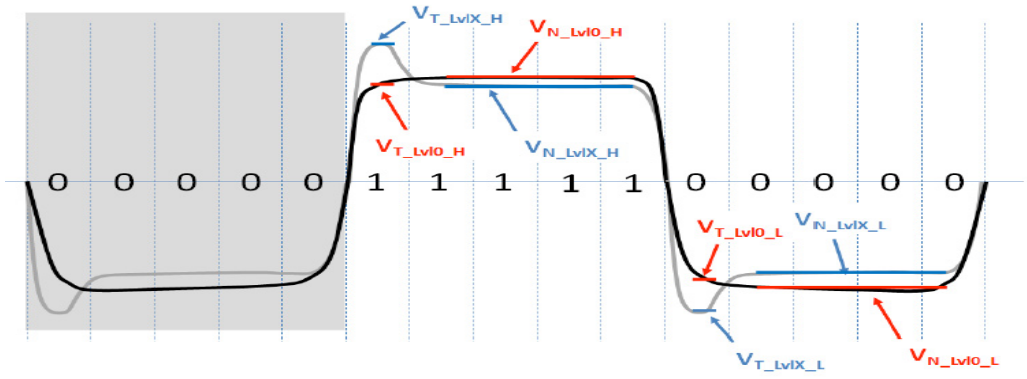


Figure 152 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

l Calculate the pre-emphasis level using the equation:

$$\text{Pre-Emphasis}_{LvlX} = 20 * \text{Log}_{10}[V_{T\_LvlX\_PP} / V_{N\_LvlX\_PP}]$$

2 For Pre-Emphasis Level 0 (no pre-emphasis level), the result for $\text{Pre-Emphasis}_{Lvl0}$ is compared with the maximum pre-emphasis disabled limit.

3 Repeat Step 1 for the next Pre-Emphasis level and for each Pre-Emphasis levels, compare the pre-emphasis delta with the pre-emphasis delta limits.

4 Calculate the pre-emphasis delta using the equation:

$$\text{Pre-Emphasis Delta (Level 1 vs Level 0)} = \text{Pre-Emphasis}_{Lvl1} - \text{Pre-Emphasis}_{Lvl0}$$

$$\text{Pre-Emphasis Delta (Level 2 vs Level 1)} = \text{Pre-Emphasis}_{Lvl2} - \text{Pre-Emphasis}_{Lvl1}$$

$$\text{Pre-Emphasis Delta (Level 3 vs Level 2)} = \text{Pre-Emphasis}_{Lvl3} - \text{Pre-Emphasis}_{Lvl2}$$

5 Report the measurement results.

PASS Condition

Pre-emphasis values for the Level 0 (OFF) state (Normative)

Level 0 (OFF) Pre-emphasis measurement:

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for all supported levels.

Level 0 (OFF) Pre-emphasis Measurement condition: +0.25 dB $\geq$ Resultant

Pre-emphasis Delta values for:

a Level 1 vs. Level 0 Pre-emphasis settings (NORMATIVE)

b Level 2 vs. Level 1 Pre-emphasis settings (NORMATIVE)

c Level 3 vs. Level 2 Pre-emphasis settings (NORMATIVE)

Pre-emphasis Delta measurements:

- Level 1 vs. Level 0

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl1\_PP} / \text{Voltage}_{N\_Lvl1\_PP}] - 20 * \text{Log}[\text{Voltage}_{T\_Lvl0\_PP} / \text{Voltage}_{N\_Lvl0\_PP}]$ for Voltage Swing Levels 0, 1 and 2.

- Level 2 vs. Level 1

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl2\_PP} / \text{Voltage}_{N\_Lvl2\_PP}] - 20 * \text{Log}[\text{Voltage}_{T\_Lvl1\_PP} / \text{Voltage}_{N\_Lvl1\_PP}]$ for Voltage Swing Levels 0 and 1.

- Level 3 vs. Level 2

Resultant = $20 * \text{Log}[\text{Voltage}_{T\_Lvl3\_PP} / \text{Voltage}_{N\_Lvl3\_PP}] - 20 * \text{Log}[\text{Voltage}_{T\_Lvl2\_PP} / \text{Voltage}_{N\_Lvl2\_PP}]$ for Voltage Swing Level 0, if supported.

Table 140 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
$V_{TX-PREEMP-OFF}$	Maximum Pre-emphasis when disabled	-	-	0.25	dB	Pre-emphasis Level 0 setting must not show any pre-emphasis at TP2 to prevent link training issues.
$V_{TX-PREEMP-DELTA}$	Delta of Pre-emphasis Level 1 vs. Level 0	2	-	-	dB	Applies to all valid voltage settings. Measured at Pre-emphasis Post Cursor2 Level 0. Support for Pre-emphasis Level 3 is optional.
	Delta of Pre-emphasis Level 2 vs. Level 1	1.6	-	-	dB	
	Delta of Pre-emphasis Level 3 vs. Level 2	1.6	-	-	dB	

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis level or pre-emphasis delta for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Non Transition Voltage Range Measurement Test

Test ID

For RBR and HBR:

- 1272001 – Non Transition Voltage Range Measurement (Swing 0)
- 1273001 – Non Transition Voltage Range Measurement (Swing 1)
- 1274001 – Non Transition Voltage Range Measurement (Swing 2)

For HBR2 and HBR25:

- 1272101 – Non Transition Voltage Range Measurement (Swing 0)
- 1273101 – Non Transition Voltage Range Measurement (Swing 1)
- 1274101 – Non Transition Voltage Range Measurement (Swing 2)

Test Overview

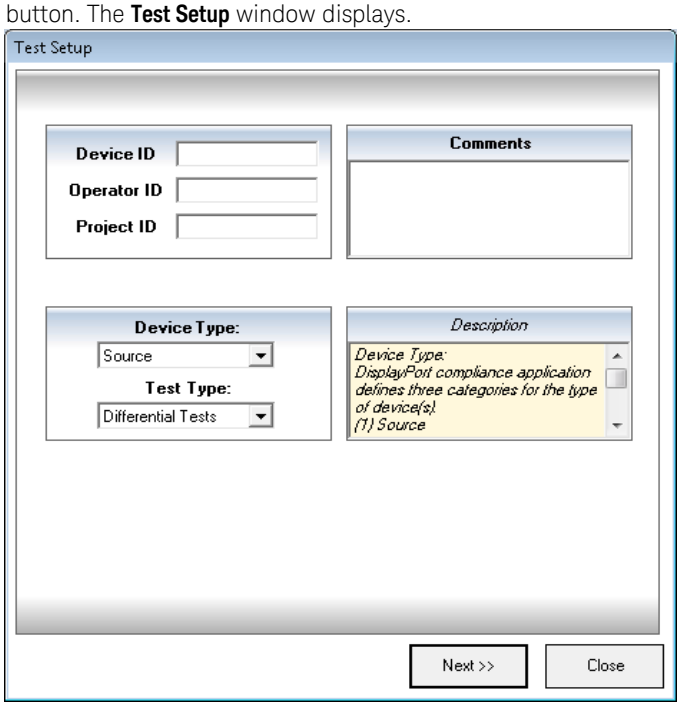
The objective of this test is to evaluate the effect of pre-emphasis of the source waveform by measuring the peak differential amplitude to assure accuracy of the pre-emphasis settings. Comparisons are also made for the Level 0 transition state as well as non-transition levels.

Test Conditions for Non Transition Voltage Range Measurement Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR25– PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



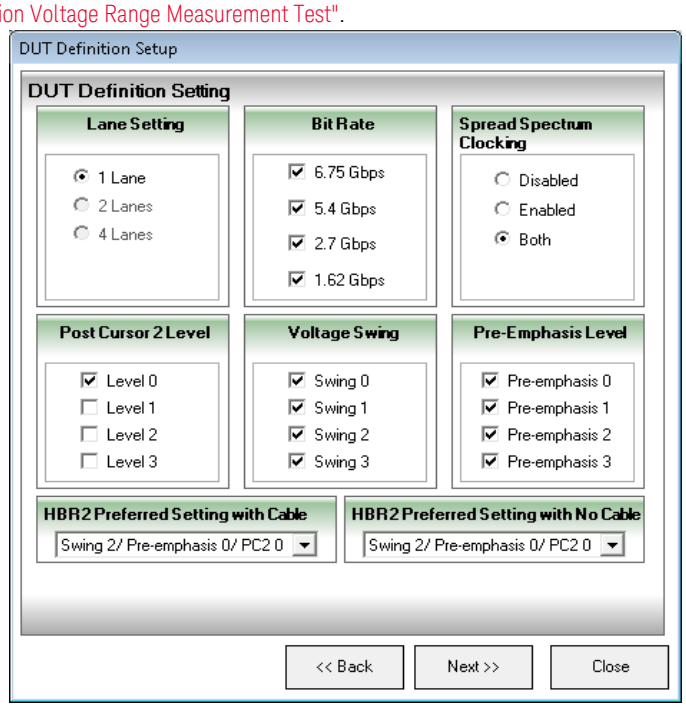
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

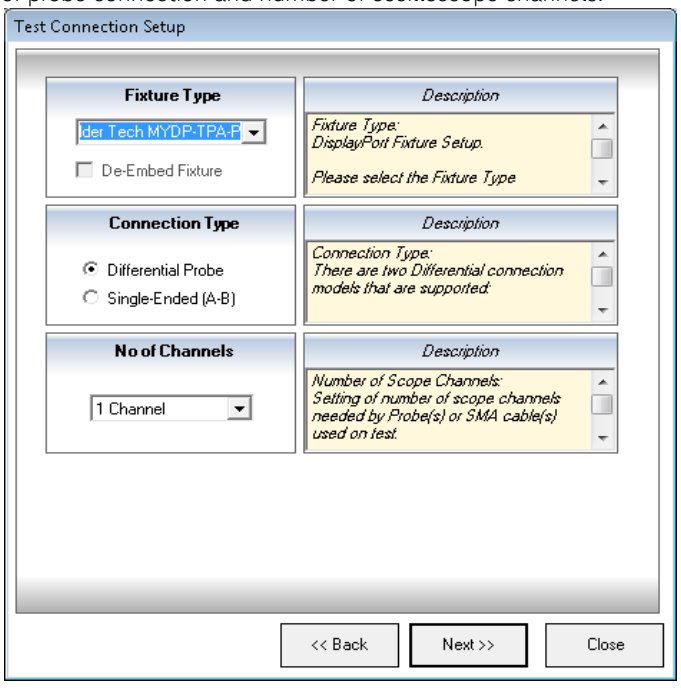
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

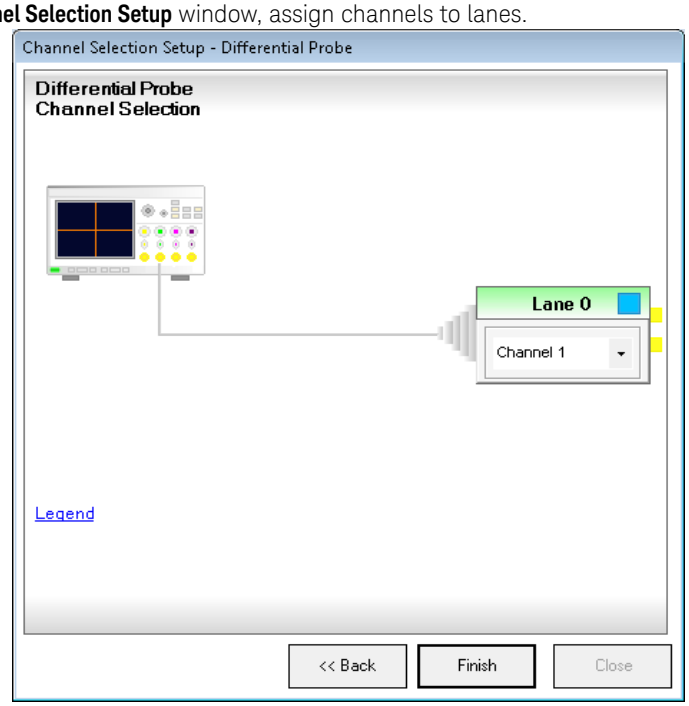
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non Transition Voltage Range Measurement Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

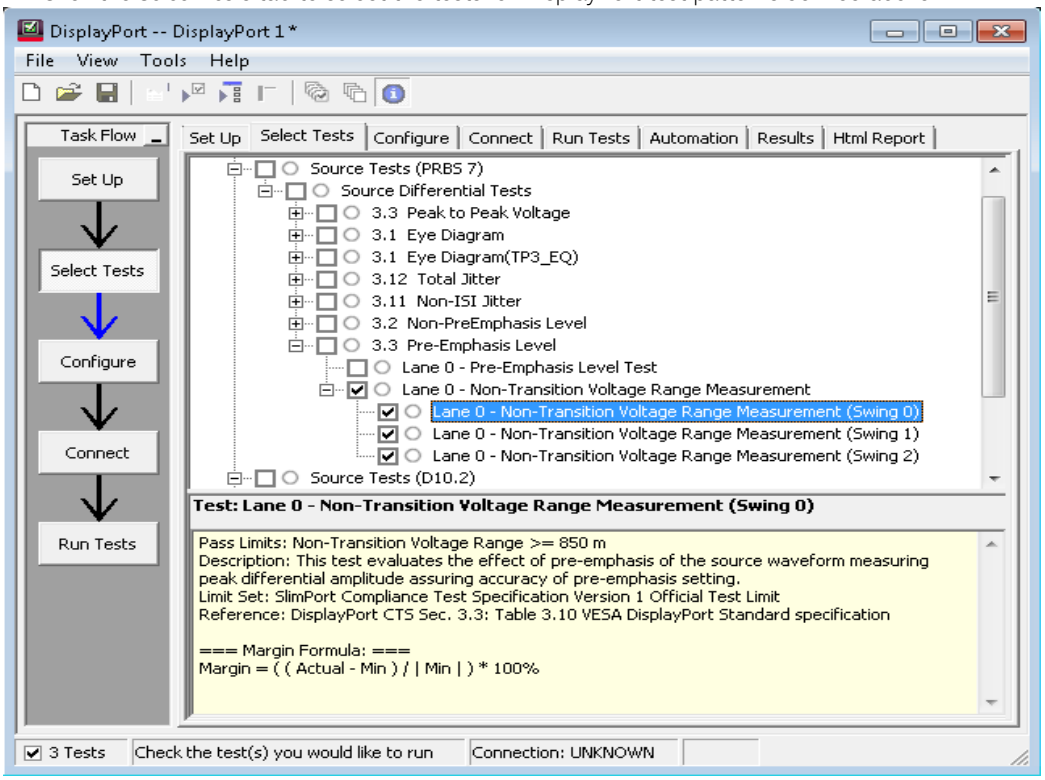


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level, repeat the following steps for all pre-emphasis levels subjected to constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard:

a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.

b Acquire and verify the input signal:

i Verify the trigger and the amplitude of the input signal.

ii Scale the vertical display of the input signal to optimum value.

iii Measure V_{TOP} and V_{BASE} of the input signal.

iv Measure the data rate of the input signal.

c Set up the parameter of the measurement:

i Enable measurement of all edges to obtain a statistical value of the measurement.

ii Set up the measurement threshold.

iii Set up the Clock Recovery as described in the section “Clock Recovery”.

d For RBR and HBR using the test pattern PRBS7:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 10111111
- V_L – 1010000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 6^{th} bit of the seven successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over two UI ending at the 50% point of the 4^{th} bit of the four successive transmitted zeros of the pattern.

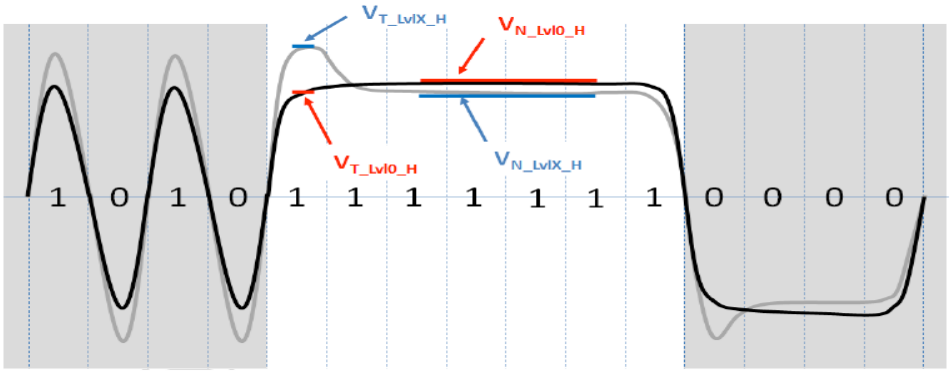


Figure 153 High Voltage measurement for RBR and HBR

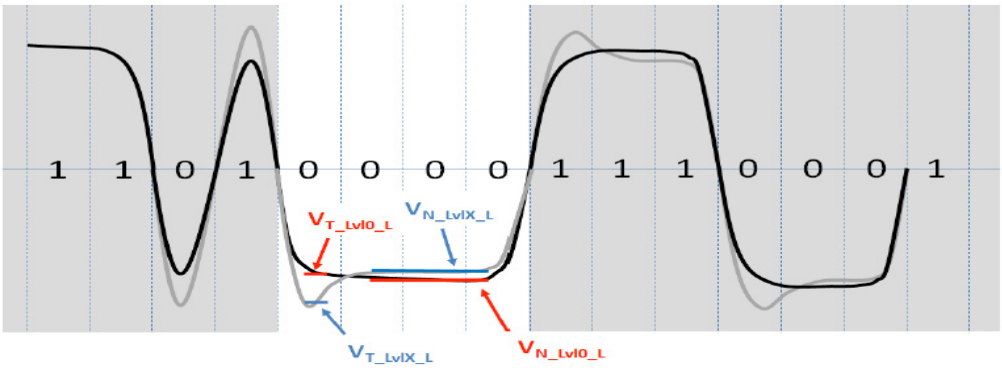


Figure 154 Low Voltage measurement for RBR and HBR

e For HBR2 and HBR25 using the test pattern PLTPAT:

i The qualifying pattern in the test pattern PRBS7 for V_H and V_L is:

- V_H – 011111
- V_L – 100000

ii For a given voltage level and pre-emphasis level (LvlX):

- The transition voltage measurement, $V_{T\_LvlX\_H}$ and $V_{T\_LvlX\_L}$ are the average values over the 40% to 70% UI points in the transition bit.
- The non-transition voltage measurement, $V_{N\_LvlX\_H}$ is the average of the High voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted ones of the pattern while $V_{N\_LvlX\_L}$ is the average of the Low voltage over three UI ending at the 50% point of the 5th bit of the five successive transmitted zeros of the pattern.

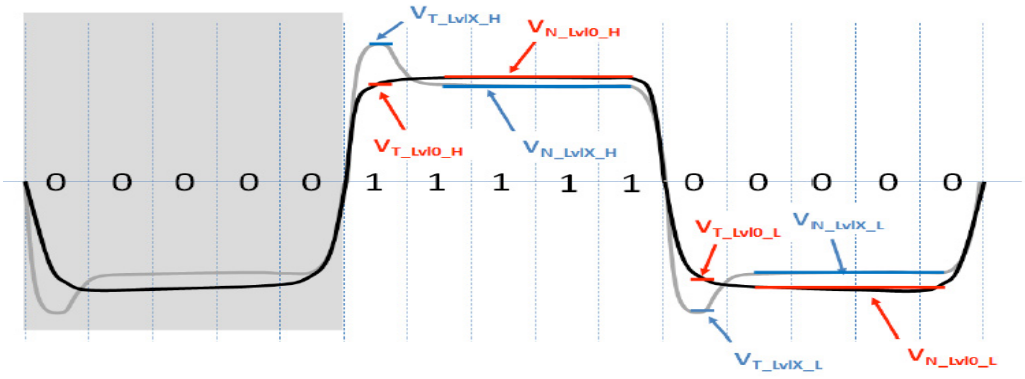


Figure 155 High Voltage and Low Voltage measurement for HBR2

f Fold the pattern of the input signal based on the qualifying pattern for V_H, as shown above.

g Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the High voltage.

h Fold the pattern of the input signal based on the qualifying pattern for V_L, as shown above.

i Set up the vertical waveform histogram on the input signal at the point specified earlier, so as to measure the transition voltage and the non-transition voltage of the Low voltage.

j Calculate the peak-to-peak value of the transition voltage using the equation:

$$V_{T\_LvlX\_PP} = V_{T\_LvlX\_H} - V_{T\_LvlX\_L}$$

k Calculate the peak-to-peak value of the non-transition voltage using the equation:

$$V_{N\_LvlX\_PP} = V_{N\_LvlX\_H} - V_{N\_LvlX\_L}$$

2 Calculate the non transition voltage range using the equation:

$$\text{Non Transition Voltage Range} = \text{Minimum } [(V_{N\_LvlX\_PP}) / (V_{N\_Lvl0\_PP})]$$

where, $V_{N\_LvlX\_PP}$) refers to all supported pre-emphasis levels (Level1, Level2, Level3 and so on up to Level X).

3 Report the measurement results.

PASS Condition

Non-Transition Voltage Range Measurements

For Level 2 voltage setting: Resultant $\geq$ 0.708 OR 20*log(Resultant) > -3dB

For Level 1 voltage setting: Resultant $\geq$ 0.708 OR 20*log(Resultant) > -3dB

For Level 0 voltage setting: Resultant $\geq$ 0.85 OR 20*log(Resultant) > -1.4dB

Table 141 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFF\_REDUCTION}$	Non-transition reduction Output Voltage Level 2	-	-	3	dB	$V_{TX\text{-}DIFF}$ at each non-zero nominal pre-emphasis level must not be lower than the specified amount less than $V_{TX\text{-}DIFF}$ at the zero nominal pre-emphasis level.
	Non-transition reduction Output Voltage Level 1	-	-	3	dB	
	Non-transition reduction Output Voltage Level 0	-	-	1.4	dB	

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured output voltage level reduction of the non transition bit for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Peak to Peak Voltage Test

Test ID

For RBR and HBR:

- 1266001 – Peak to Peak Voltage Test

For HBR2 and HBR25:

- 1266101 – Peak to Peak Voltage Test

Test Overview

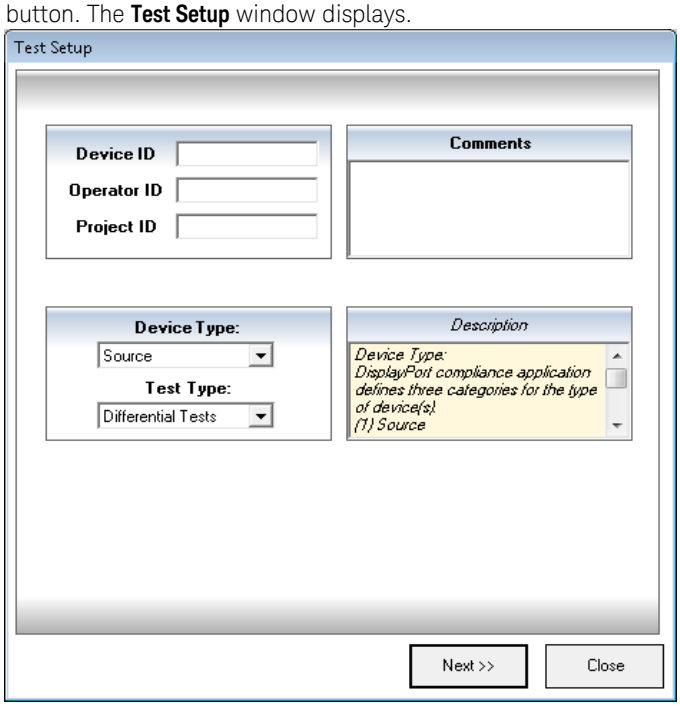
The objective of this test is to evaluate the maximum differential peak to peak voltage.

Test Conditions for Peak to Peak Voltage Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels are supported with constraints specified in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR – PRBS7 HBR2, HBR25– PLTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



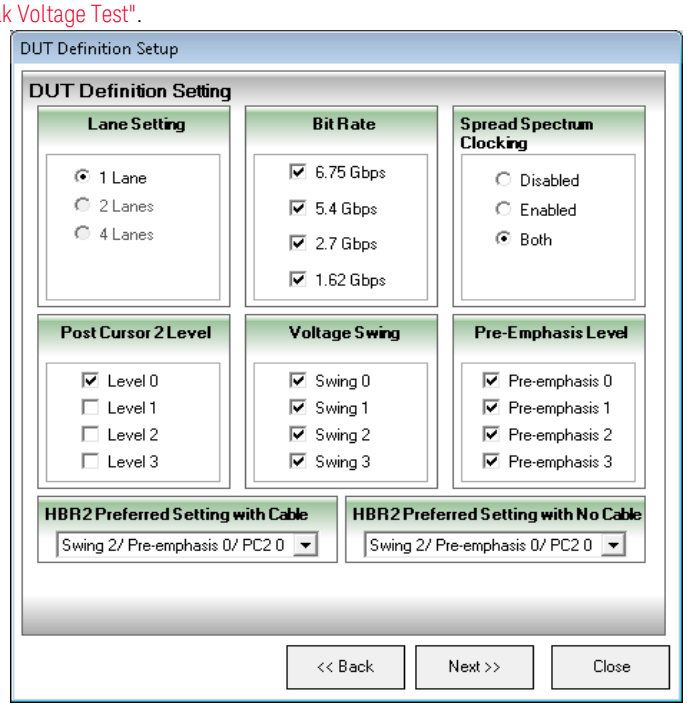
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

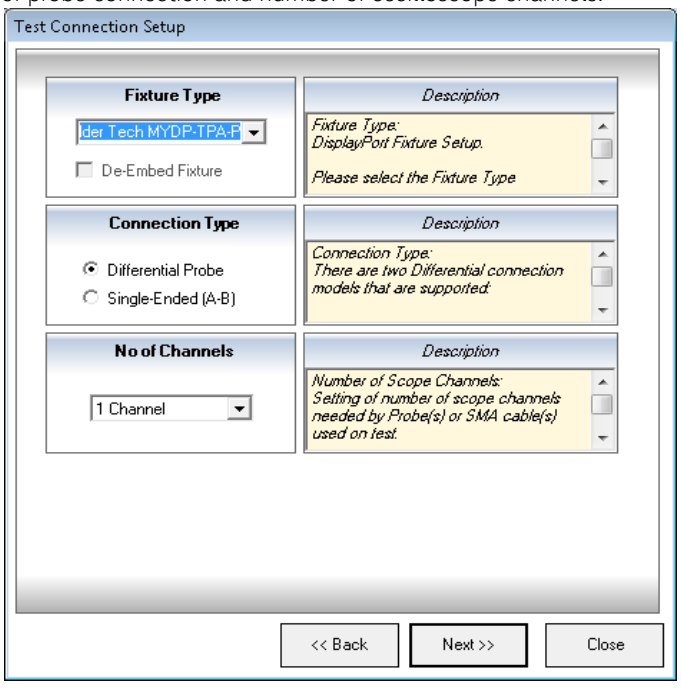
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

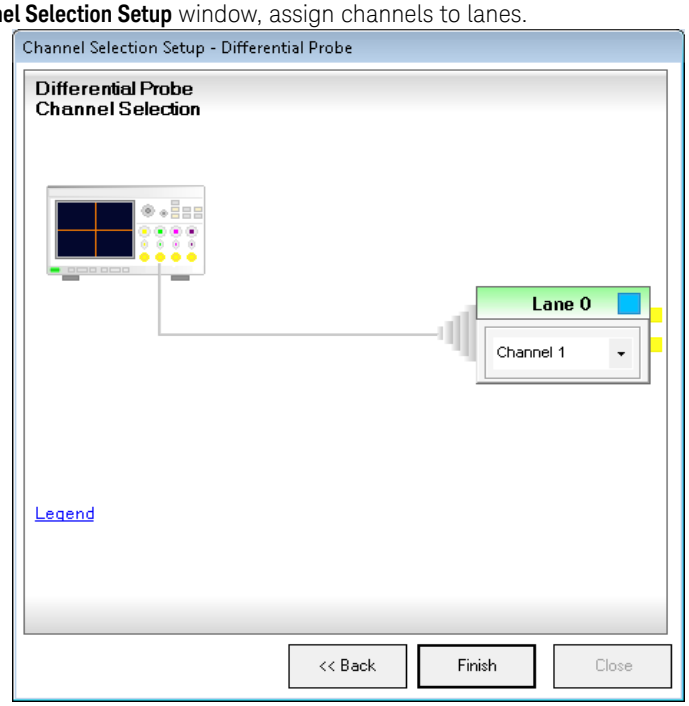
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Peak to Peak Voltage Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

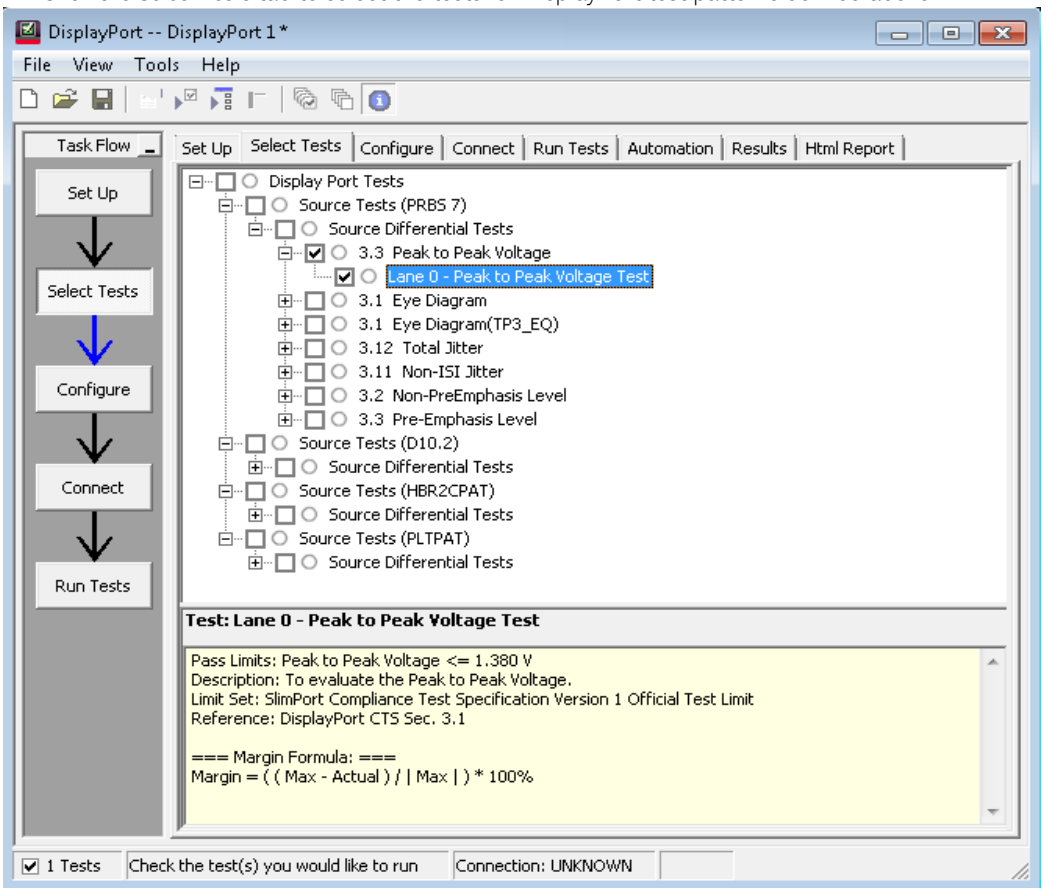


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Measure the maximum and minimum voltage of the input signal.
4 Calculate the peak to peak voltage using the equation:

$$\text{Peak to Peak Voltage} = \text{Maximum Voltage} - \text{Minimum Voltage}$$

5 Report the measurement results.

PASS Condition

For all Data Rates:

Maximum Differential Peak to Peak Voltage $\leq$ 1.38V.

Table 142 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX\text{-}DIFFp\text{-}p\_MAX}$	Max Output Voltage Level	-	-	1.38	V	For all Output Level and Pre-emphasis combinations.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured peak to peak voltage for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

Source Main Link Frequency Compliance Test

Test ID

12193001 – Main Link Frequency Compliance

Test Overview

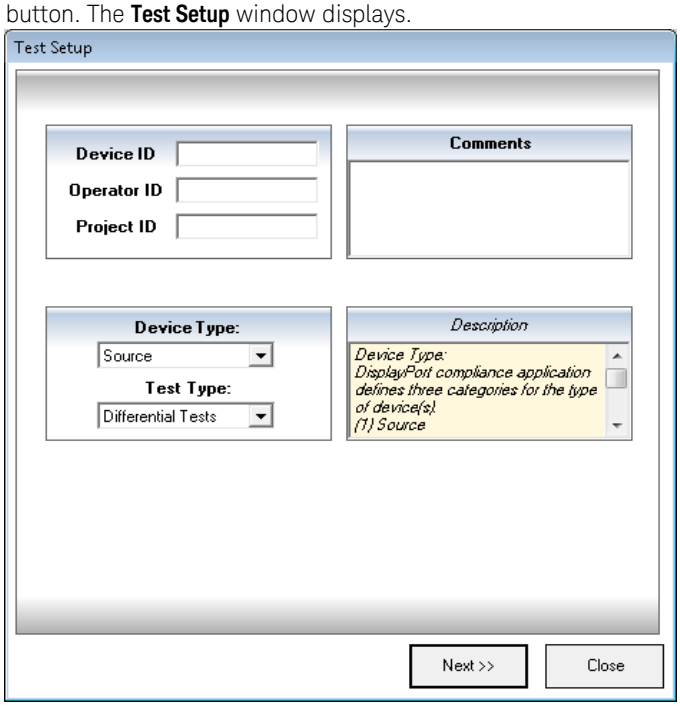
The objective of this test is to ensure that the average data rate under all conditions does not exceed the minimum and maximum values as set by the VESA DisplayPort 1.2a Standard.

Test Conditions for Main Link Frequency Compliance Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



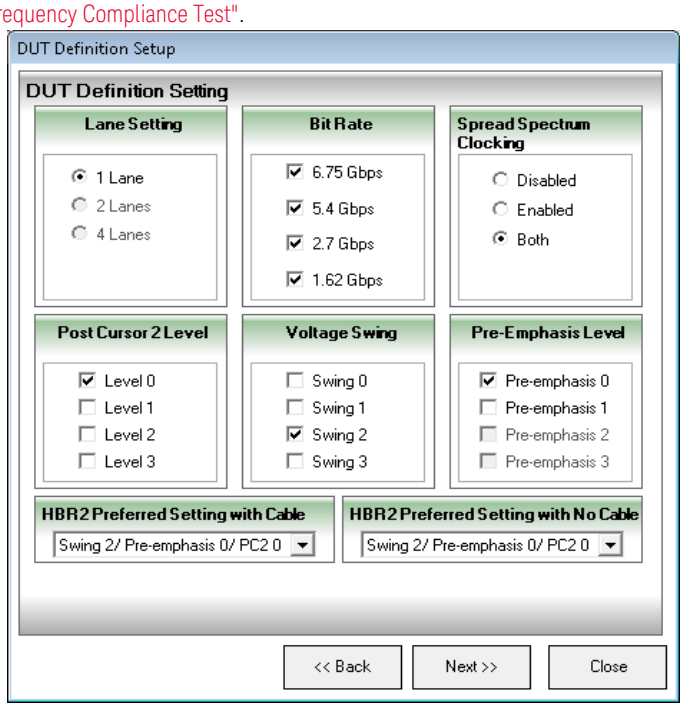
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

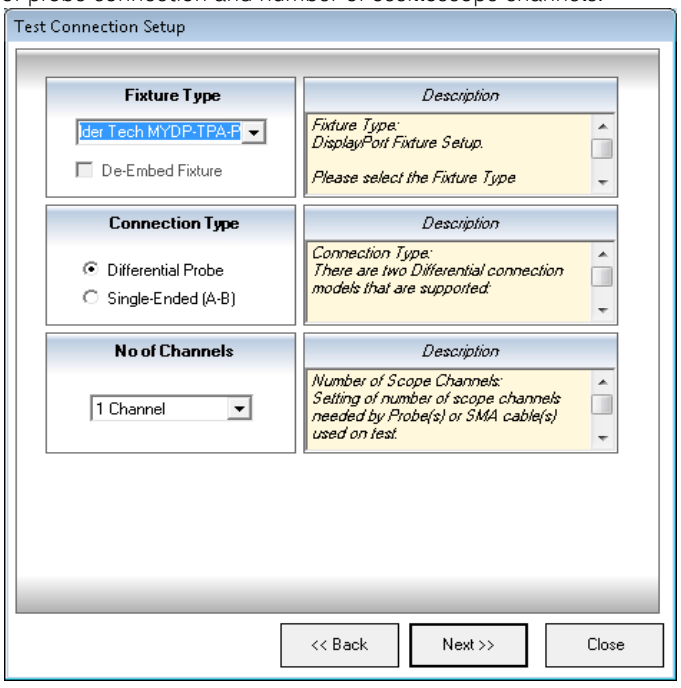
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

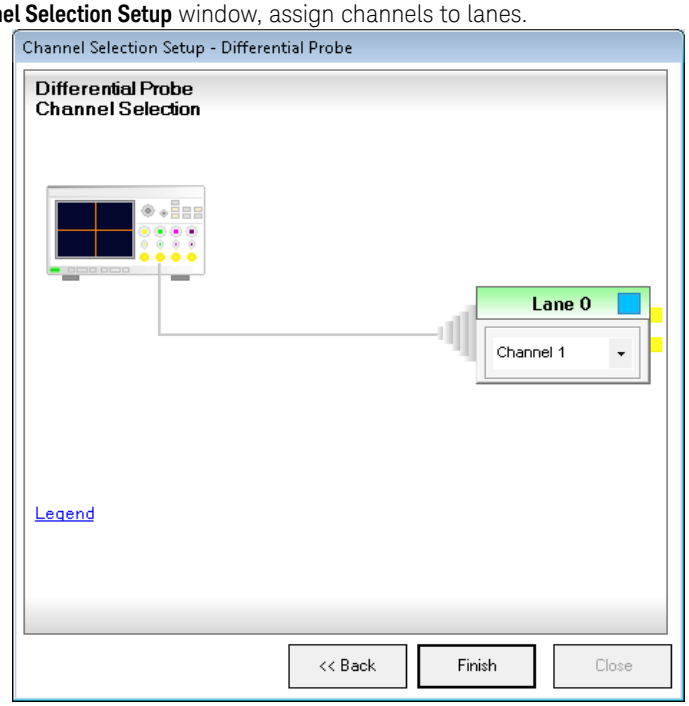
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Main Link Frequency Compliance Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

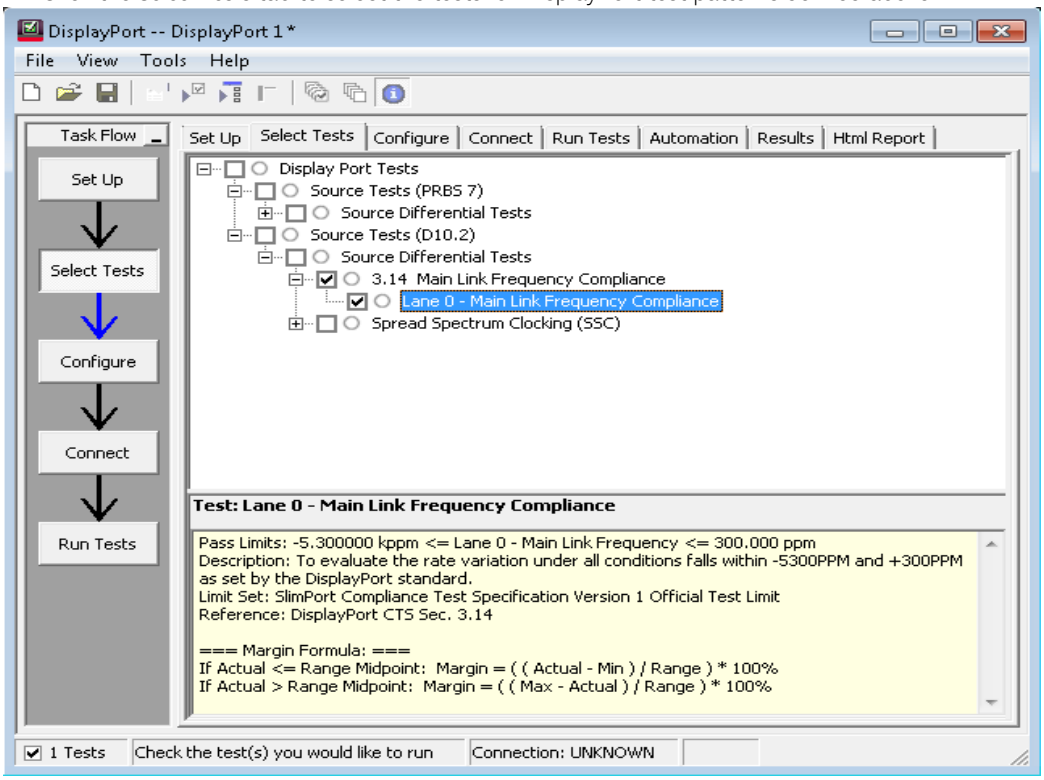


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.
5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and the minimum measurement levels for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurement levels for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e For SSC Enabled Test condition, check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.

9 For the test condition “SSC Enabled”, set up the parameter of the SSC measurement:

a Set up the memory depth and time-base to display one complete SSC cycle based on the measured SSC modulation frequency in Step 5.

b Acquire the signal with one complete SSC cycle.

c Get the minimum of FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

Maximum Data Rate = 1 / (Minimum Unit Interval)

d Get the maximum of FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

Minimum Data Rate = 1 / (Maximum Unit Interval)

e Repeat steps b, c and d until you acquire 10 SSC Cycles.

f Calculate the mean value for the maximum and minimum data rates.

10 Report the measurement results.

PASS Condition

Maximum Data Rate (Frequency Max_{ppm}) $\leq$ 300 ppm

Minimum Data Rate (Frequency Min_{ppm}) $\geq$ -5300 ppm

Table 143 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	Parameter	Min	Nom	Max	Unit	Comments
f_{HBR2}	Frequency for High Bit Rate 2	5.37138	5.4	5.40162	Gbps	Frequency high limit = +300ppm Frequency low limit = -5300ppm
f_{HBR}	Frequency for High Bit Rate	2.68569	2.7	2.70081	Gbps	
f_{RBR}	Frequency for Reduced Bit Rate	1.611414	1.62	1.620486	Gbps	

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.14*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured data rate for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Frequency Test

Test ID

12170001 – SSC Modulation Frequency Test

Test Overview

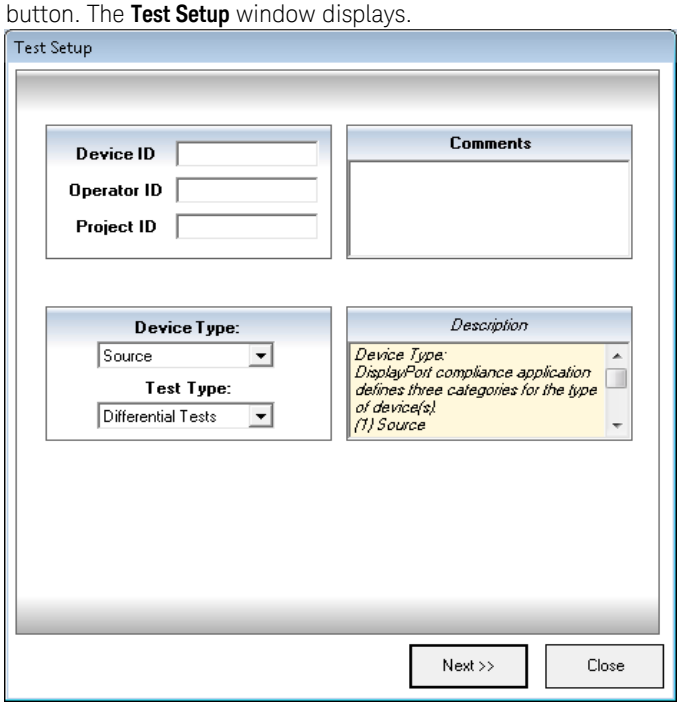
The objective of this test is to evaluate the frequency of the SSC modulation and to validate that the frequency is within specification limits. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. Calculate the SSC modulation frequency from the average of the measured SSC modulation frequency for each cycle.

Test Conditions for SSC Modulation Frequency Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR25)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



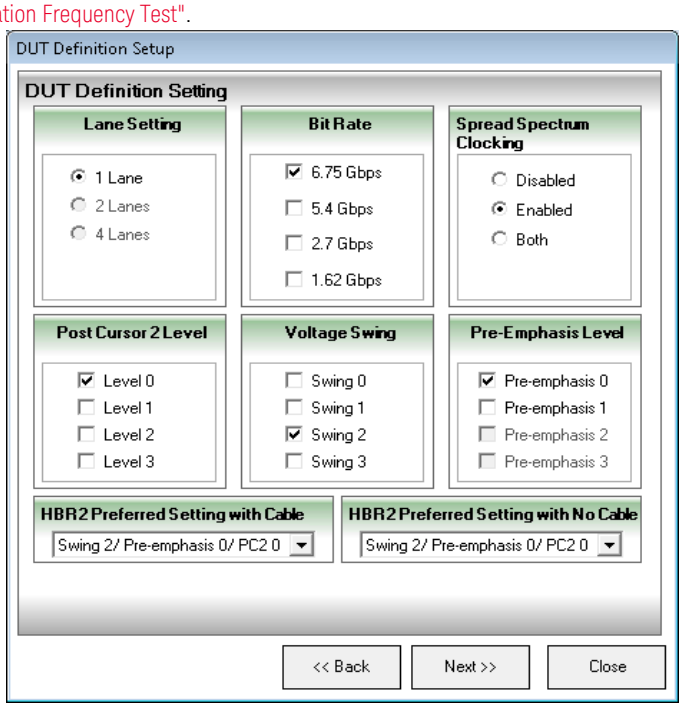
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

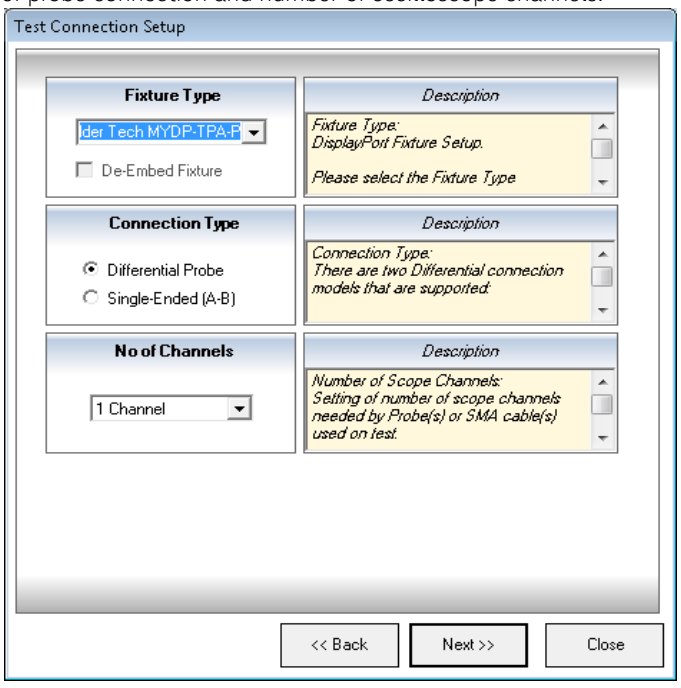
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

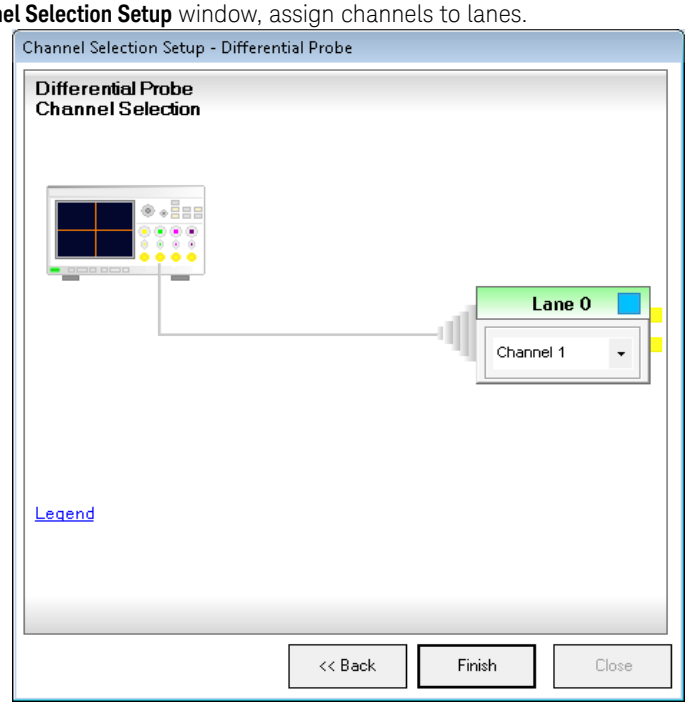
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Modulation Frequency Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

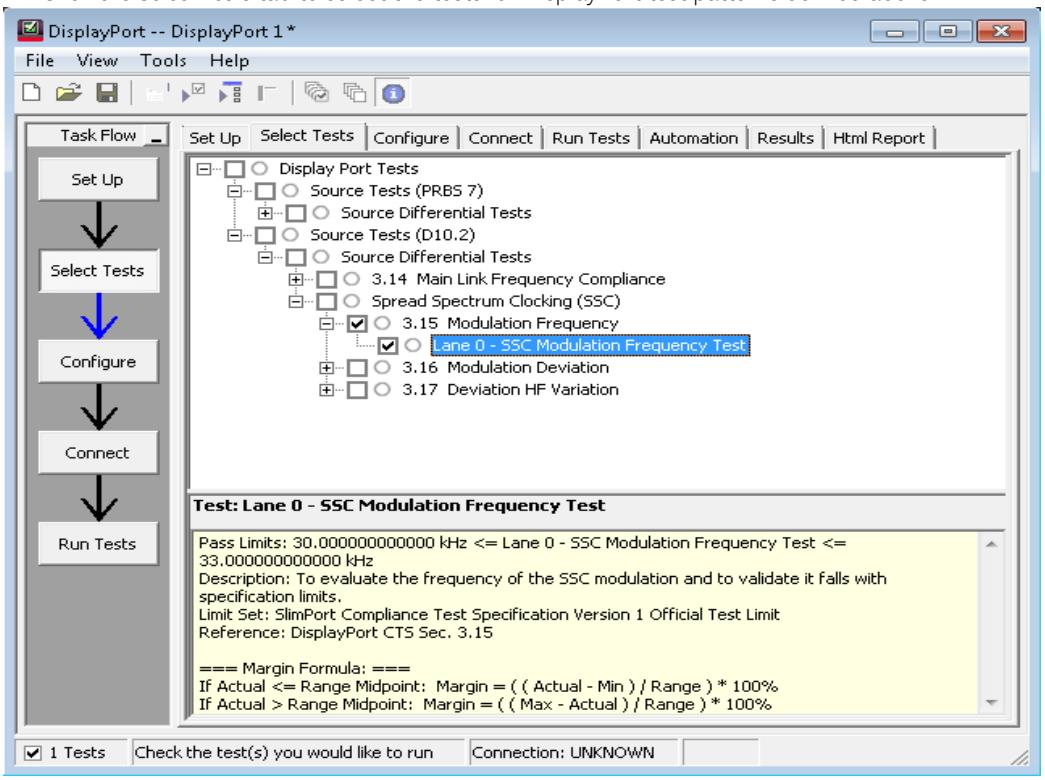


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
   g Acquire the signal for 10 SSC Cycles.
6 Get the mean value for the SSC Modulation frequency.
7 Report the measurement results.

PASS Condition

30kHz ≤ SSC Modulation Frequency (f_{SSC}) ≤ 33kHz

Table 144 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	Range: 30kHz ~ 33kHz when down-spread enabled

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.15*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation frequency for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Modulation Deviation Test

Test ID

12180001 – SSC Modulation Deviation Test

Test Overview

The objective of this test is to evaluate the range of SSC down-spreading of the transmitter signal in ppm and to validate that the values are within specification limits. This test includes the use of the 2^{nd} order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles. For each cycle, the minimum and maximum data rate is evaluated. Calculate the SSC modulation deviation from the average of the maximum minus the average of the minimum using the equation:

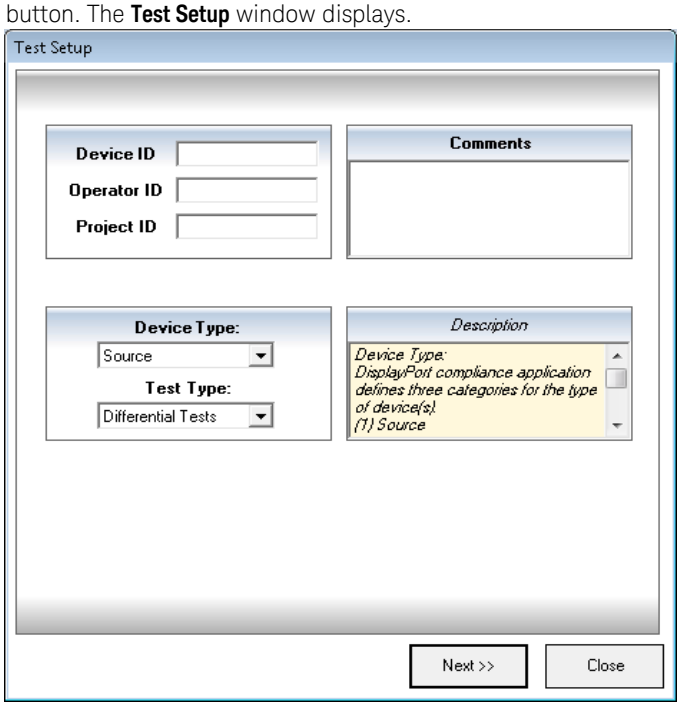
SSC Modulation Deviation = {[Average (Maximum Data Rate) - Average (Minimum Data Rate)] / Nominal Data Rate}*1e6

Test Conditions for SSC Modulation Deviation Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR25)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



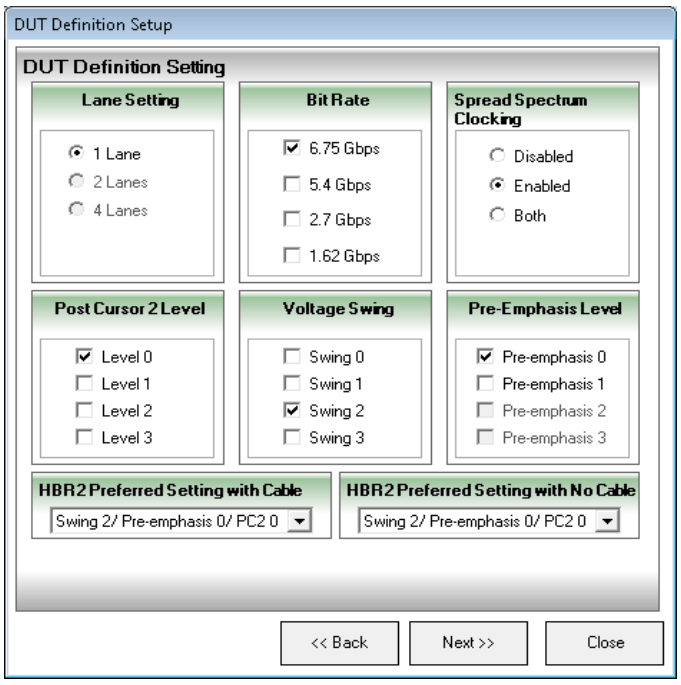
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

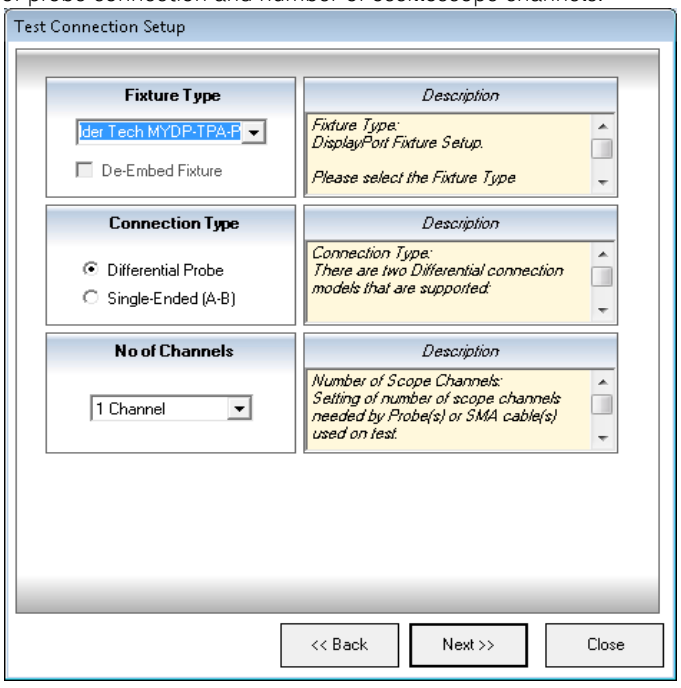
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

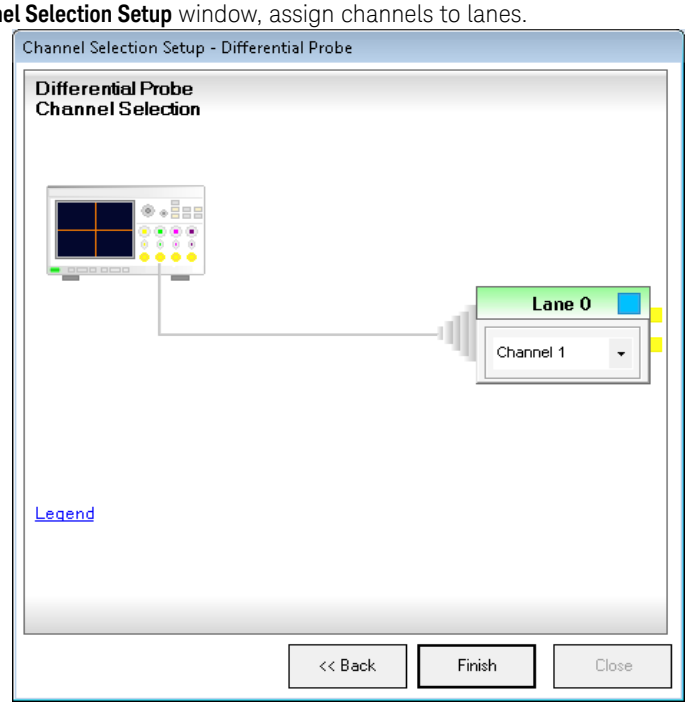
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Modulation Deviation Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

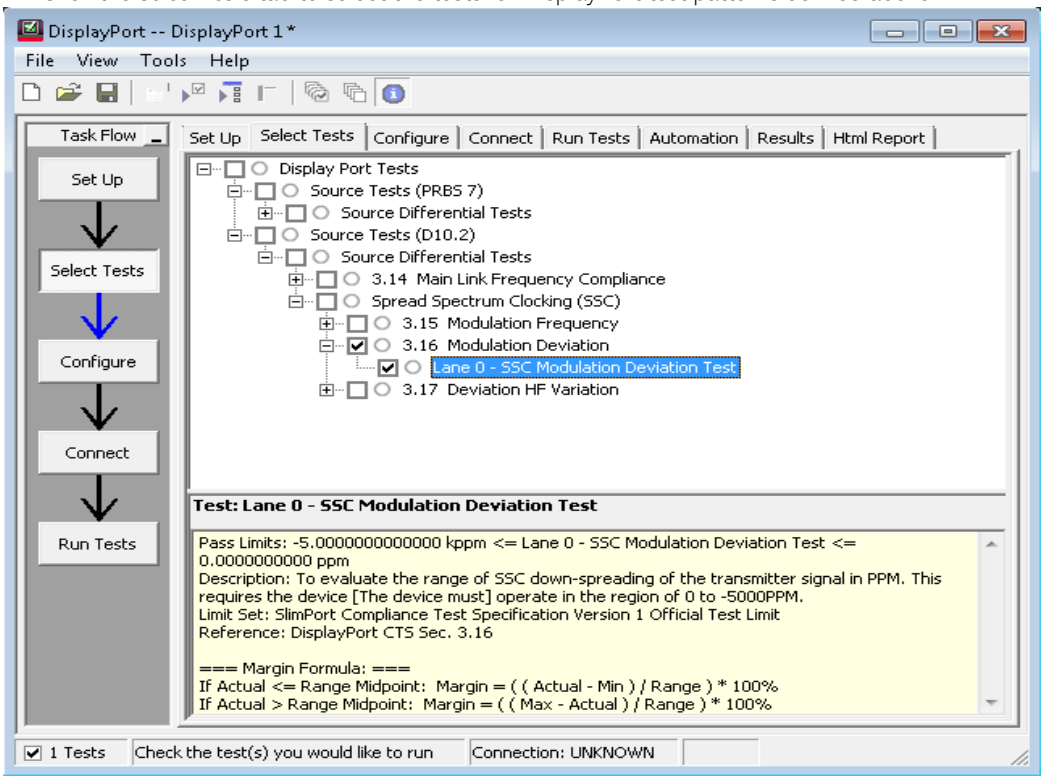


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to filter the unit interval measurement trend with 3dB corner frequency of 1.98 MHz.
5 Set up the parameters for the verification of the existence of SSC in the input signal.
   a Create FUNC2 signal, which is the magnify signal of the unit interval measurement trend.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the maximum and minimum measurements for the FUNC2 magnified unit interval measurement trend.
   d Set up two frequency measurements for the FUNC2 magnified unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   e Check the measured frequency to verify the existence of SSC in the input signal.
6 Clear all measurements.
7 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point for three points to filter the unit interval measurement trend.
8 Set up the parameters for the unit interval and data rate measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 filtered unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurements for the FUNC2 filtered unit interval measurement trend.
   e Set up the data rate or clock recovery rate (CDR rate) for the input signal.
   f Acquire the signal for 10 SSC Cycles.
   g Get the mean value for the data rate measurement.

9 Set up the parameters for SSC measurement.

a Set up memory depth and time-base to display one complete SSC Cycle based on the measured SSC modulation frequency in step 5.

b Acquire the signal with one complete SSC Cycle.

c Get the minimum of the FUNC2 filtered unit interval measurement trend to calculate the maximum data rate:

Maximum Data Rate = 1/Minimum Unit Interval

d Get the maximum of the FUNC2 filtered unit interval measurement trend to calculate the minimum data rate:

Minimum Data Rate = 1/Maximum Unit Interval

e Repeat step b,c and d until you acquire 10 SSC Cycles.

f Calculate the mean value for the maximum and minimum data rate.

10 Calculate the SSC Modulation Deviation using the equation:

SSC Modulation Deviation = (Maximum Data Rate - Minimum Data Rate) / (Nominal Data Rate) * 1E6

11 Report the measurement results.

PASS Condition

-5000ppm ≤ SSC Modulation Deviation ($Resultant_{SSC\ Range}$) ≤ 0ppm

Table 145 DisplayPort Main Link Transmitter System Parameters

Symbol	Parameter	Min	Nom	Max	Unit	Comments
Down_Spread_Amplitude	Link clock down-spreading	0	-	0.5	%	Range: 0% ~ 0.5% when down-spread enabled

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.16*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-16*

Expected/Observable Results

The measured SSC modulation deviation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Source Spread Spectrum Clocking (SSC) Deviation HF Variation Test (Informative)

Test ID

12200001 – SSC Deviation HF Variation Test (Informative)

Test Overview

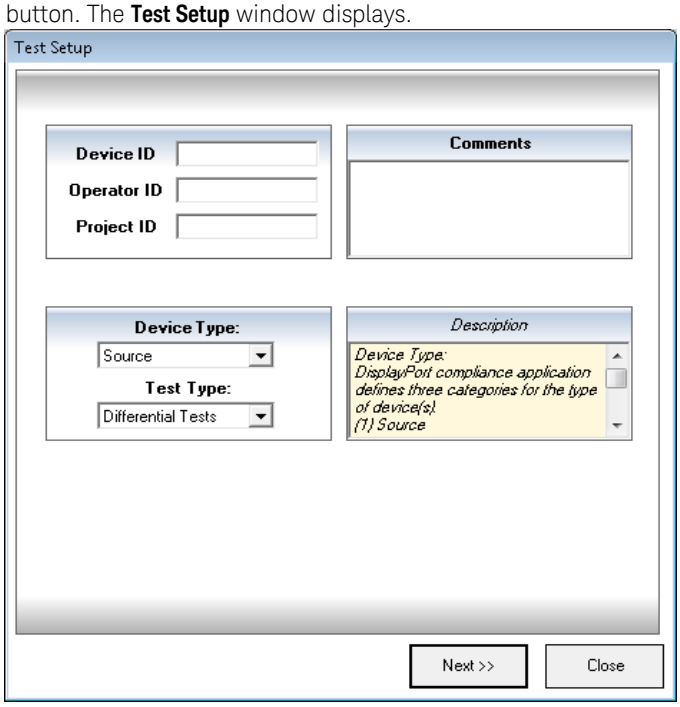
The objective of this test is to verify that the SSC profile does not include any frequency deviation that may exceed 1250 ppm/µsec. This test includes the use of the 2nd order Butterworth low-pass filter with a 3dB corner frequency of 1.98MHz. The analysis is conducted over a minimum of 10 full SSC cycles.

Test Conditions for SSC Deviation HF Variation Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR25)
SSC	SSC Enabled
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



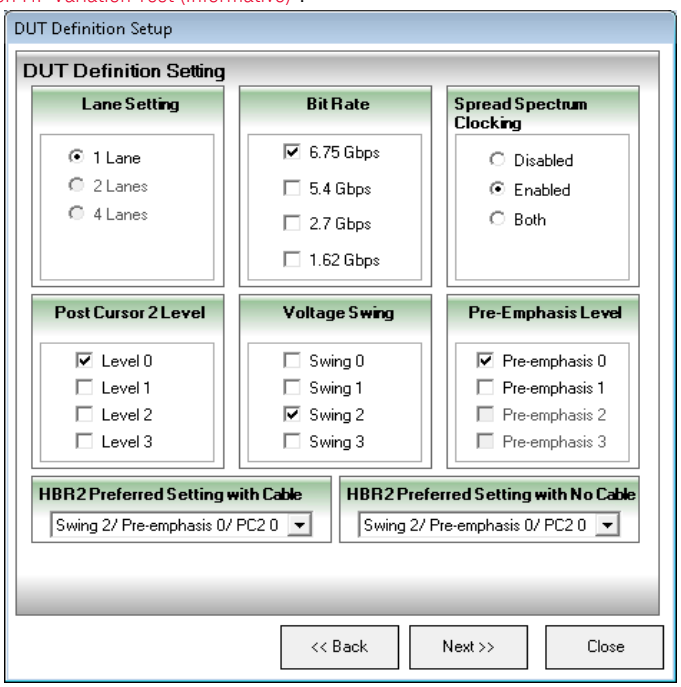
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

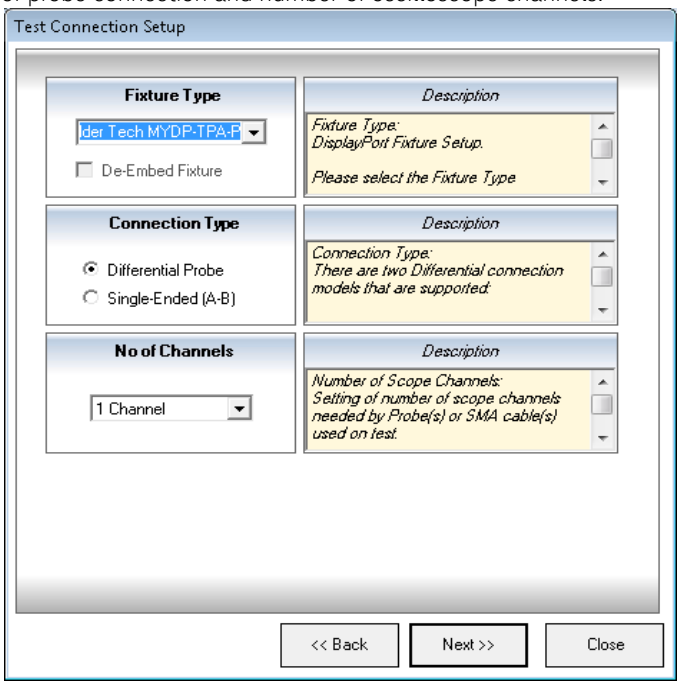
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

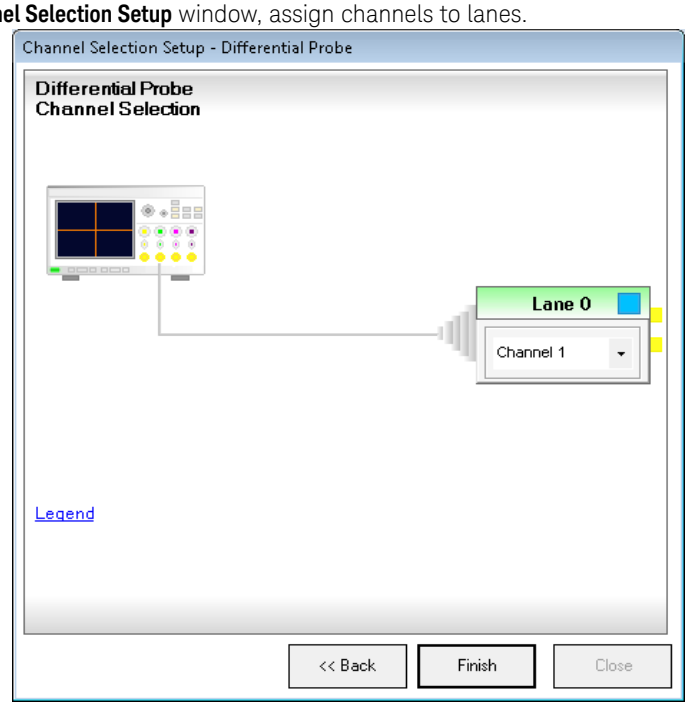
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for SSC Deviation HF Variation Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

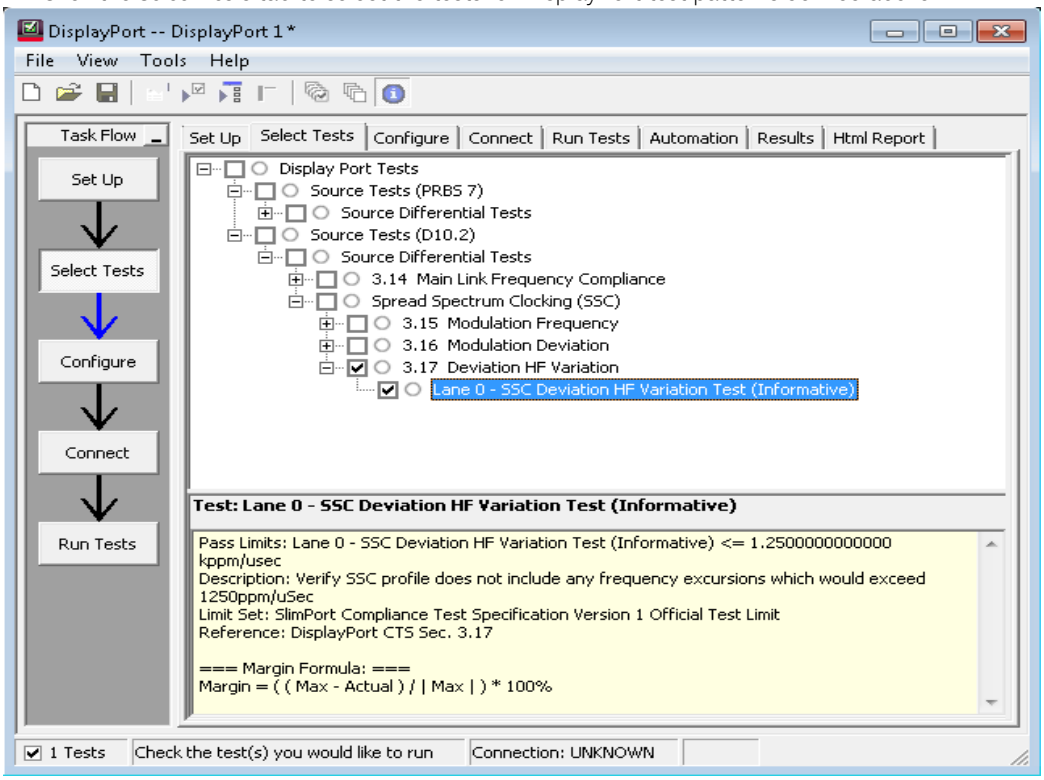


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
   d Measure the data rate of the input signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
4 Set up the parameters for the measurement of measurement trend.
   a Set up the unit interval measurement for the input signal.
   b Set up the measurement trend for the unit interval measurement.
   c Set up the smoothing point to three points to filter the unit interval measurement trend.
5 Set up the parameters for the frequency measurement.
   a Create FUNC2 signal, which is the filtered signal of the unit interval measurement trend, using a Butterworth Low Pass Filter with 3dB corner frequency of 1.98 MHz.
   b Set up two display grids such that one grid displays the input signal and the unit interval measurement trend while the other grid displays the FUNC2 magnified unit interval measurement trend.
   c Set up the memory depth and time-base using the settings defined in the Configuration Variable.
   d Set up the average, maximum and minimum measurement for the FUNC2 filtered unit interval measurement trend.
   e Set up two frequency measurements for the FUNC2 filtered unit interval measurement trend (One frequency measurement based on the rising edge while the other frequency measurement based on the falling edge).
   f Get the frequency measurement of the FUNC2 filtered unit interval measurement trend.
6 Set up the parameters for the SSC measurement.
   a Set up memory depth and time-base to display one complete SSC cycle using the measured SSC Modulation Frequency in Step 5.
   b Acquire the signal with one complete SSC Cycles.
   c Read the FUNC2 filtered unit interval measurement trend.
   d Compute the slope using the “Sliding Window” with 1.00 µsec window width. Calculate the slope using the equation:

$$\text{Slope} = [f(t) - f(t\text{-}1.00\ \mu\text{sec})/1.00\ \mu\text{sec}]$$

   e Repeat step b, c and d until you acquire 10 SSC Cycles.
   f Get the maximum value for the computed value of slope.
7 Report the measurement results.

PASS Condition

$SSC_t\ dF/dt \leq 1250 ppm/\mu sec$

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.17*

Expected/Observable Results

The measured SSC deviation high frequency variation for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Post-Cursor 2 Verification Test (Informative)

Test ID

1279001 – Post Cursor 2 Verification Test - Level 1/Level 0 (Informative)

1279101 – Post Cursor 2 Verification Test - Level 2/Level 1 (Informative)

1279201 – Post Cursor 2 Verification Test - Level 3/Level 2 (Informative)

Test Overview

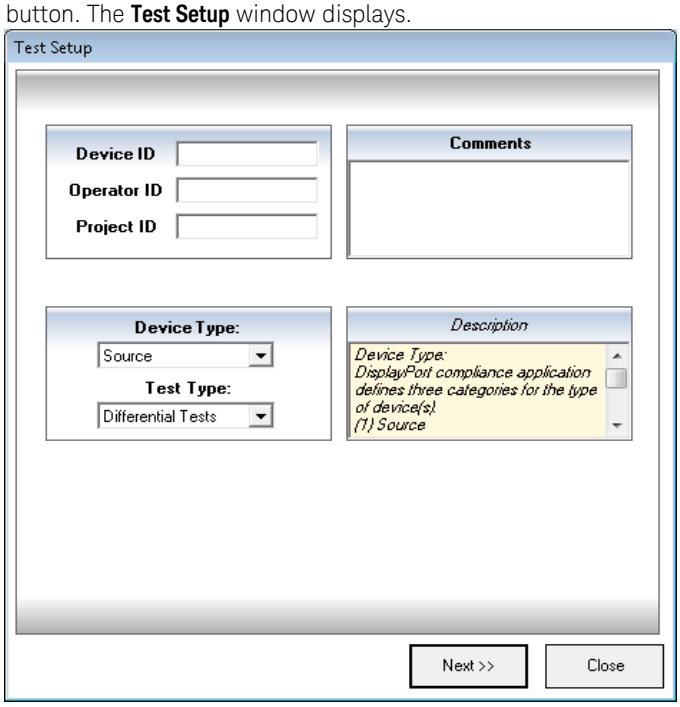
The objective of this test is to evaluate the effect of adding Post-Cursor 2 of the source waveform by measuring the peak differential amplitude to assure accuracy of the Post-Cursor 2 settings.

Test Conditions for Post-Cursor 2 Verification Test

Test Parameter	Condition
Test Point	TP2
Bit Rate	HBR2, HBR25
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage levels supported
Pre-Emphasis Level	All pre-emphasis levels supported subject to constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard.
Post-Cursor2 Level	All Post-Cursor 2 levels supported
Test Lane	Lane 0
Test Pattern	PCTPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



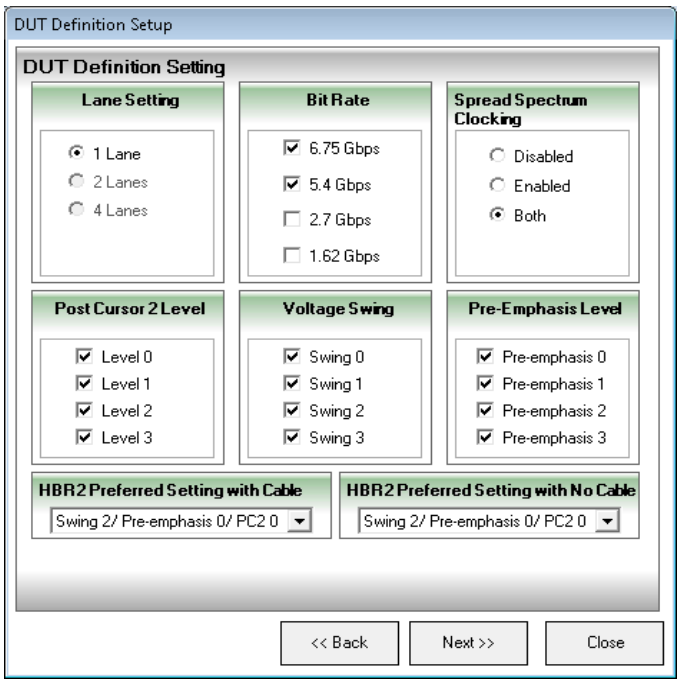
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

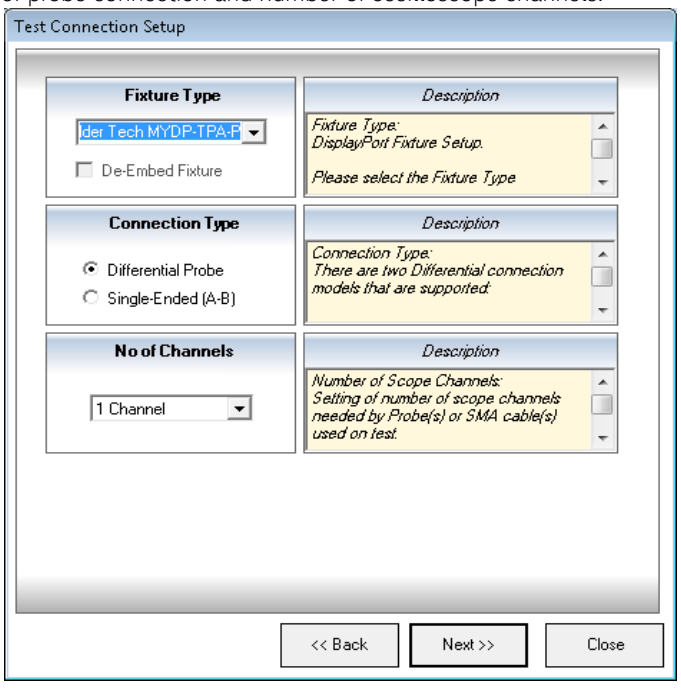
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

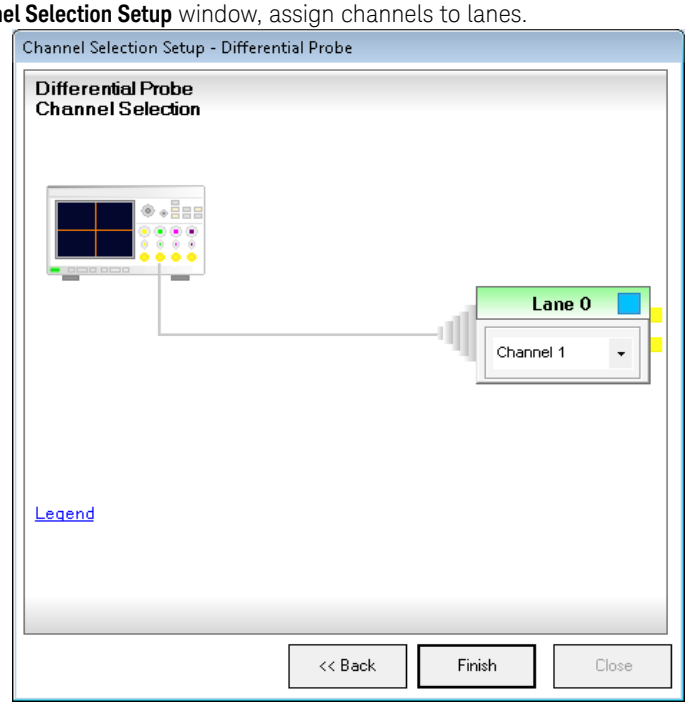
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Post-Cursor 2 Verification Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

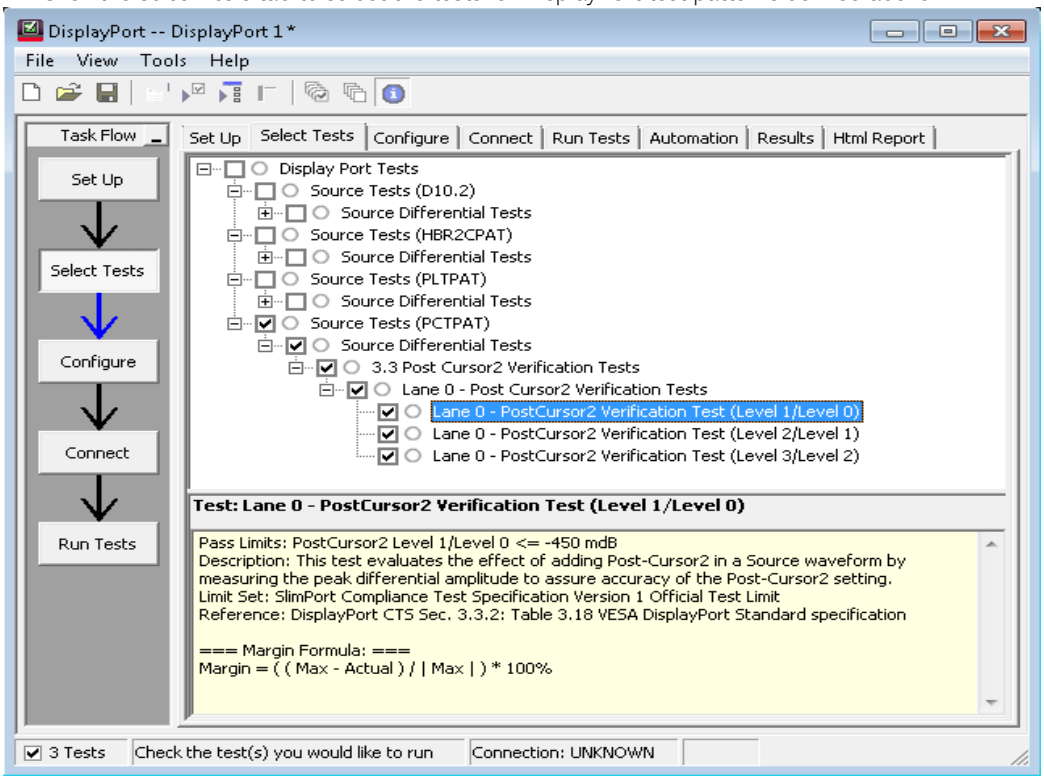


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 For a given Voltage Level, Pre-Emphasis Level and Post-Cursor 2 Level X:
   a Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   b Acquire and verify the input signal:
      i Verify the trigger and the amplitude of the input signal.
      ii Scale the vertical display of the input signal to optimum value.
      iii Measure V_{TOP} and V_{BASE} of the input signal.
      iv Measure the data rate of the input signal.
   c Set up the parameter of the measurement:
      i Enable measurement of all edges to obtain a statistical value of the measurement.
      ii Set up the measurement threshold.
      iii Set up the Clock Recovery as described in the section “Clock Recovery”.
   d Pattern fold the input signal based on the qualifying pattern 00101010 for the measurement of voltage $V_{T1010\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.
   e Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1010\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1010\_PC2\_LvlX\_L}$.
      i $V_{T1010\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1010 portion of the qualifying pattern.
      ii $V_{T1010\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1010 portion of the qualifying pattern.
   f Calculate the peak-to-peak voltage $V_{T1010\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1010\_PC2\_LvlX\_PP} = V_{T1010\_PC2\_LvlX\_H} - V_{T1010\_PC2\_LvlX\_L}$$

   g Pattern fold the input signal based on the qualifying pattern 00011001100 for the measurement of voltage $V_{T1100\_PC2\_LvlX\_PP}$ in the test pattern PLTPAT.
   h Set up the vertical waveform histogram on the input signal at the points specified below to measure the High voltage $V_{T1100\_PC2\_LvlX\_H}$ and Low Voltage $V_{T1100\_PC2\_LvlX\_L}$.
      i $V_{T1100\_PC2\_LvlX\_H}$ is the average value over the 40% to 70% UI points in the fifth relevant bit (1s bit) in the 1100 portion of the qualifying pattern.
      ii $V_{T1100\_PC2\_LvlX\_L}$ is the average value over the 40% to 70% UI points in the sixth relevant bit (0s bit) in the 1100 portion of the qualifying pattern.
   i Calculate the peak-to-peak voltage $V_{T1100\_PC2\_LvlX\_PP}$ using the equation:

$$V_{T1100\_PC2\_LvlX\_PP} = V_{T1100\_PC2\_LvlX\_H} - V_{T1100\_PC2\_LvlX\_L}$$

   j Calculate the Post-Cursor 2 ratio using the equation:

$$\text{Post-Cursor 2 Ratio}_{LvlX} = V_{T1100\_PC2\_LvlX\_PP} / V_{T1010\_PC2\_LvlX\_PP}$$

2 Compare the pre-emphasis delta of Post-Cursor 2 Level with the limits by repeating Step 1 with another Post-Cursor2 Level.
3 Calculate the pre-emphasis delta of Post-Cursor 2 Level using the equation:

$$\text{Post-Cursor 2 Delta (Level 1 vs Level 0)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl1} / \text{Post-Cursor 2 Ratio}_{Lvl0}]$$

$$\text{Post-Cursor 2 Delta (Level 2 vs Level 1)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl2} / \text{Post-Cursor 2 Ratio}_{Lvl1}]$$

$$\text{Post-Cursor 2 Delta (Level 3 vs Level 2)} = 20 * \text{Log}_{10}[\text{Post-Cursor 2 Ratio}_{Lvl3} / \text{Post-Cursor 2 Ratio}_{Lvl2}]$$

4 Report the measurement results.

PASS Condition

Post Cursor2 Verification Measurements:

For Level 1 vs. Level 0 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl0\_to\_Lvl1} < -0.45$ dB

For Level 2 vs. Level 1 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl1\_to\_Lvl2} < -0.5$ dB

For Level 3 vs. Level 2 Pre-emphasis Post Cursor 2 settings: $Resultant_{Lvl2\_to\_Lvl3} < -0.6$ dB

Table 146 DisplayPort Main Link Transmitter TP2 Parameters

TP2 (TX External Connector - Normative)						
Symbol	**Parameter**	**Min**	**Nom**	**Max**	**Unit**	**Comments**
$V_{TX-PREEMP\_POST2-DELTA}$	Delta of Pre-emphasis Post Cursor2 Level 1 vs. Level 0	-0.45	-	-	dB	Measured on 2nd TBIT at Pre-emphasis Level 0
	Delta of Pre-emphasis Post Cursor2 Level 2 vs. Level 1	-0.5	-	-	dB	Support for Pre-emphasis Post Cursor2 is optional
	Delta of Pre-emphasis Post Cursor2 Level 3 vs. Level 2	-0.6	-	-	dB	

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2a, Section 3.3.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured pre-emphasis delta of Post-Cursor 2 for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Eye Diagram Test (TP3_EQ)

Test ID

For HBR

- 1211001 – Eye Diagram Test (TP3_EQ)
- 1211011 – Eye Diagram Test with No Cable Model (TP3_EQ)

For HBR2 and HBR25

- 1215001 – Eye Diagram Test (TP3_EQ)
- 1215011 – Eye Diagram Test with No Cable Model (TP3_EQ)

Test Overview

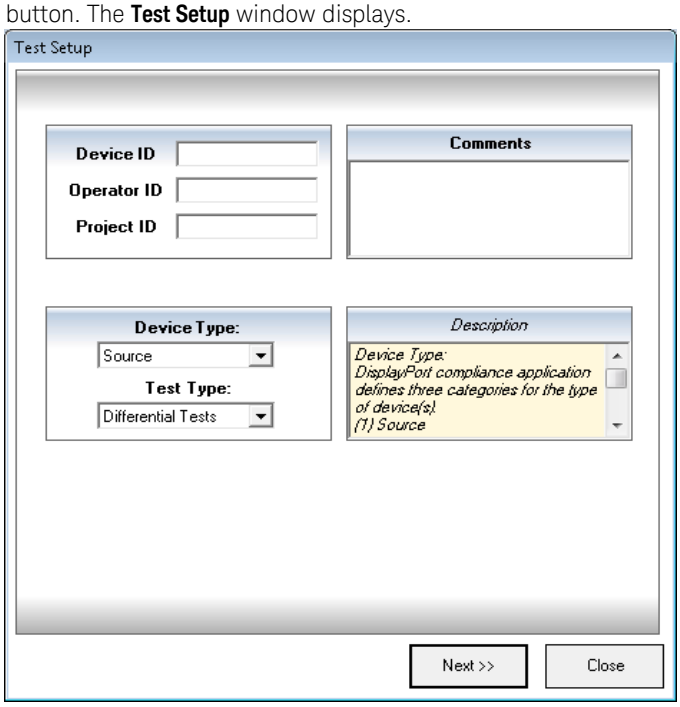
The objective of this test is to evaluate the waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions for Eye Diagram Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR (Informative), HBR2 and HBR25
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	HBR – Level 2 HBR2, HBR25 – Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	HBR – Level 0 HBR2, HBR25 – Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	HBR – Level 0 HBR2, HBR25 – Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR–PRBS7 HBR2, HBR25–HBR2CPAT
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



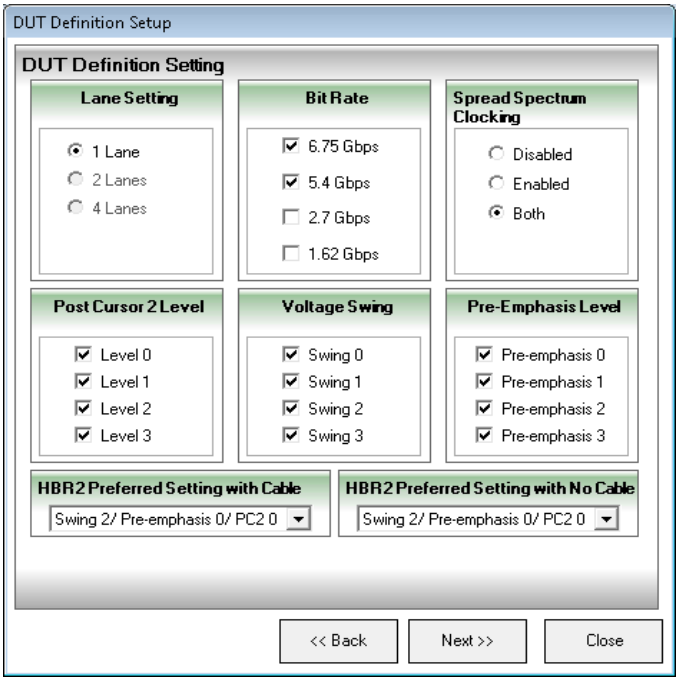
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

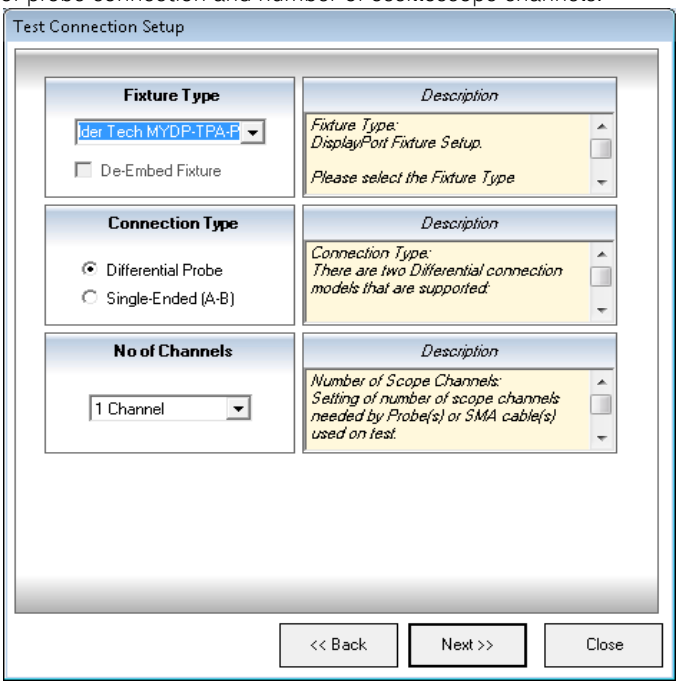
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

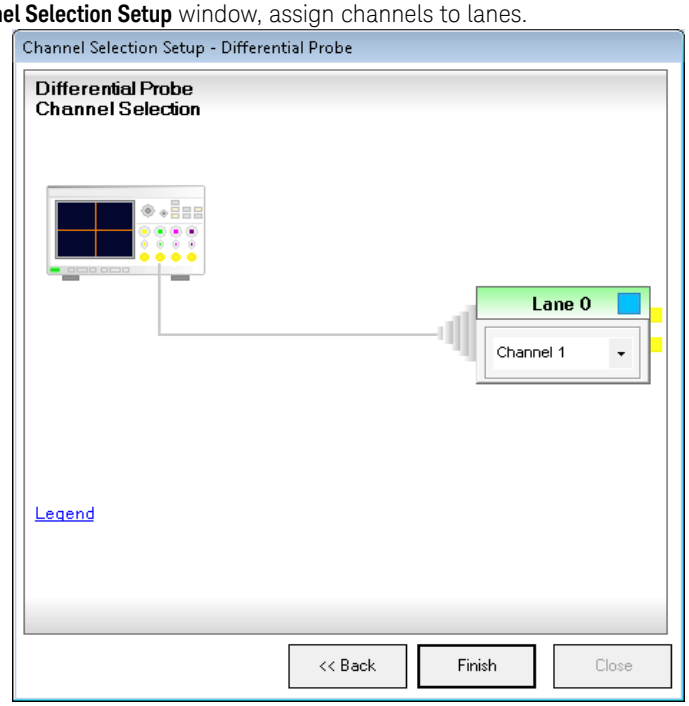
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

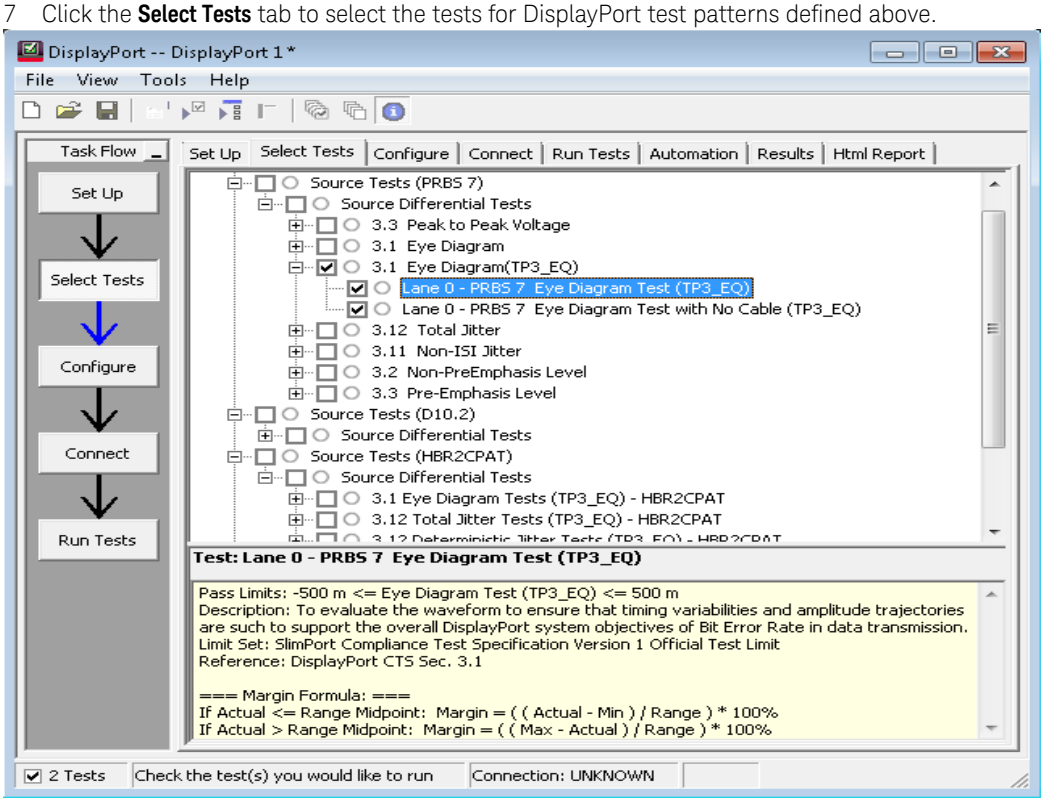


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure for HBR and HBR25

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
6 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
7 Set up the parameters for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
8 Measure the jitter of the eye diagram using the Histogram.
9 Check for any signal trajectories that may have entered into the mask.
10 Report the measurement results.

Measurement Procedure for HBR2

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.

4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Pattern fold the equalized signal based on the High Level Voltage (V_{HIGH}) random noise configuration variable.
   b Set up the vertical waveform histogram on the equalized signal to measure random noise of High Level Voltage (V_{HIGH}).
   c Measure the High Level Voltage (V_{HIGH}) random noise based on the standard deviation of the waveform histogram.
   d Pattern fold the equalized signal based on the Low Level Voltage (V_{LOW}) random noise configuration variable.
   e Set up the vertical waveform histogram on the equalized signal to measure the random noise of Low Level Voltage (V_{LOW}).
   f Measure the Low Level Voltage (V_{LOW}) random noise based on the standard deviation of the waveform histogram.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge and right edge.
8 Set up the vertical waveform histogram on the equalized signal eye diagram to measure the eye height from 0.375 UI to 0.625 UI.
9 Find the maximum eye height location of the eye diagram.
10 If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]:
   a Set up the parameter of the jitter separation using the EZJIT Plus/Complete Software.
      i Load the jitter separation parameter into EZJIT Plus/Complete Software based on the settings in the Configuration Variable.
      ii Acquire the signal until 1,000,000 edges are analyzed.
   b Note the value of the jitter component from the EZJIT Plus/Complete Software.
11 Create the eye mask based on the following criteria:
   a If random noise/ jitter derate includes [“Exclude Random Noise” configuration variable set to “False” (Default)]: eye mask height and width is derate as below to comprehend the noise/jitter extrapolated to BER 10^{-9} for an Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI:
      i Calculate the Eye Mask Width Derate (Random Jitter) using the equation:

$$\text{Eye Mask Width Derate (Random Jitter)} = 2.5 * \text{Random Jitter}_{rms}$$

      ii Calculate the Eye Mask Height Derate (Random Noise) using the equation:

$$V_{HIGH}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{HIGH}\ \text{Random Noise}_{rms}$$

$$V_{LOW}\ \text{Eye Mask Height Derate (Random Noise)} = 2.5 * V_{LOW}\ \text{Random Noise}_{rms}$$

NOTE The factor 2.5 is the delta between BER 10^{-6} (9.507) and 10^{-9} (11.996) to comprehend the noise/jitter extrapolated to BER 10-9 as the Eye Diagram Test (TP3_EQ) only acquiring 1e6 UI.

BER	N
10^{-6}	9.507
10^{-7}	10.399
10^{-8}	11.224
10^{-9}	11.996

b Place the eye mask height at the point of the maximum eye height found in Step 9.

c Calculate the Eye Mask Width:

Eye Mask Width = Eye Width Specification (0.38 UI) + Eye Mask Width Derate (Crosstalk) + 2 * Eye Mask Width Derate (Random Jitter)

d Calculate the Eye Mask Height:

Eye Mask Height = {Eye Height Specification (0.09 UI) + Eye Mask Height Derate (Crosstalk)}/2 + V_{HIGH} Eye Mask Height Derate (Random Noise)

Eye Mask Height = -{Eye Height Specification (0.09 UI) + Eye Mask Height Derate (Crosstalk)}/2 - V_{LOW} Eye Mask Height Derate (Random Noise)

12 Set up the parameters for the Mask Test.

a Load the eye mask based on the settings in the Configuration Variable.

b Center the eye mask at the middle of the eye diagram.

c Run the eye mask until 1,000,000 UI are folded.

13 Measure the eye height of the eye diagram using the Histogram.

14 Measure the jitter of the eye diagram using the Histogram.

15 Calculate the eye width based on the measured jitter of the eye diagram.

16 Check for any signal trajectories that may have entered into the mask.

17 Report the measurement results.

PASS Condition

The following table and figures define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 147 shows the voltage and time coordinates for the mask used for the eye diagram.

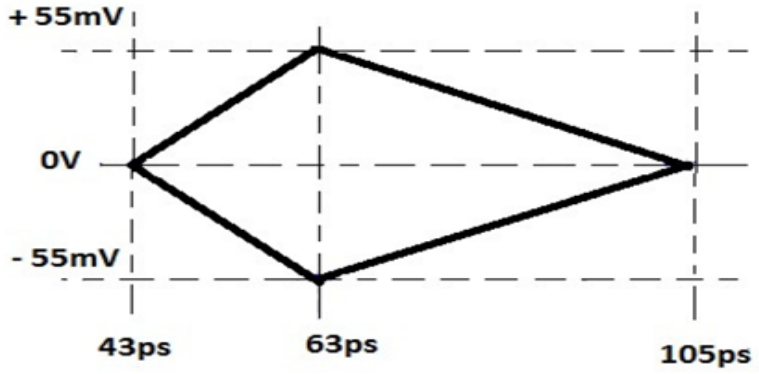


Figure 156 Eye Mask at TP3_EQ (HBR25)

Table 147 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	High (2.7 Gb/s)
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

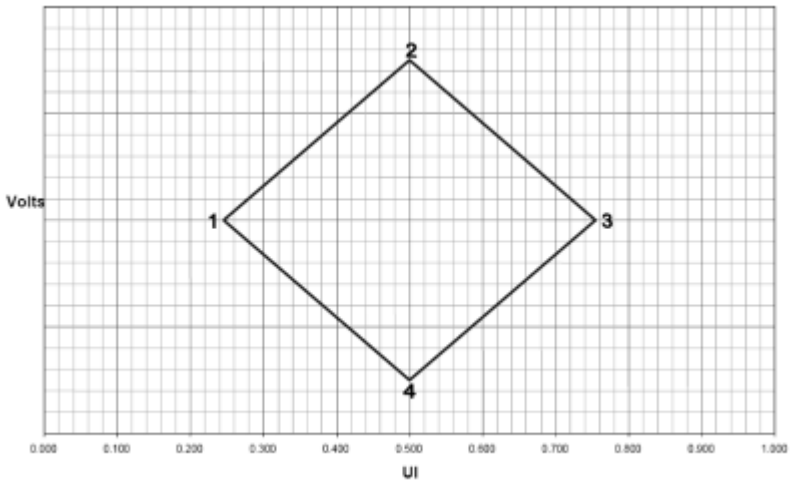


Figure 157 Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 148 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045

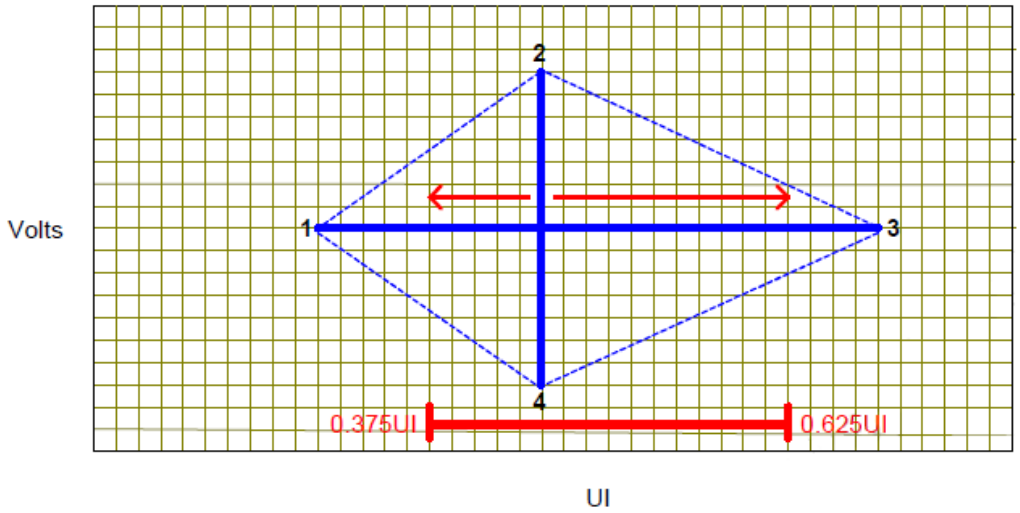


Figure 158 Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Total Jitter Test (TP3_EQ)

Test ID

For HBR2 and HBR25

- 1222001 – Total Jitter Test (TP3_EQ) - HBR2CPAT
- 1222011 – Total Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1221001 – Total Jitter Test (TP3_EQ) - D10.2
- 1221011 – Total Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

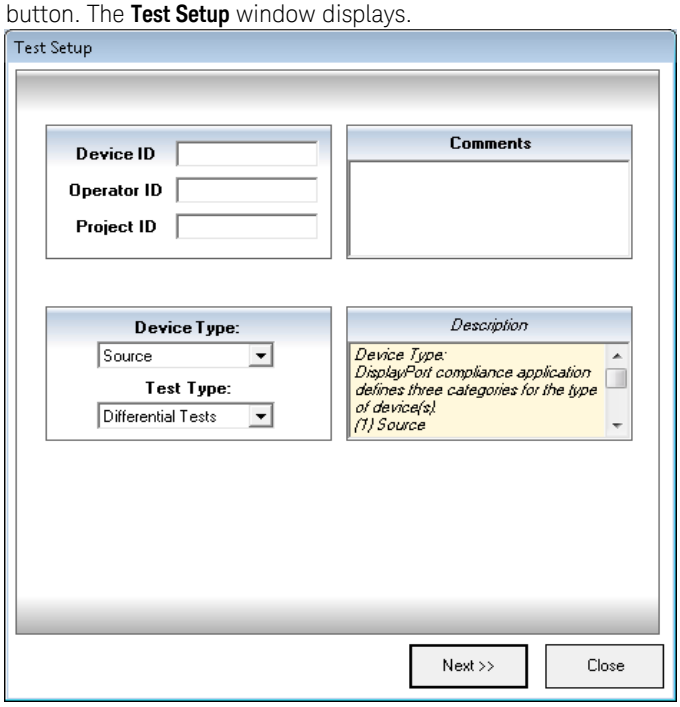
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2, HBR25
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



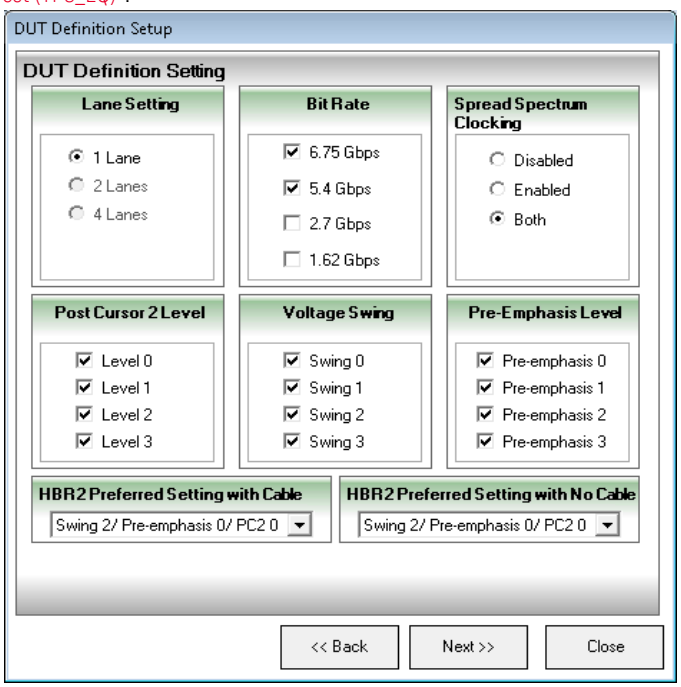
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

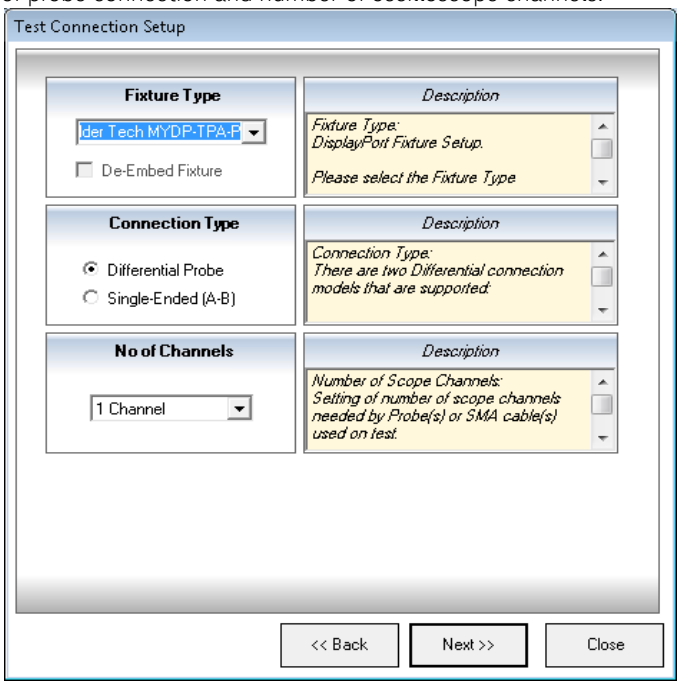
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

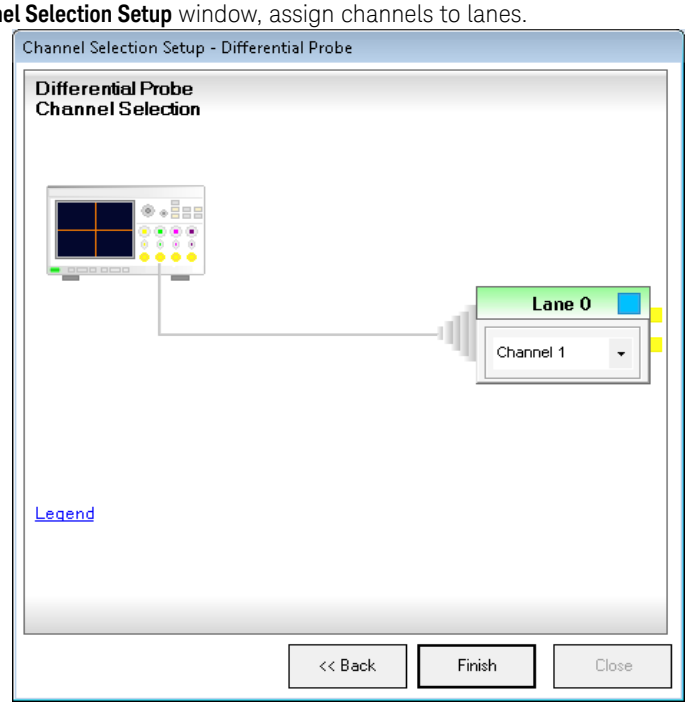
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

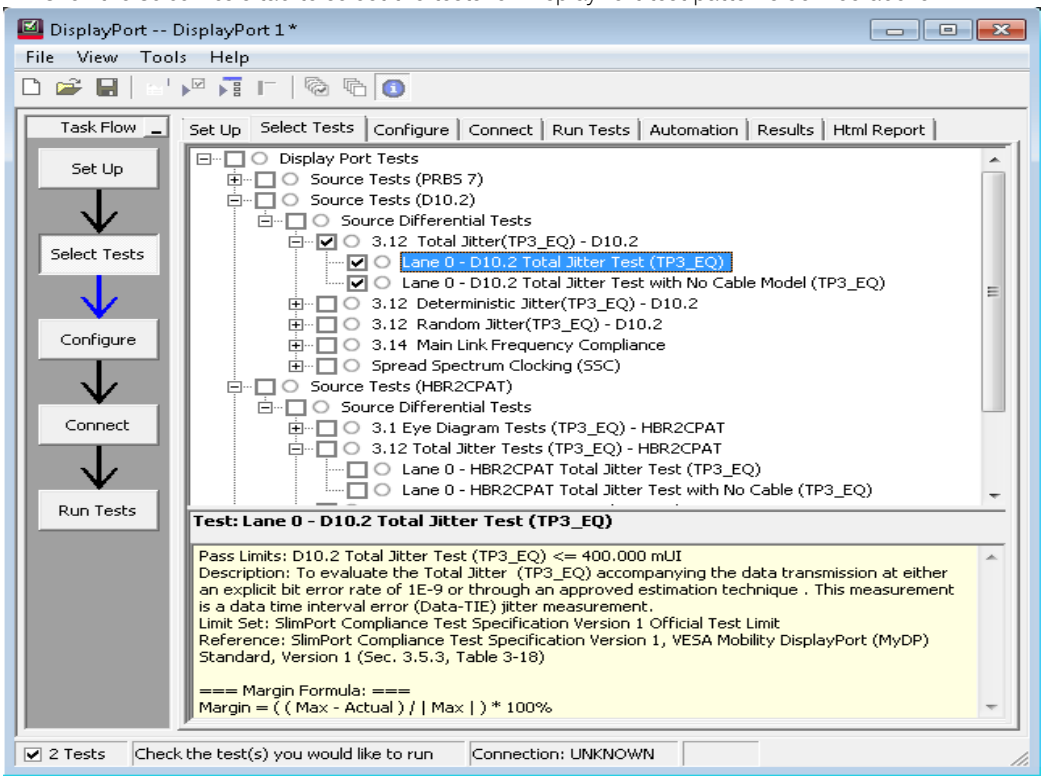


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 149 Total Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) and High-Bit Rate 25 (6.75 Gb/s per lane)	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI limit in DisplayPort 1.2a Standard.

Table 150 Total Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) and High-Bit Rate 25 (6.75 Gb/s per lane)	
$T_{TX-TJ\_D10.2\_HBR2}$	0.40 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured total jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Deterministic Jitter Test (TP3_EQ)

Test ID

For HBR2 and HBR25

- 1236001 – Deterministic Jitter Test (TP3_EQ) - HBR2CPAT
- 1236011 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - HBR2CPAT
- 1235001 – Deterministic Jitter Test (TP3_EQ) - D10.2
- 1235011 – Deterministic Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the deterministic jitter accompanying the data transmission. The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

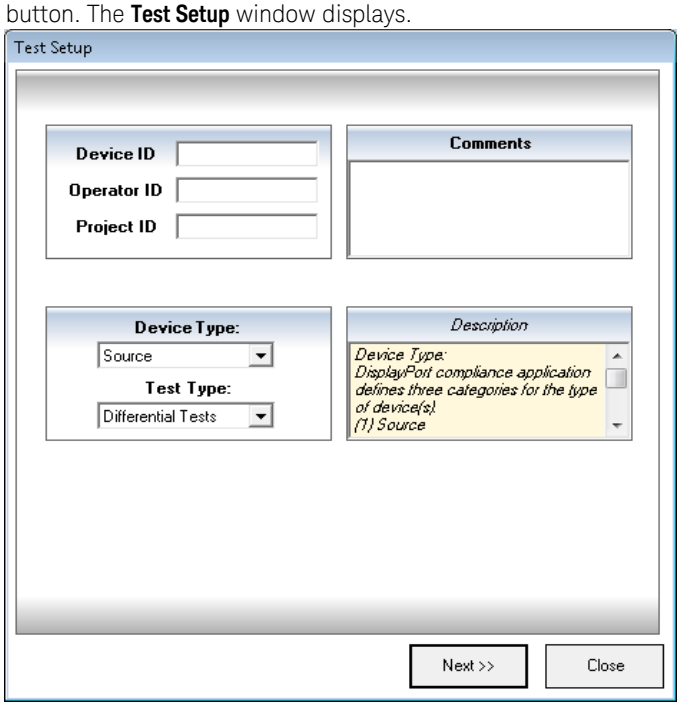
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Deterministic Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2, HBR25
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	HBR2CPAT and D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



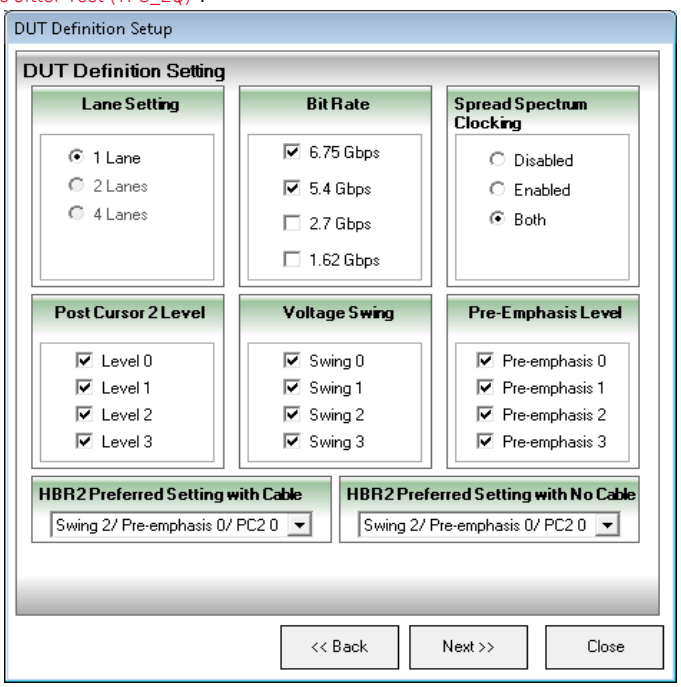
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

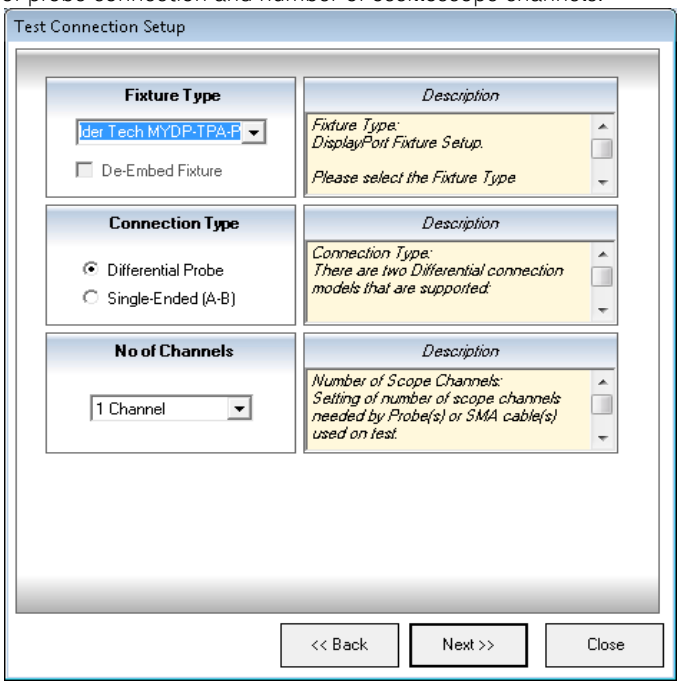
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

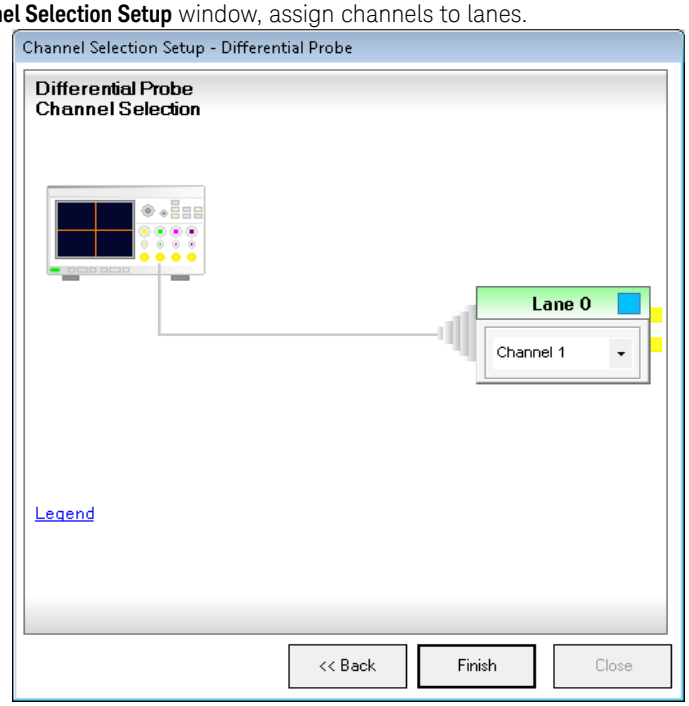
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Deterministic Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

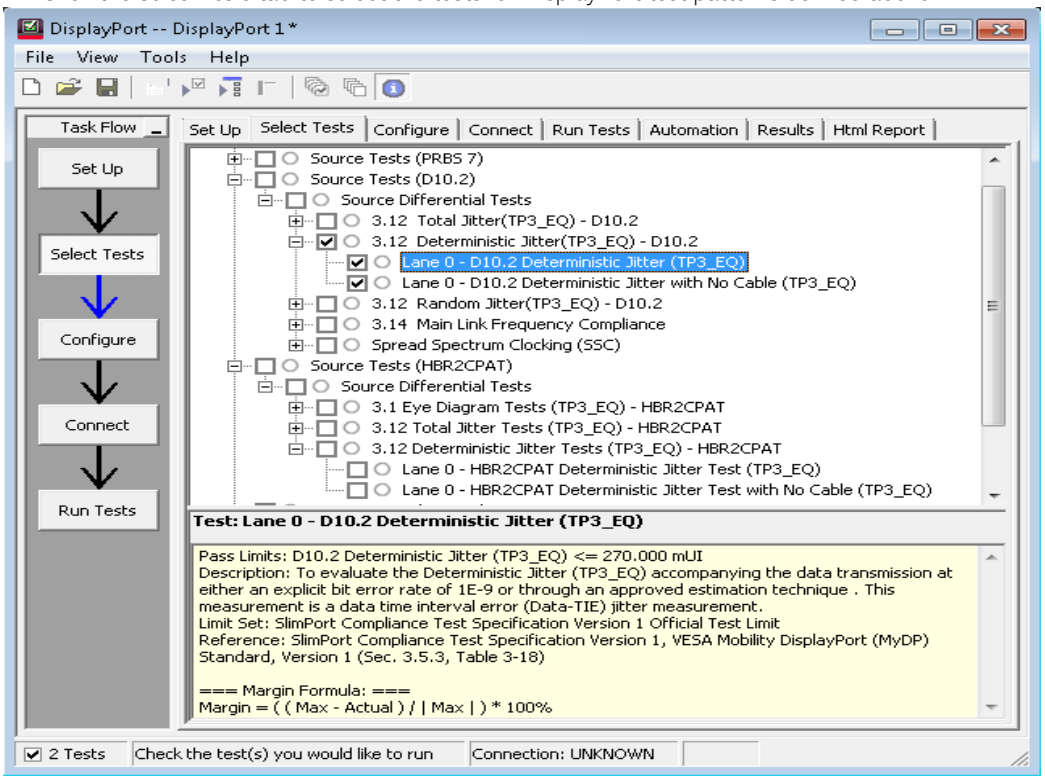


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 151 Deterministic Jitter at TP3_EQ (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
A_{p-p}	0.49 UI

Table 152 Deterministic Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
$T_{TX-DJ\_D10.2\_HBR2}$	0.25 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*

For HBR2CPAT

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

For D10.2

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured deterministic jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Random Jitter Test (TP3_EQ)

Test ID

For HBR2 and HBR25

- 1238001 – Random Jitter Test (TP3_EQ) - D10.2
- 1238011 – Random Jitter Test with No Cable Model (TP3_EQ) - D10.2

Test Overview

The objective of this test is to evaluate the random jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. The jitter is separated into each jitter components and the random jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

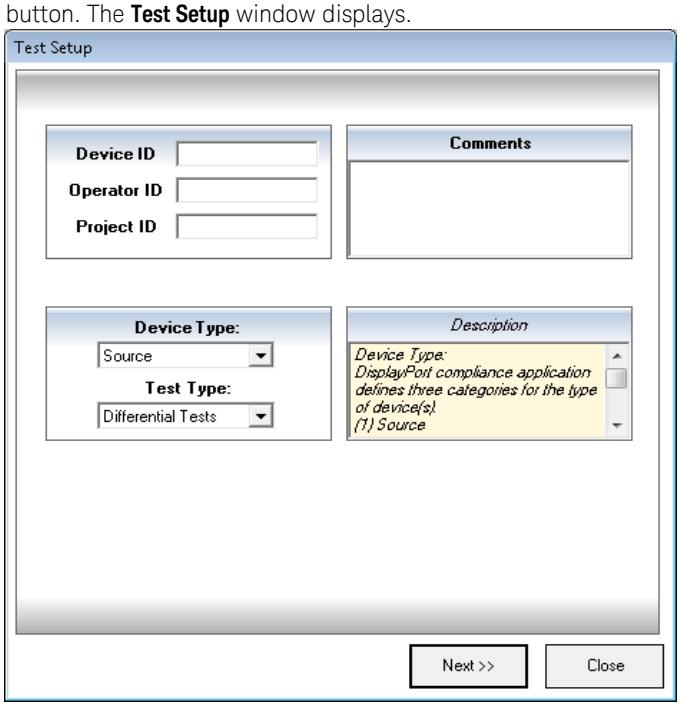
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Random Jitter Test (TP3_EQ)

Test Parameter	Condition
Test Point	TP3_EQ
Bit Rate	HBR2, HBR25
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Any voltage level such that the source meets the Pass/Fail criteria.
Pre-Emphasis Level	Any pre-emphasis level such that the source meets the Pass/Fail criteria.
Post-Cursor2 Level	Any post-cursor 2 level such that the source meets the Pass/Fail criteria.
Test Lane	Lane 0
Test Pattern	D10.2
Cable Model	“Worst Case” and “Zero Length” conditions

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



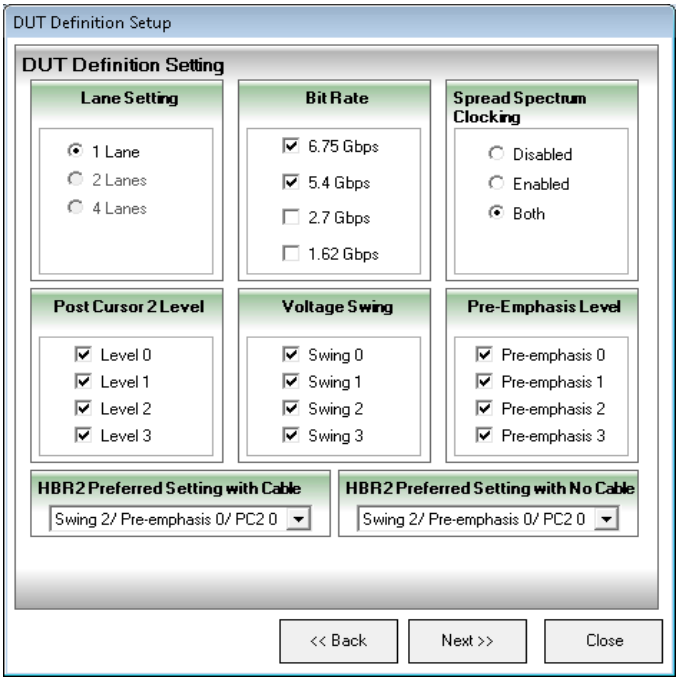
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

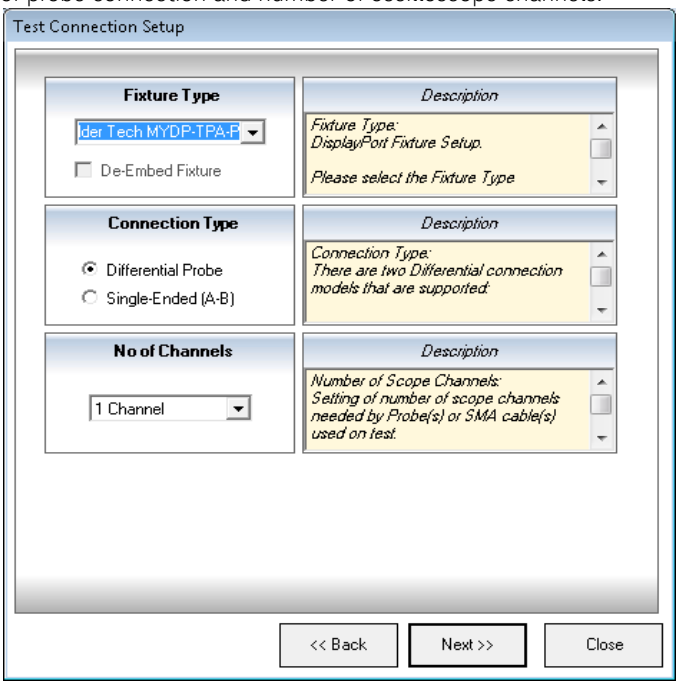
b Select **Device Type:** as **Source**, **Test Type:** as **Differential Tests**.

c Click **Next**.

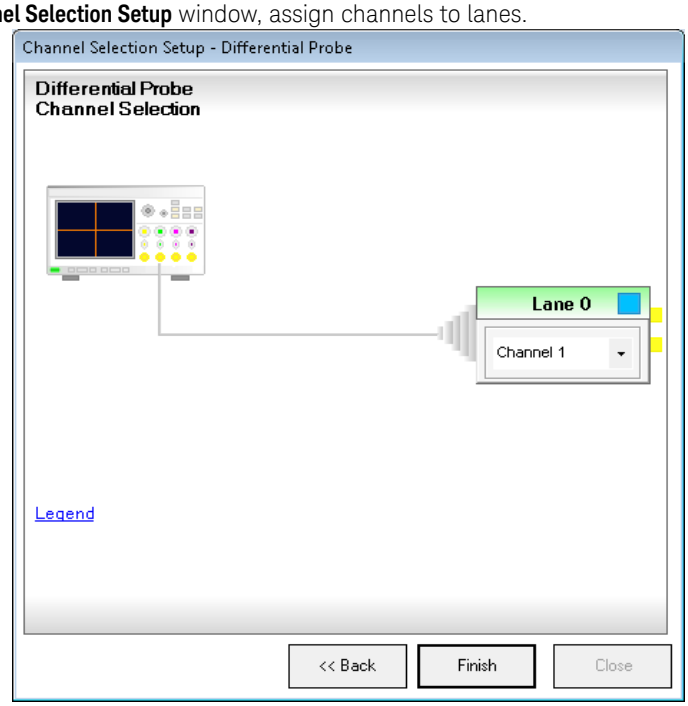
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Random Jitter Test (TP3_EQ)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

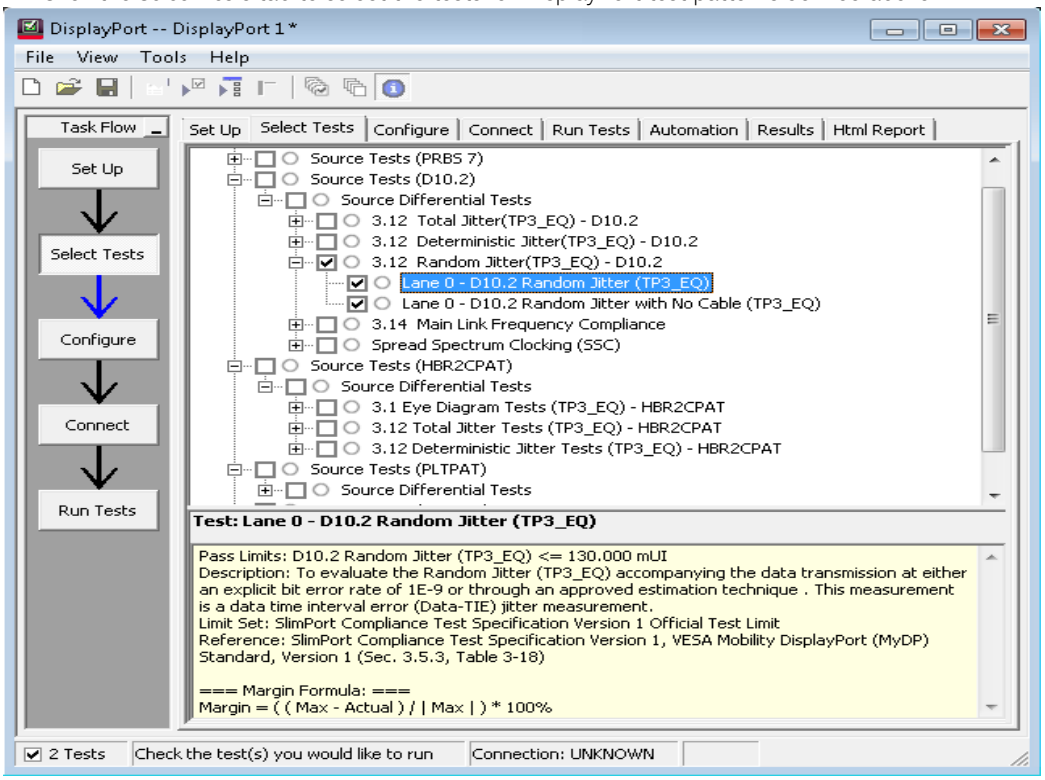


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
   a For Eye Diagram Test (TP3_EQ): Use “Worst Cable Model” as defined in the section “Cable Model”.
   b For Eye Diagram Test with No Cable Model (TP3_EQ): Use “Zero Length Cable Model” as defined in the section “Cable Model”.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Set up equalized signal as defined in the section “Equalization”.
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the clock recovery as defined in the section “Clock Recovery”.
5 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
6 Note the jitter component value from the EZJIT Plus/Complete Software.
7 Report the measurement results.

PASS Condition

Table 153 Random Jitter at TP3_EQ (for D10.2)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane)	
$T_{TX\text{-}RJ\_D10.2\_HBR2}$	0.23 UI

UI is Unit Interval.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.1*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.12.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-18*

Expected/Observable Results

The measured random jitter for the test signal at TP3_EQ shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AC Common Mode Test (Informative)

Test ID

12110001 – AC Common Mode Test (Informative)

Test Overview

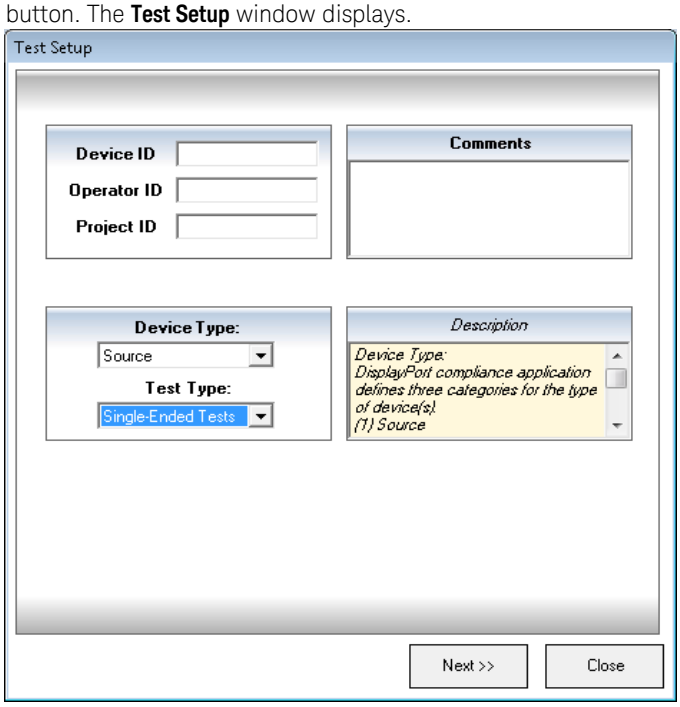
The objective of this test is to evaluate the AC Common Mode noise (unfiltered rms) of the differential data line of the DP interface.

Test Conditions for AC Common Mode Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	All bit rates supported (RBR, HBR, HBR2, HBR25)
SSC	Both SSC Conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	All voltage level supported
Pre-Emphasis Level	All pre-emphasis level supported subject to the constraints in Table 3-1 of the VESA DisplayPort 1.2a Standard
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



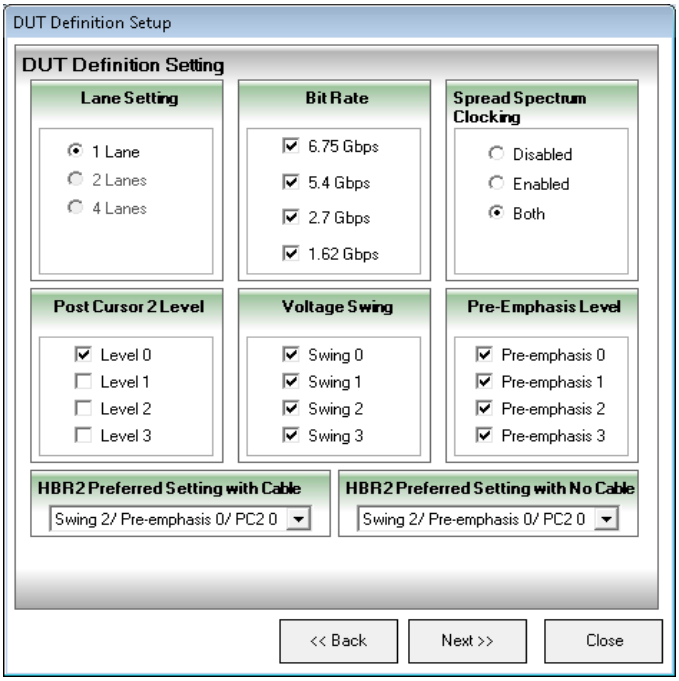
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

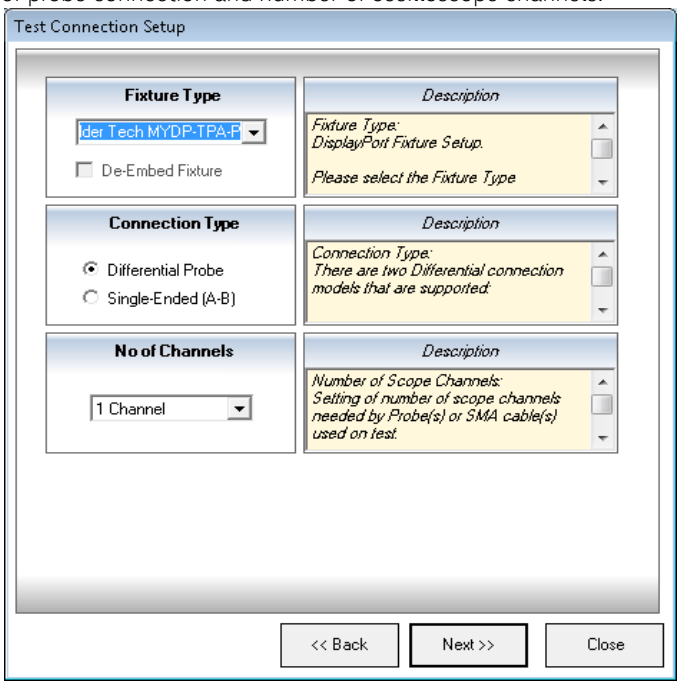
b Select **Device Type:** as **Source**, **Test Type:** as **Single-Ended Tests**.

c Click **Next**.

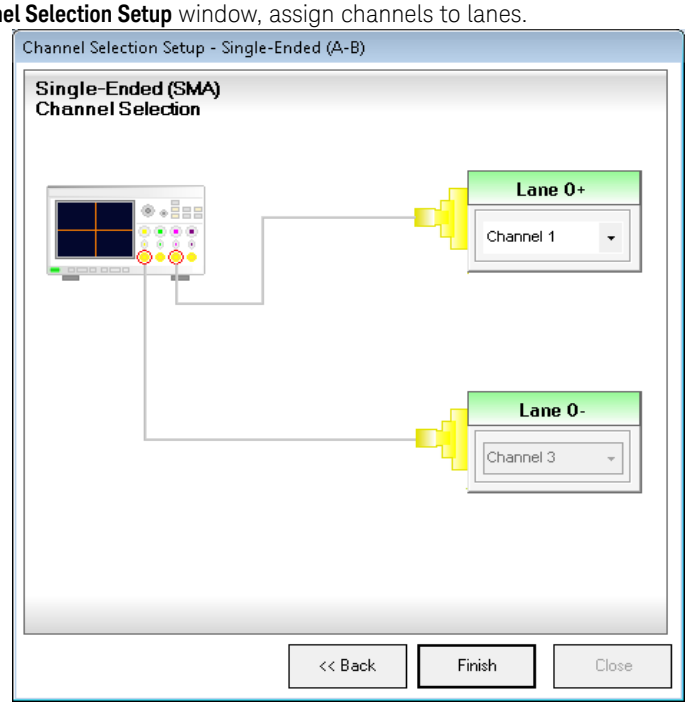
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for AC Common Mode Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

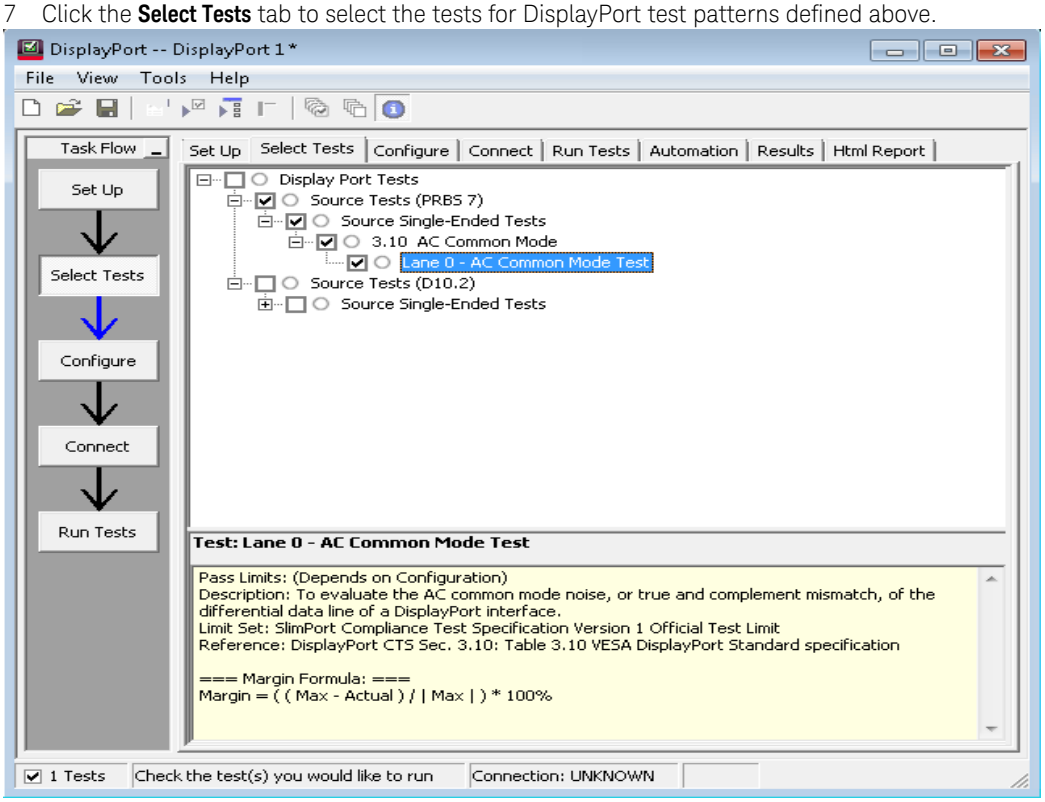


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Create FUNC3 signal, which is the common mode signal of the input single-ended signal.
4 If the filter is enabled ["Filter" configuration variable set to "High Pass Filter", "Low Pass Filter" or "None" (Default)]:
   a Create FUNC4 signal, which is the filtered FUNC3 signal by applying the High Pass filter or Low Pass filter on the FUNC3 signal based on the Configuration Variable.
5 Set up two display grids such that one grid displays the input single-ended signal while the other grid displays the common mode signal.
6 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
7 Set up the parameters for RMS voltage measurement of the common mode signal.
   a Set up the V_{rms} measurement for the common mode signal.
   b Acquire the signal until 100,000 edges are measured.
8 Get the mean for the V_{rms} measurement.
9 Report the measurement results.

PASS Condition

For RBR and HBR:

AC Common Mode Voltage $\leq$ 20mV

For HBR2, HBR25:

AC Common Mode Voltage $\leq$ 30mV

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.10*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 9.2, Table 9-6*

Expected/Observable Results

The measured AC common mode noise for the test signal shall be within the conformance limits as specified in the specification mentioned under the "PASS Condition" section for this test.

Intra-Pair Skew Test (Informative)

Test ID

12100001 — Intra-Pair Skew Test (Informative)

Test Overview

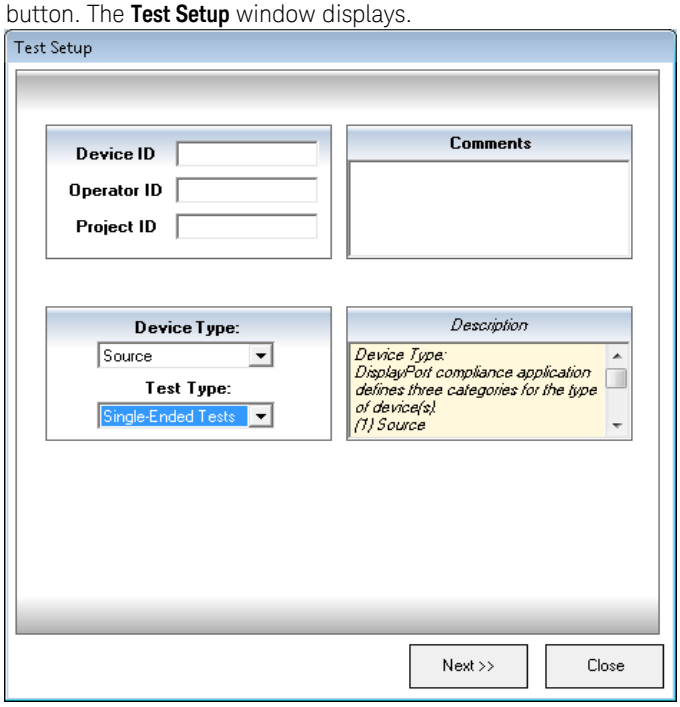
The objective of this test is to evaluate the skew or time delay between respective sides of a differential data lane in the DP interface.

Test Conditions for Intra-Pair Skew Test (Informative)

Test Parameter	Condition
Test Point	TP2
Bit Rate	Highest bit rate supported (RBR, HBR, HBR2 or HBR25)
SSC	Both SSC conditions supported (SSC Enabled and SSC Disabled)
Voltage Level	Level 2
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0 (Lane 0+ to Lane 0-)
Test Pattern	D10.2

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



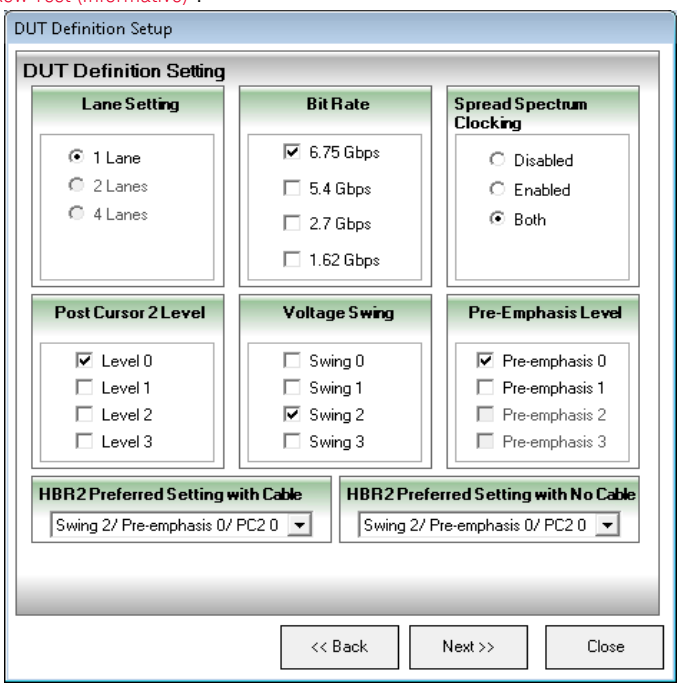
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

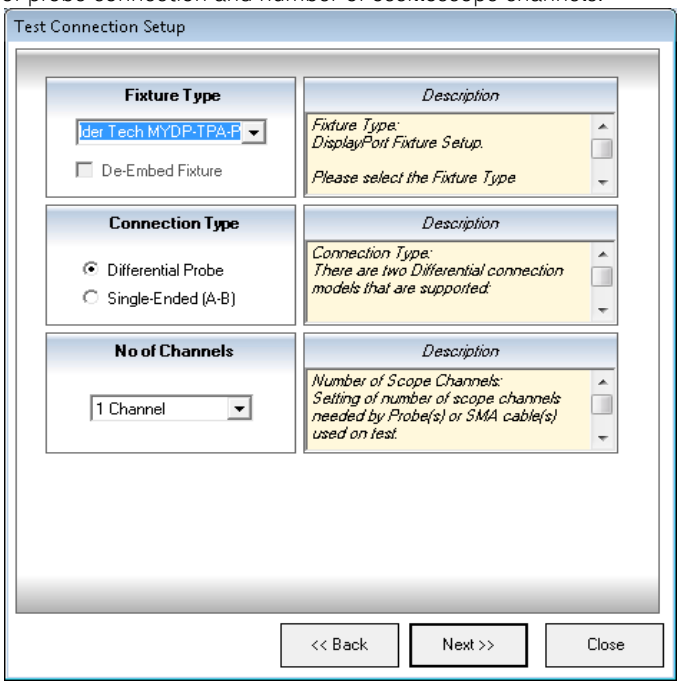
b Select **Device Type:** as **Source**, **Test Type:** as **Single-Ended Tests**.

c Click **Next**.

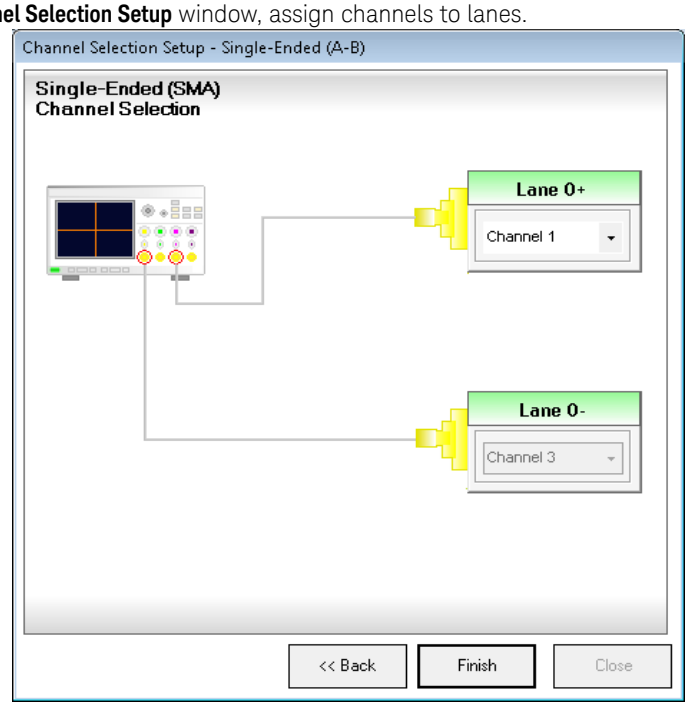
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Intra-Pair Skew Test (Informative)".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

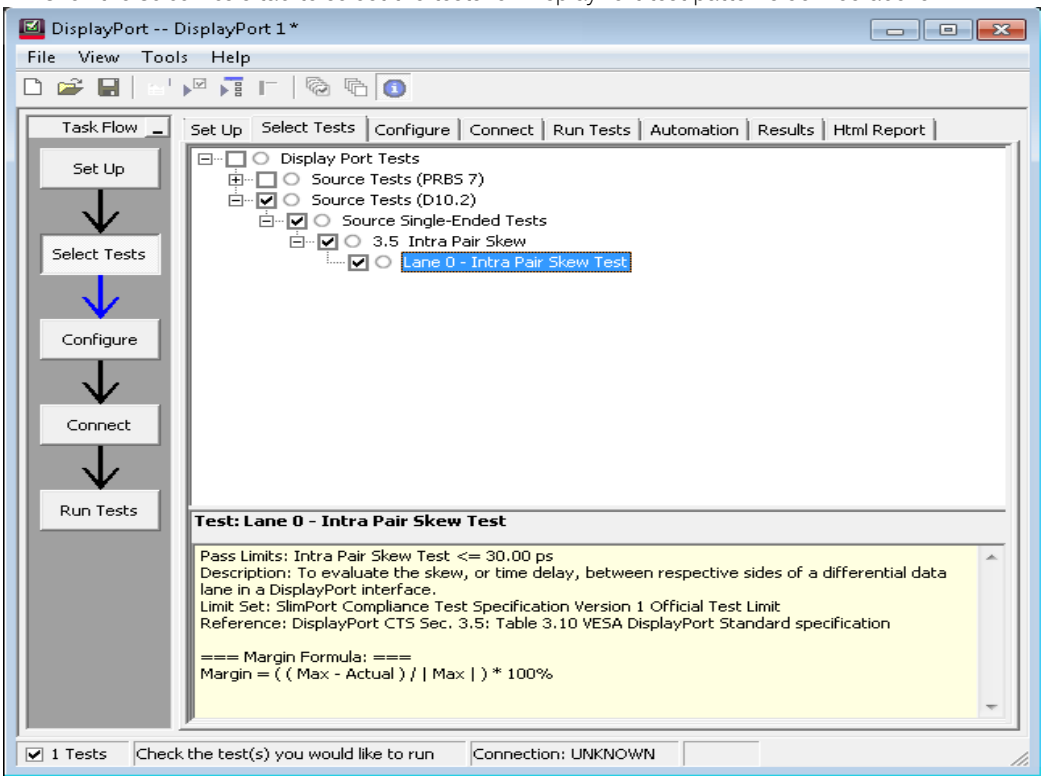


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Source Tests" on page 710 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input single-ended plus signal.
   b Scale the vertical display of the input single-ended plus signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input single-ended plus signal.
   d Verify the trigger and the amplitude of the input single-ended minus signal.
   e Scale the vertical display of the input single-ended minus signal to the optimum value.
   f Measure V_{TOP} and V_{BASE} of the input single-ended minus signal.
   g Measure the data rate of the input single-ended signal.
3 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
4 Set up the parameters to perform High Level Voltage (V_{HIGH}) and Low Level Voltage (V_{LOW}) for each input single-ended signal.
   a Scale the vertical display of the input single-ended signal to optimum value.
   b Acquire the signal for 100 waveforms.
   c Find VHIGH by measuring the average voltage at 0.06 UI to 0.75 UI of the High Level.
   d Find VLOW by measuring the average voltage at 0.06 UI to 0.75 UI of the Low Level.
   e Calculate the Transition Voltage (V_{Trans}) using the equation:

$$V_{Trans} = (V_{HIGH} + V_{LOW}) / 2$$

5 Set up the parameters for the intra-pair skew measurement:
   a Set up the measurement threshold for each single-ended data signal based on the measured Transition Voltage.
   b Set up InfiniiScan to trigger on the desired pattern.
   c Set up delta time measurement to measure time difference between the rising edge of the data true signal (D+) and the complement's (D-) falling edge:

$$D+_{Transition\_High} - D-_{Transition\_Low}$$

   d Set up delta time measurement to measure time difference between the falling edge of the data true signal (D+) and the complement's (D-) rising edge:

$$D+_{Transition\_Low} - D-_{Transition\_High}$$

   e Acquire the signal until you measure 100 edges.
   f Calculate the intra-pair skew using the equation:

$$\text{Intra-Pair Skew} = \{1/\text{Number of Edges}\}$$

$$\sum \{[(D+_{Transition\_High} - D-_{Transition\_Low}) + (D+_{Transition\_Low} - D-_{Transition\_High})] / 2\}$$

6 Report the measurement results.

PASS Condition

Intra-Pair Skew ≤ 30 ps

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 3.5*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3, Table 3-17*

Expected/Observable Results

The measured intra-pair skew for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

21 SlimPort Sink Tests

Overview

Test Point Definition for SlimPort Sink Tests

NOTE Sink Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Sink DUT at Test Point 3 (TP3) as shown in Figure 159. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

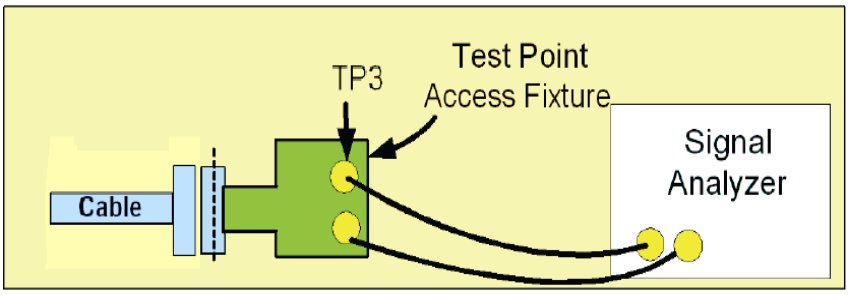


Figure 159 Test Point 3 Connection for SlimPort Sink Tests

Table 154 defines the test point fixtures and instruments used for SlimPort (MyDP HBR25) Sink Tests:

Table 154 Test Point Fixtures and Instruments for SlimPort (MyDP HBR25) Sink Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Calibration of Stress Signal

For the calibration of the stress signal, you must test the stress signal in the manner shown in the Figure 160 for RBR and Figure 161 for HBR and HBR2.

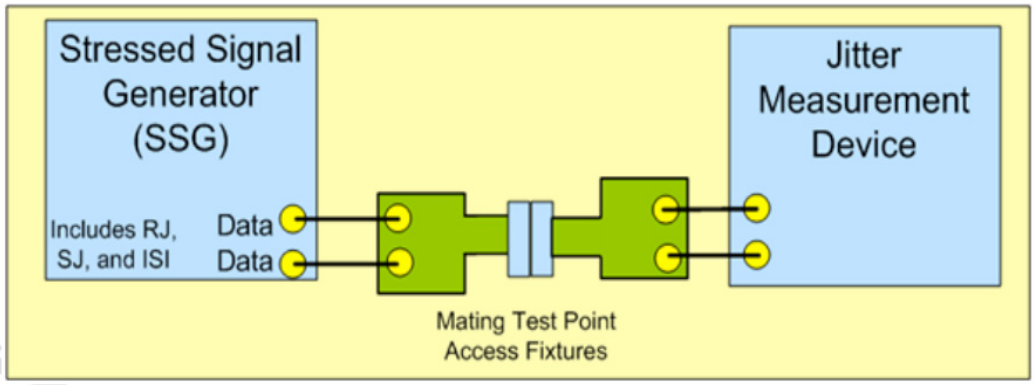


Figure 160 Test Point 3 Connection for Stress Signal Calibration of RBR

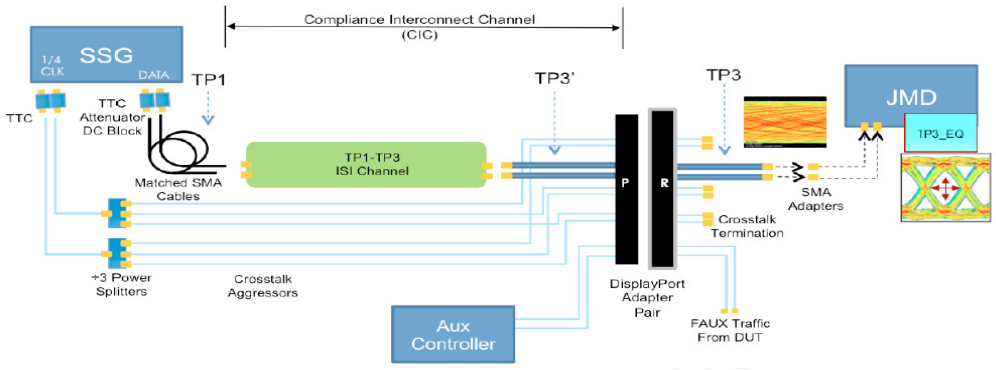


Figure 161 Test Point 3 Connection for Stress Signal Calibration of HBR and HBR2

Table 155 defines the Test Point Fixtures and Instruments for Stress Signal Calibration:

Table 155 Test Point Fixtures and Instruments for Stress Signal Calibration

Test Requirement	Device Used
Stress Signal Generator (SSG)	Bit Error Rate Tester ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Jitter Measurement Device (JMD)	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for SlimPort Sink Tests

Perform the following steps before you run the compliance tests on the sink device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 162).

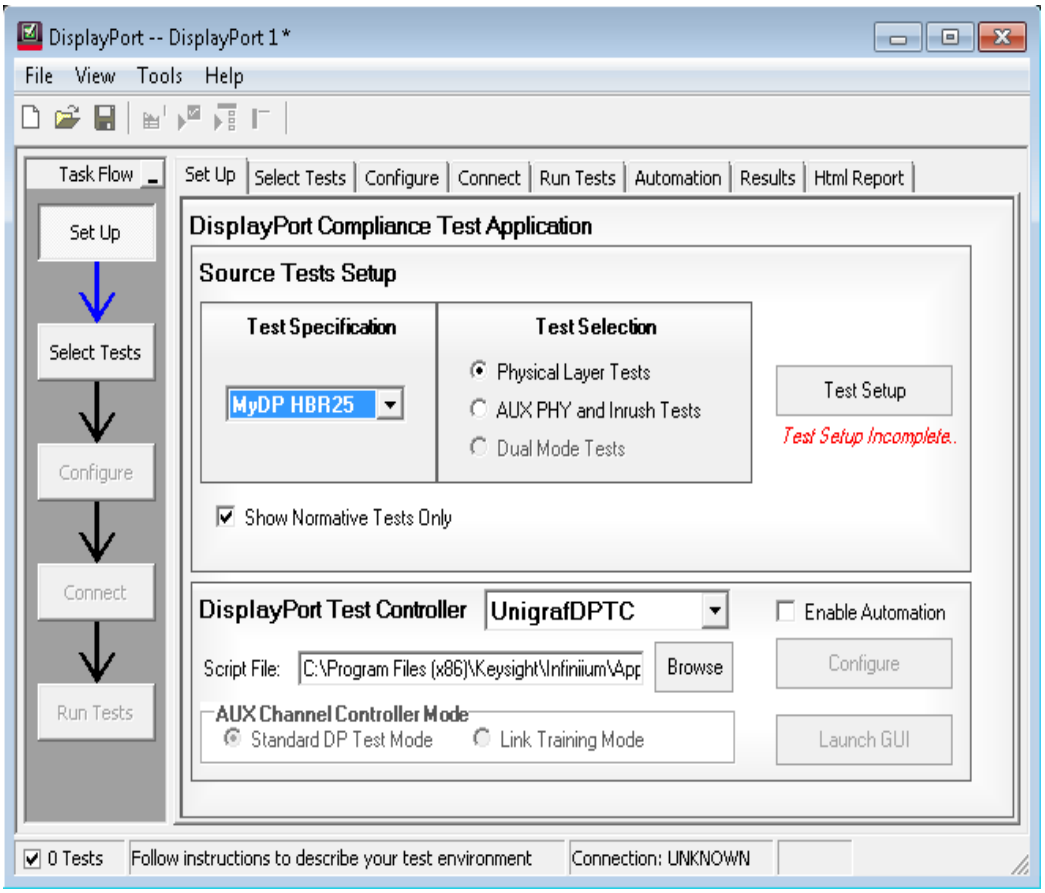


Figure 162 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with SlimPort Standards, select **MyDP HBR25** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for SlimPort Sink Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

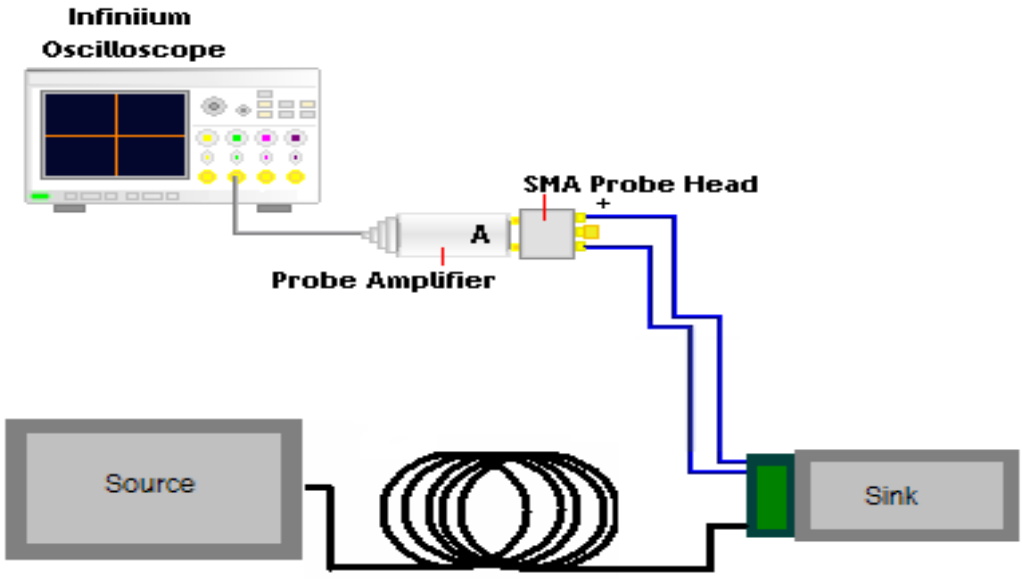


Figure 163 Sample connection diagram for SlimPort Sink Tests

Sink Eye Diagram Test

Test ID

12140001 — Eye Diagram Test

Test Overview

The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the following specifications for degradation:

- Voltage Level:
  - 90mV peak to peak +/- 10% for HBR2 at TP3_EQ (Table 3-18, DP1.2a)
  - 150mV peak to peak +/- 10% for HBR at TP3_EQ (Table 3-25, DP1.2a)
  - 46mV peak to peak +/- 10% for RBR at TP3 (Table 3-26, DP1.2a)

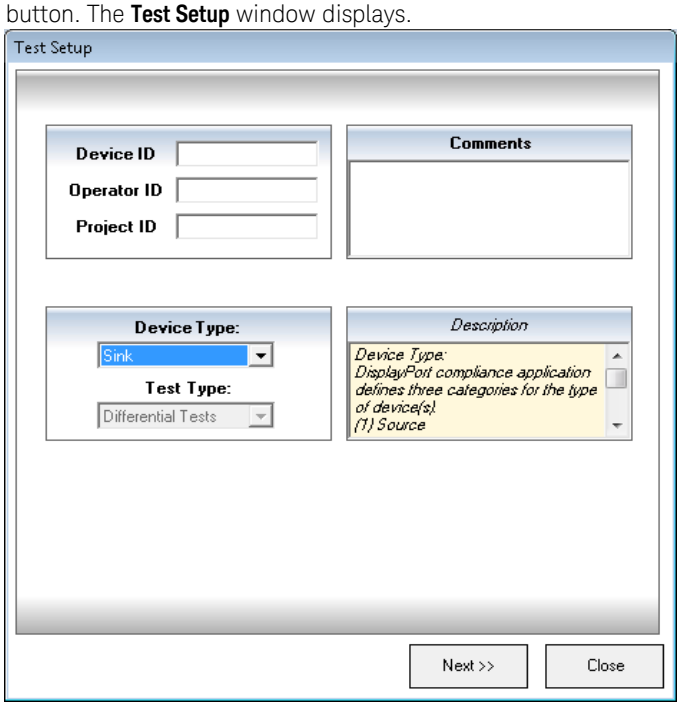
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR25–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR25)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR25–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



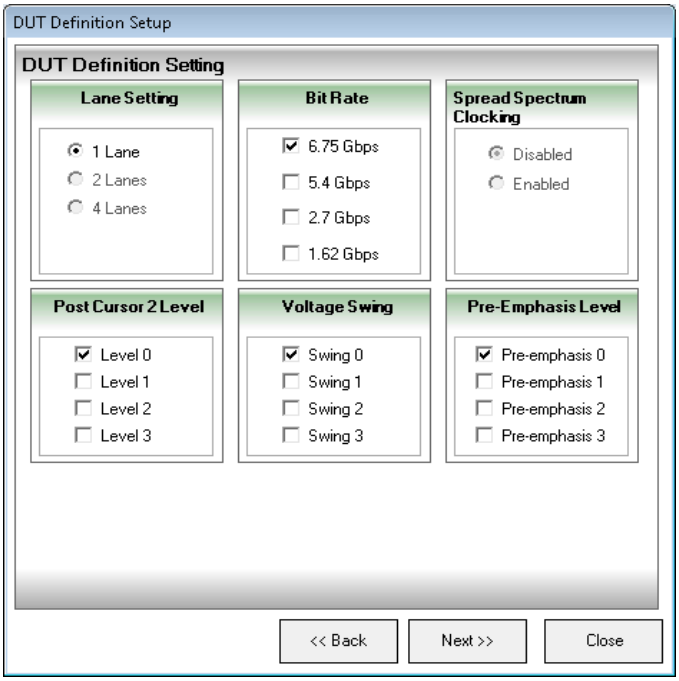
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

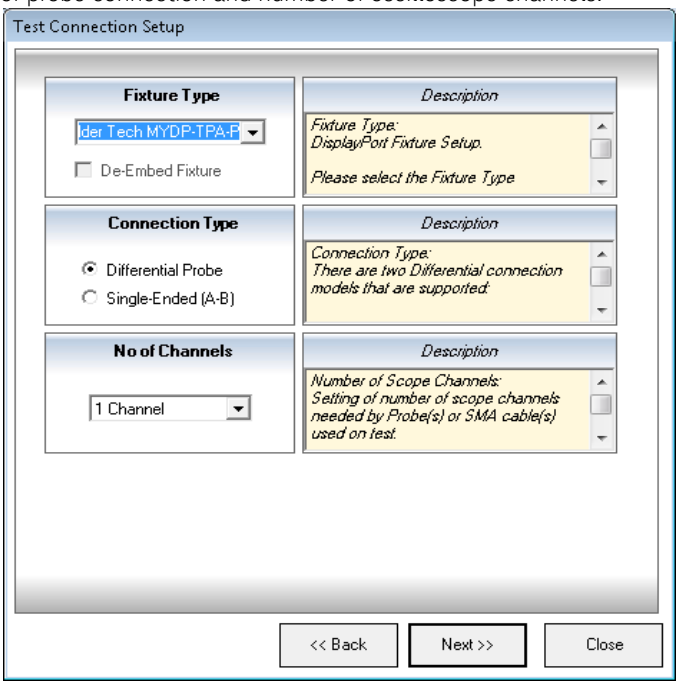
b Select **Device Type:** as **Sink**, **Test Type:** automatically grays out.

c Click **Next**.

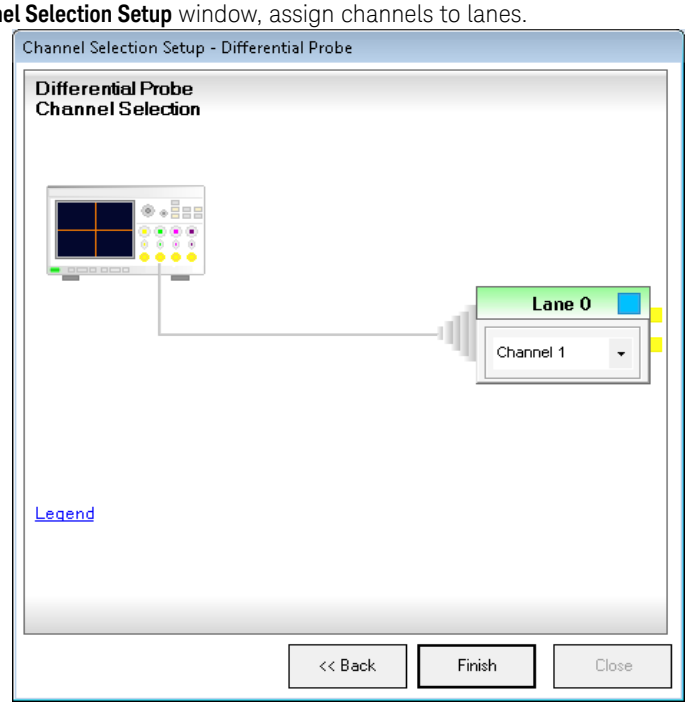
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

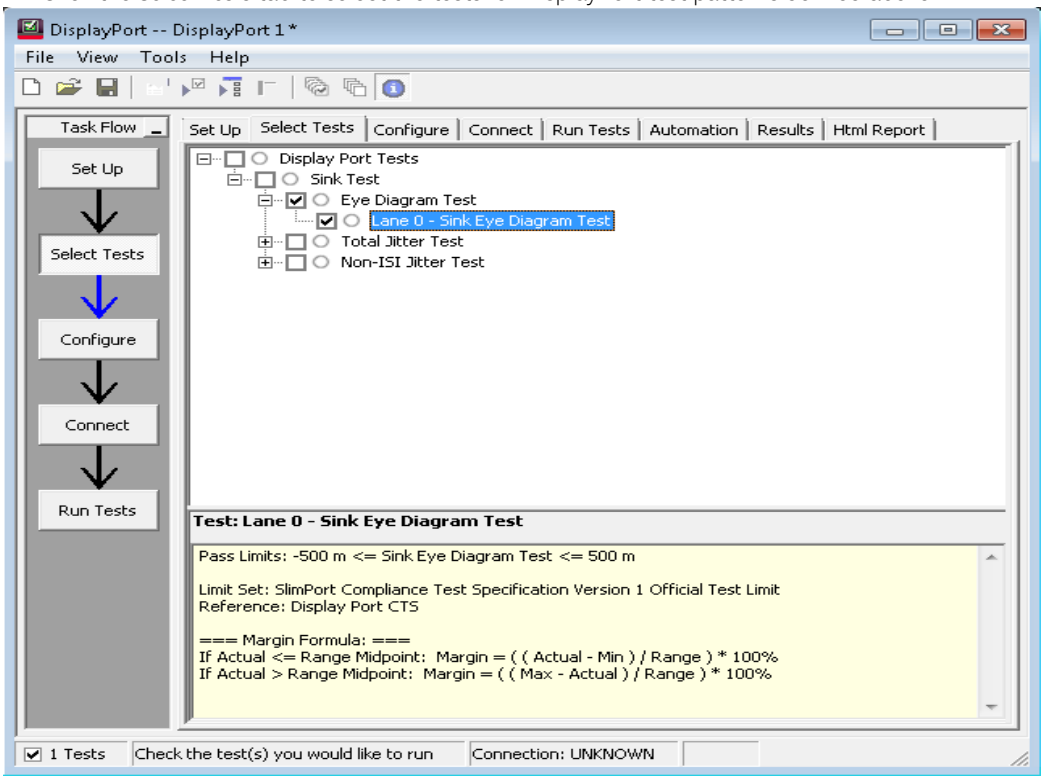


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Sink Tests" on page 828 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 156 shows the voltage and time coordinates for the mask used for the eye diagram.

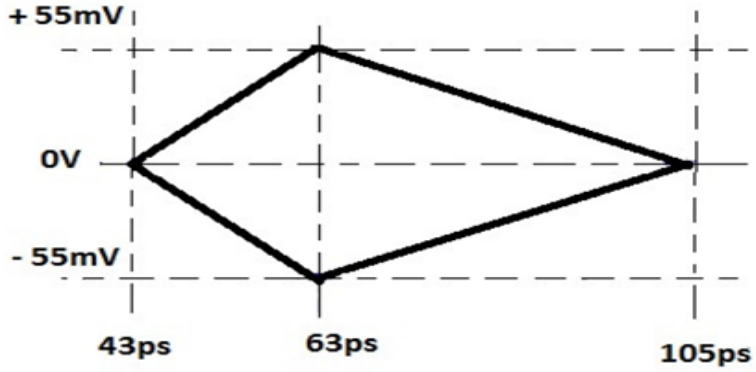


Figure 164 Eye Mask at TP3_EQ (HBR25)

Table 156 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

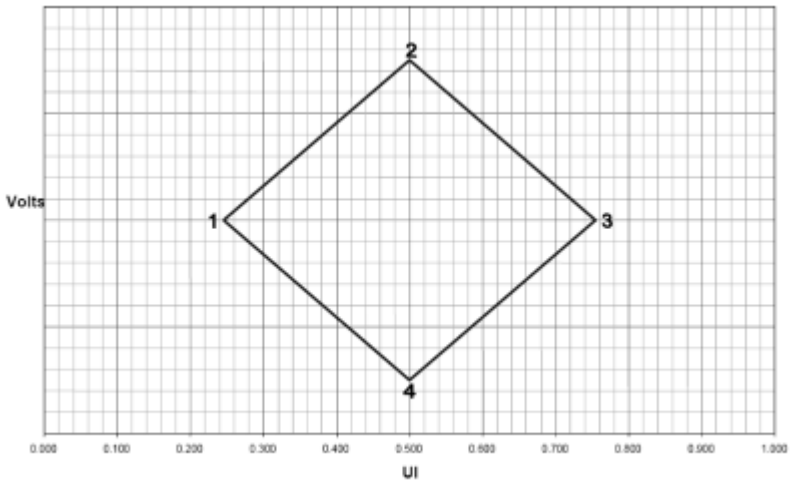


Figure 165 The Sink Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Table 157 Eye Diagram Mask Coordinates for TP3_EQ (HBR2)

Mask Point	Time (UI)	Voltage (V)
1	Any UI location (x), where the EYE width is open from x to x + 0.38UI	0.000
2	Any passing UI location between 0.375 and 0.625UI	0.0045
3	Point 1 + 0.38UI	0.0000
4	Same as Point 2	-0.0045

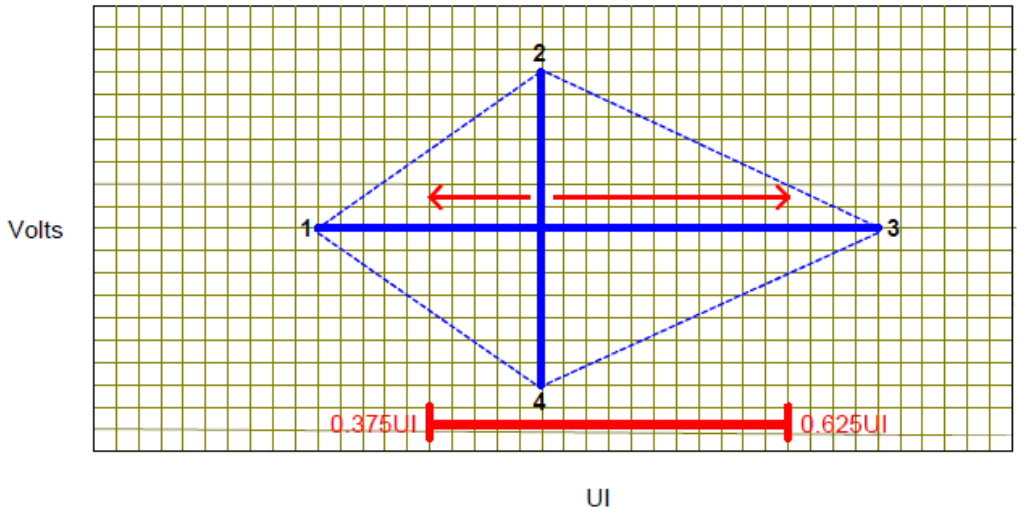


Figure 166 The Sink Eye Mask at TP3_EQ (HBR2)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Sink Total Jitter Test

Test ID

12210001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

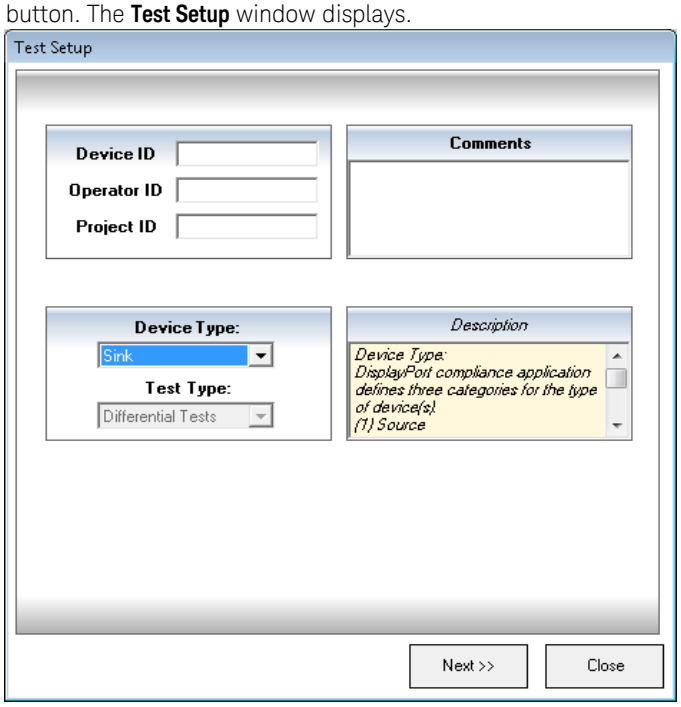
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR25–TP3_EQ
Bit Rate	All bit rates supported (RBR, HBR, HBR2 and HBR25)
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR25–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



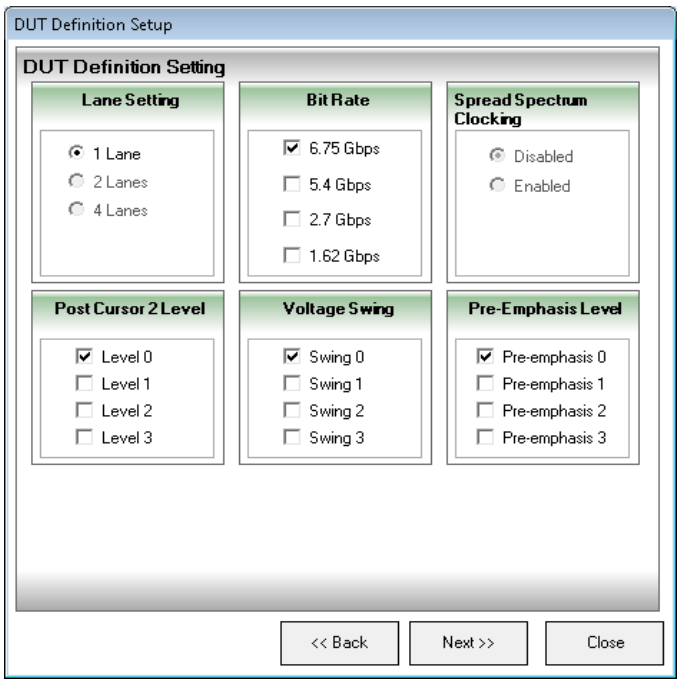
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

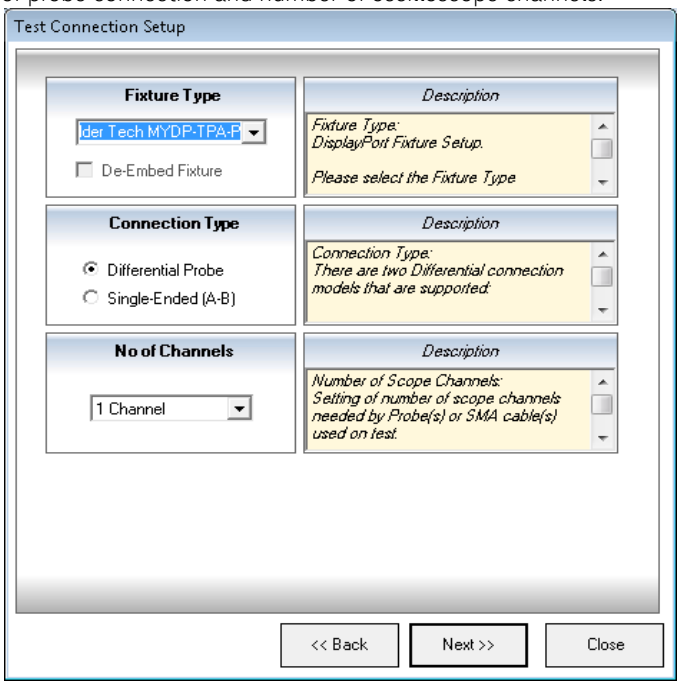
b Select **Device Type:** as **Sink**, **Test Type:** automatically grays out.

c Click **Next**.

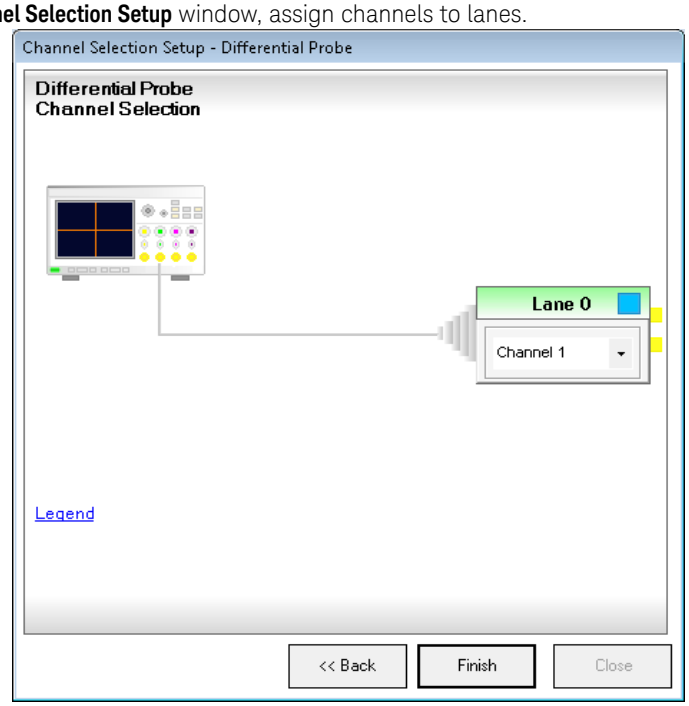
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

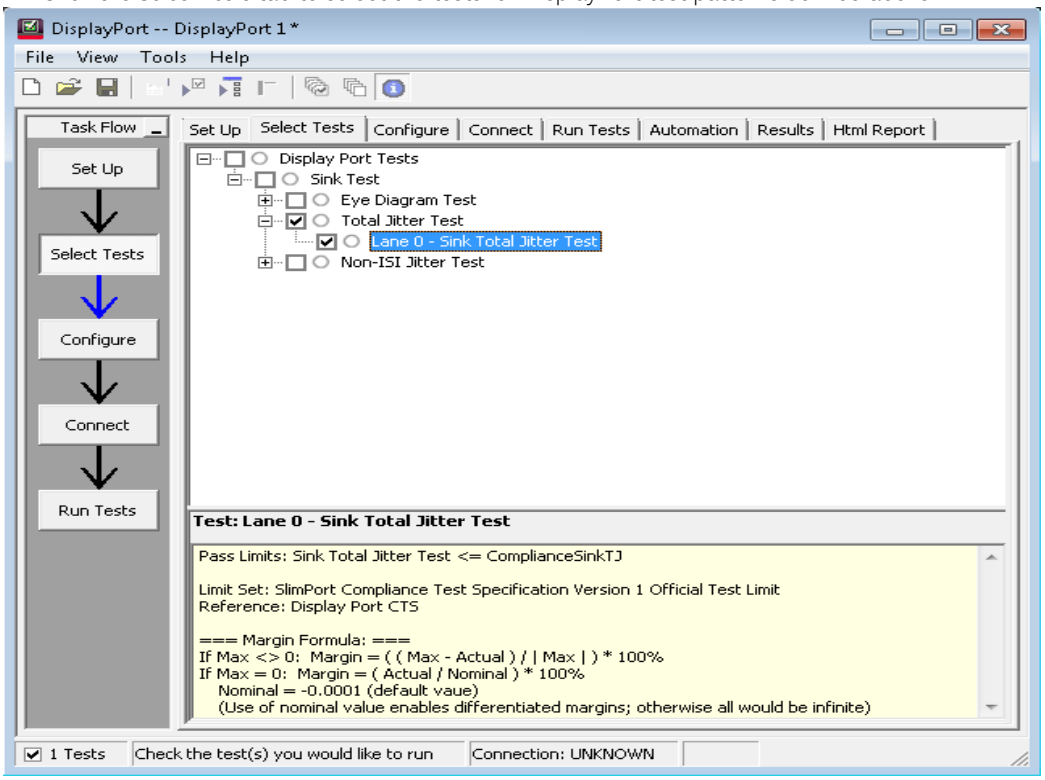


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Sink Tests" on page 828 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 158 Total Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	0.580 UI*

* The limits for the Total Jitter are derated by 0.04 UI from 0.62 UI in DisplayPort 1.2a Standard.

Table 159 Total Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Sink Non-ISI Jitter Test

Test ID

12220001 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

You can use this test to calibrate the degraded source signal or stress signal for sink jitter tolerance test. To verify the sink performance, a source signal is degraded with a prescribed amount and type of jitter as well as signal level, based on the specifications for degradation.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Calculate Non-ISI Jitter using the following equation:

$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

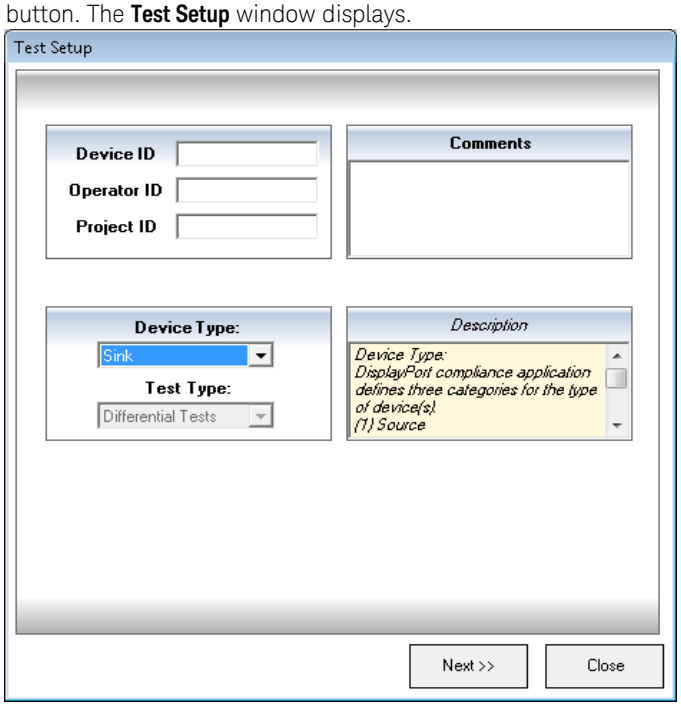
With the degraded source signal applied to the sink (receiver), the sink shall perform at 10^{-9} BER or better.

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR, HBR2, HBR25–TP3_EQ
Bit Rate	All bit rates (for RBR, HBR, HBR2 and HBR25) supported
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	RBR, HBR–PRBS7 HBR2, HBR25–HBR2CPAT

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



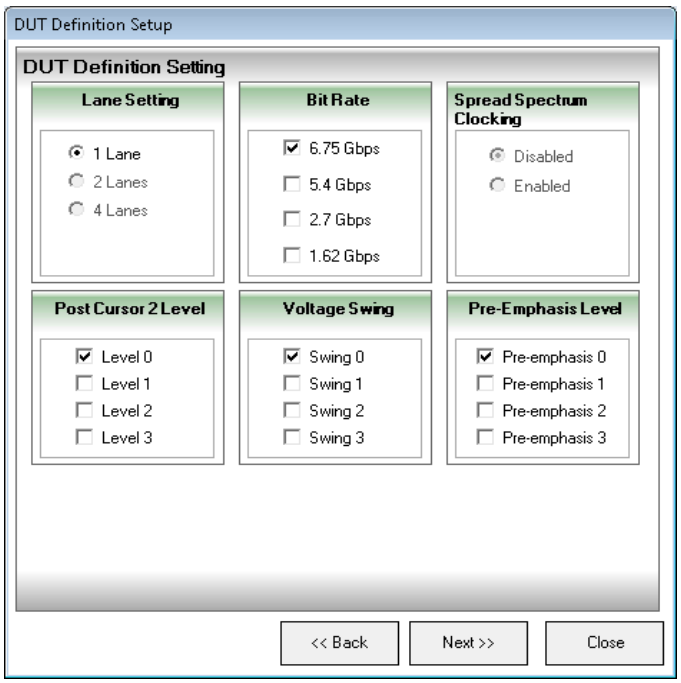
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

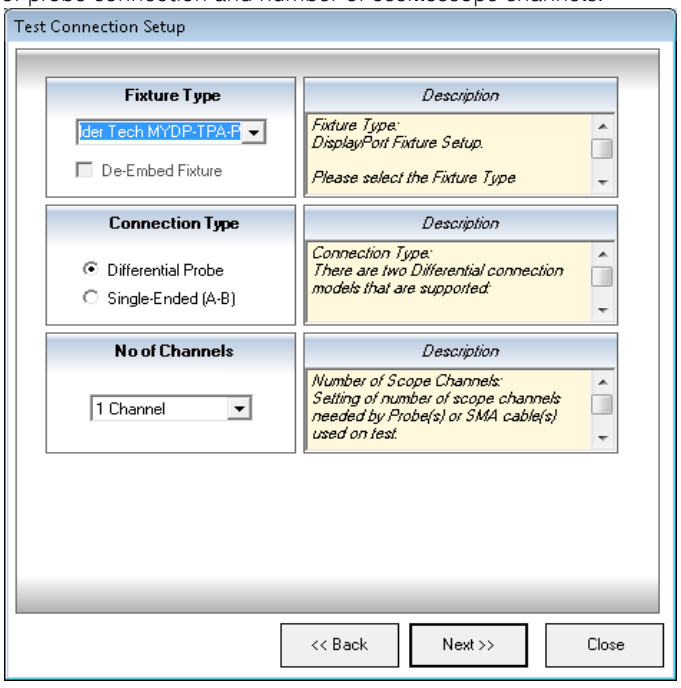
b Select **Device Type:** as **Sink**, **Test Type:** automatically grays out.

c Click **Next**.

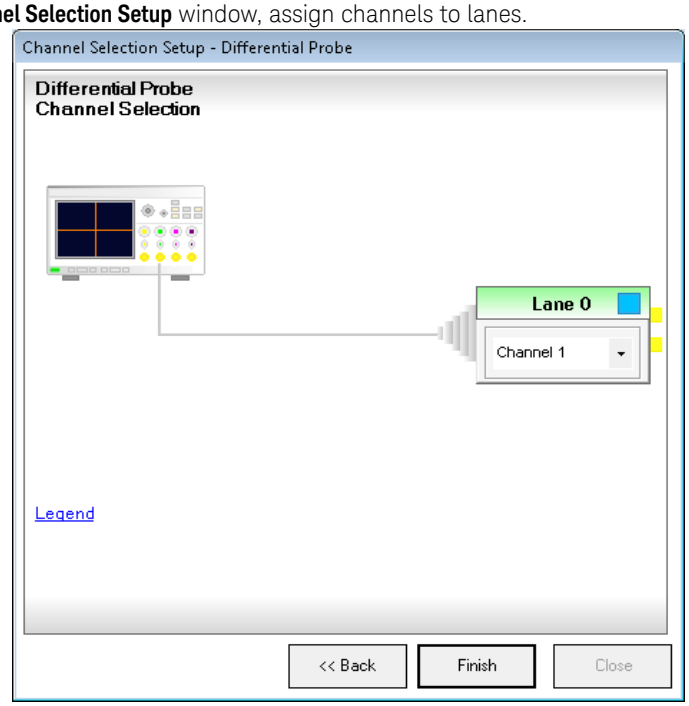
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

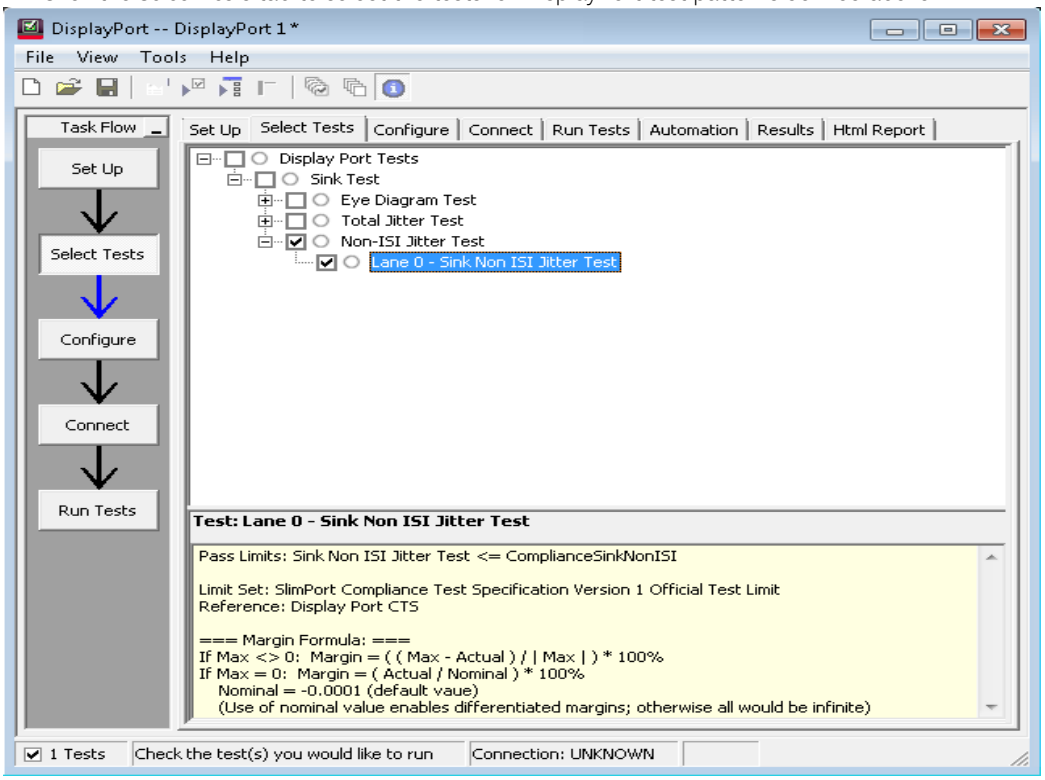


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Sink Tests" on page 828 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Sink Equalizer)
   a Scale the vertical display of the input signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the input signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

The calibrated EYE opening of the signal applied:

- For HBR2: 90mV measured at TP3_EQ
- For HBR: 150mV measured at TP3_EQ
- For RBR: 46mV measured at TP3

Table 160 Non ISI Jitter (for HBR2CPAT)

	Receiver Connector (TP3_EQ)
High-Bit Rate 2 (5.4 Gb/s per lane) at TP3_EQ	
A_{p-p}	-

Table 161 Non ISI Jitter (for PRBS7)

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 4.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

22 SlimPort Cable Tests

Overview

Test Point Definition for SlimPort Cable Tests

NOTE Cable Tests are meant only for the Test Automation of DisplayPort Receiver Tests (Keysight N4990A-155 or BIT-2051-0155-0).

Test the Cable DUT at Test Point 3 (TP3) as shown in Figure 167. Unless specifically stated under the Test Conditions, all supported lanes for the DUT shall be evaluated:

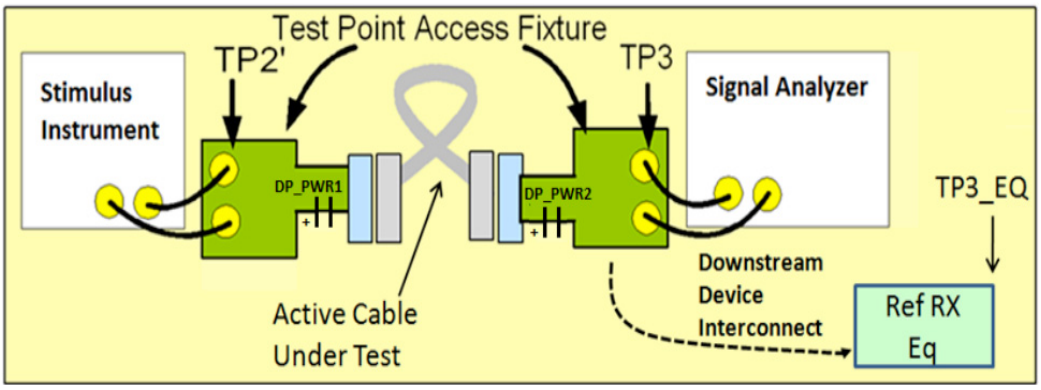


Figure 167 Test Point 3 Connection for SlimPort Cable Tests

Table 162 defines the test point fixtures and instruments used for SlimPort (MyDP HBR25) Cable Tests:

Table 162 Test Point Fixtures and Instruments for SlimPort (MyDP HBR25) Cable Tests

Test Requirement	Device Used
Stimulus Instrument	Pulse Pattern Generator ▪ N4903B J-BERT High Performance Serial BERT ▪ M8020A J-BERT High Performance BERT
Test Point Access Fixture	DisplayPort Test Point Adapter For DisplayPort Connector ▪ Wilder Technologies DP-TPA-R* For mini DisplayPort Connector ▪ Wilder Technologies mDP-TPA-R* ▪ Luxshare ICT mDP Plug (mDP-TPA-R)** ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters. ▪ **Use Luxshare ICT DP-TPA-A AUX Control board for all Luxshare ICT Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Table 163 defines the input signal parameters applied by the stimulus instrument at TP2:

Table 163 Input Signal Parameters by Stimulus Instrument

RBR	▪ Reference Table 3-22 and Table 3-24, DP 1.2a ▪ Edge Rate (20-80): 155-165ps (260mUI) ▪ Eye Height: 400mV ▪ Total Jitter: 270mUI ▪ ISI: 100mUI ▪ Random Jitter (rms): 7.9mUI ▪ Sinusoidal Jitter: ~75mUI at 20MHz (Adjust to achieve Total Jitter)
HBR	▪ Reference Table 3-22 and Table 3-23, DP 1.2a ▪ Edge Rate (20-80): 90-100ps (260mUI) ▪ Eye Height: 350mV ▪ Total Jitter: 420mUI ▪ ISI: 144mUI ▪ Random Jitter (rms): 13.2mUI ▪ Sinusoidal Jitter: ~117mUI at 20MHz (Adjust to achieve Total Jitter)

Setting Up the DisplayPort Compliance Test Application for SlimPort Cable Tests

Perform the following steps before you run the compliance tests on the cable device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 168).

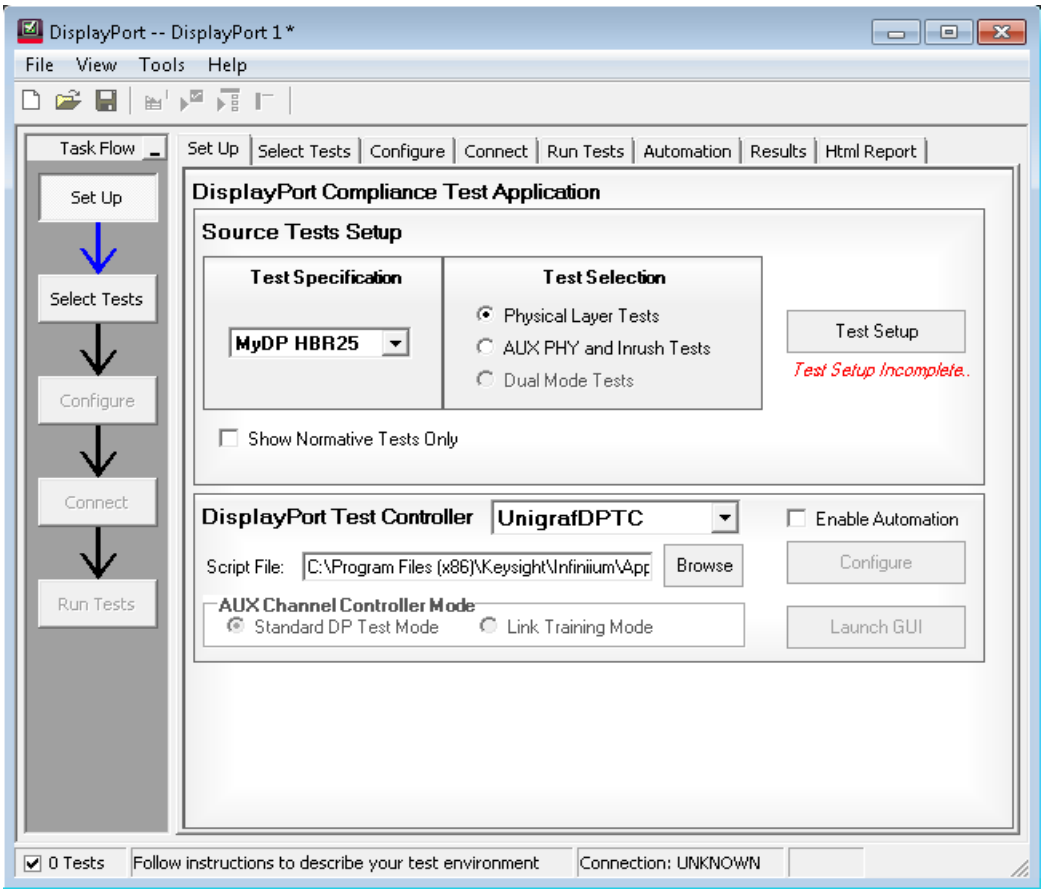


Figure 168 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with SlimPort Standards, select **MyDP HBR25** from the drop-down options in the **Test Specification** area and select **Physical Layer Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Probing/Connection Set Up for SlimPort Cable Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests.

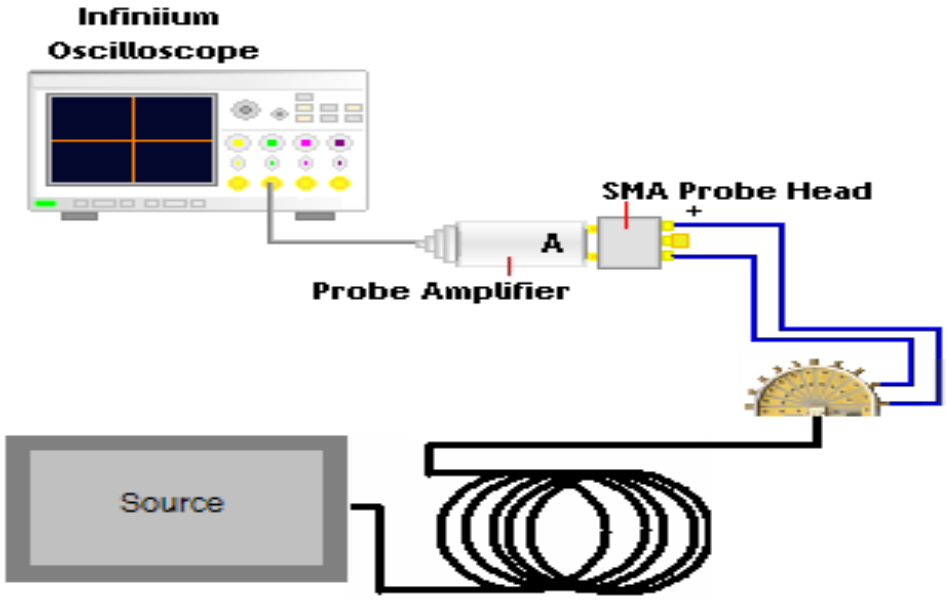


Figure 169 Sample connection diagram for SlimPort Cable Tests

Cable Eye Diagram Test

Test ID

12150001 – Eye Diagram Test

Test Overview

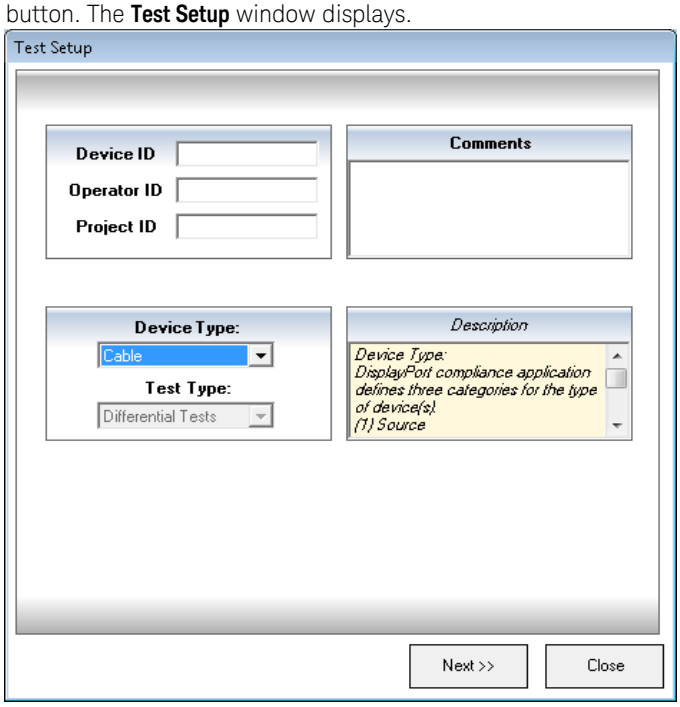
The objective of the eye diagram test is to evaluate the waveform, ensuring that the amplitude trajectories and timing variations of the waveform support the overall DP system objectives of Bit Error Rate in Data transmission.

Test Conditions for Eye Diagram Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 163
Crosstalk Signal Parameter	Quarter-rate clock signal (D24.3 pattern) is injected to lanes other than the lane under test. The characteristics of the aggressor signals are: Pattern–D24.3 Bit Rate–(Same as lane under test) Voltage Amplitude–(Same as lane under test) ▪ RBR-400mV ▪ HBR-350mV Edge Rate (20-80)–130ps at TP3

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



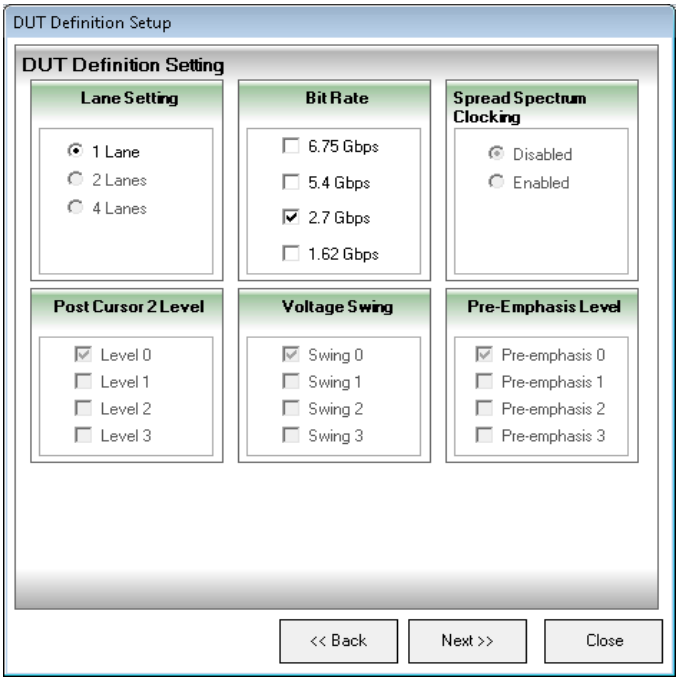
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

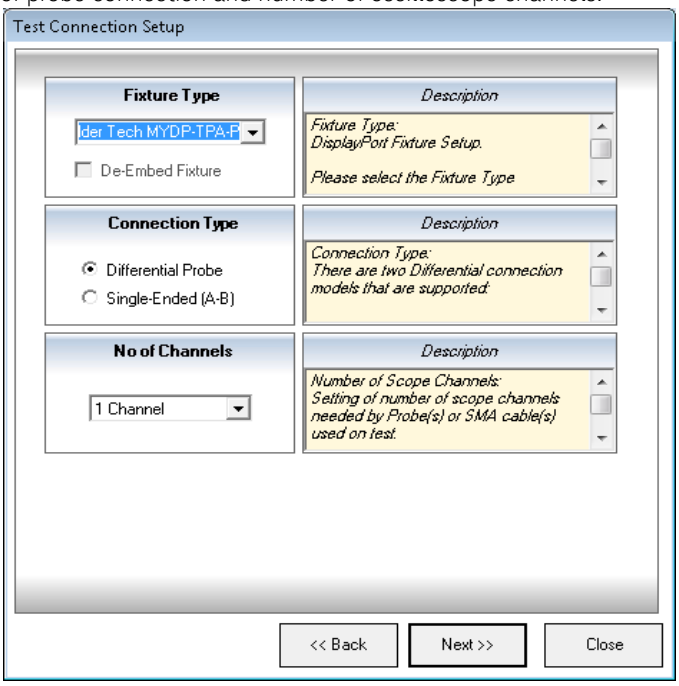
b Select **Device Type:** as **Cable**, **Test Type:** automatically grays out.

c Click **Next**.

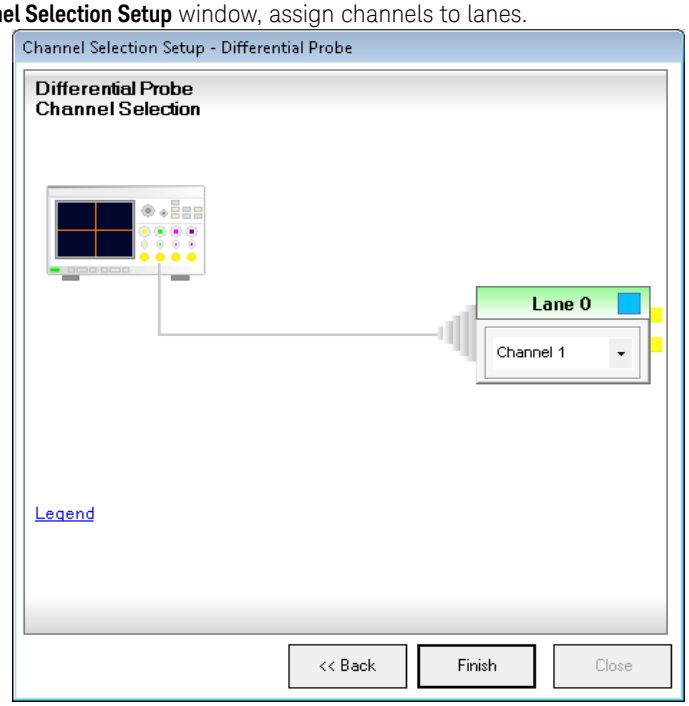
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Eye Diagram Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

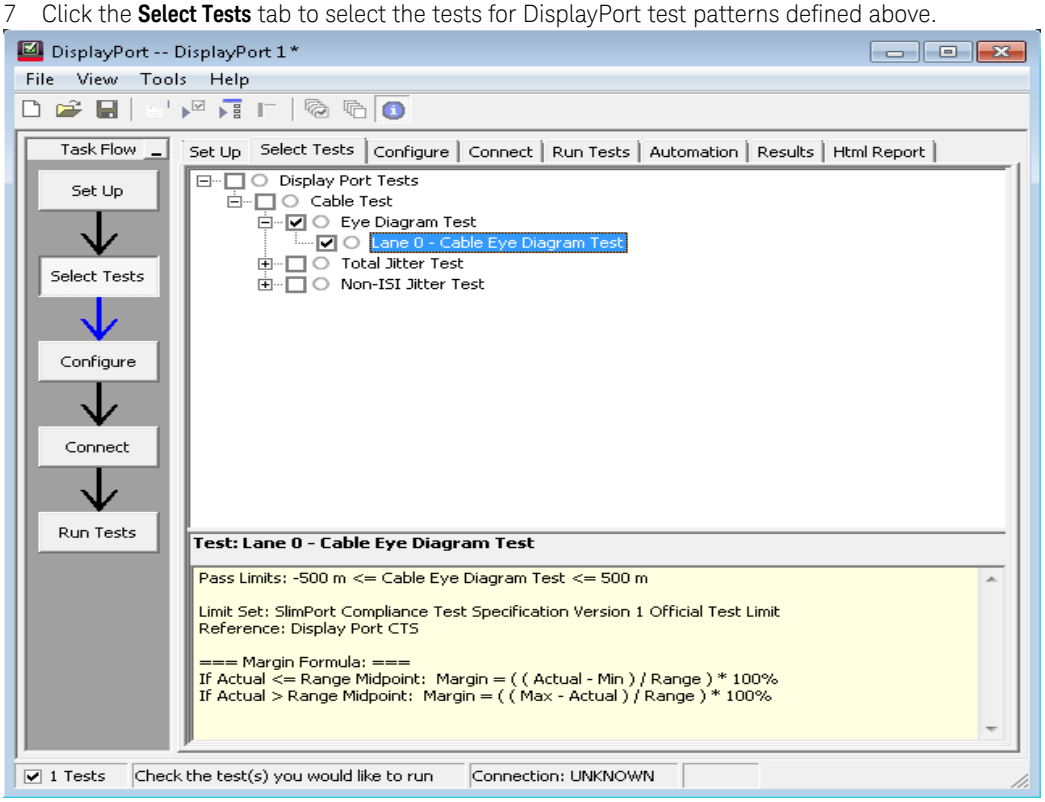


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Cable Tests" on page 852 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure:

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Fold the equalized signal to generate an eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.
7 Set up the horizontal waveform histogram on the equalized signal eye diagram to measure the left edge.
8 Set up the parameter for the Mask Test.
   a Load the eye mask based on the settings in the Configuration Variable.
   b Center the eye mask at the middle of the eye diagram based on the measured left edge.
   c Run the eye mask until 1,000,000 UI are folded.
9 Measure the jitter of the eye diagram using the Histogram.
10 Check for any signal trajectories that may have entered into the mask.
11 Report the measurement results.

PASS Condition

The following table and figure define the mask for the eye measurements. There can be no signal trajectories entering into the mask. Table 164 shows the voltage and time coordinates for the mask used for the eye diagram.

Table 164 Eye Diagram Mask Coordinates for TP3 (RBR) and TP3_EQ (HBR)

Mask Point	Bit Rate	
	Reduced (1.6 Gb/s)	**High (2.7 Gb/s)**
1	0.375, 0.000	0.246, 0.000
2	0.500, 0.023	0.500, 0.075
3	0.625, 0.000	0.755, 0.000
4	0.500, -0.023	0.500, -0.075

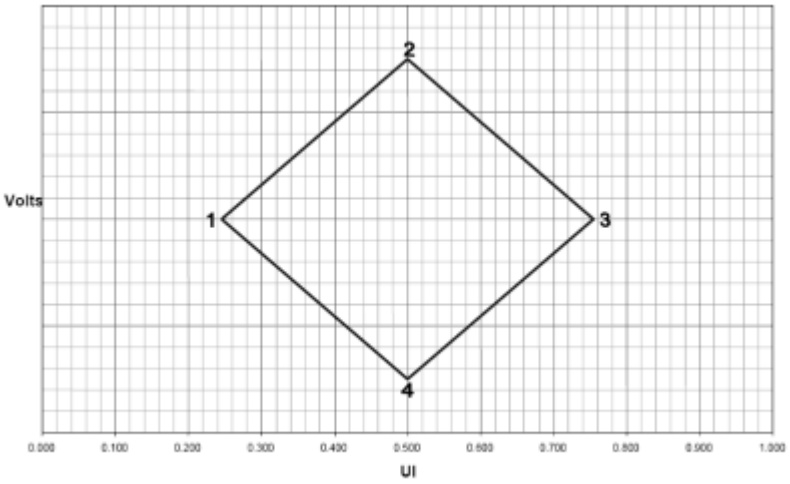


Figure 170 The Cable Eye Mask at TP3 (RBR) and TP3_EQ (HBR)

Mask Test: Zero mask failures.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.3*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.8, Table 3-26 for RBR, Table 3-25 for HBR and Table 3-18 for HBR2*

Expected/Observable Results

The measured eye diagram for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

Cable Total Jitter Test

Test ID

12230001 – Total Jitter Test

Test Overview

The objective of the test is to evaluate the total jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

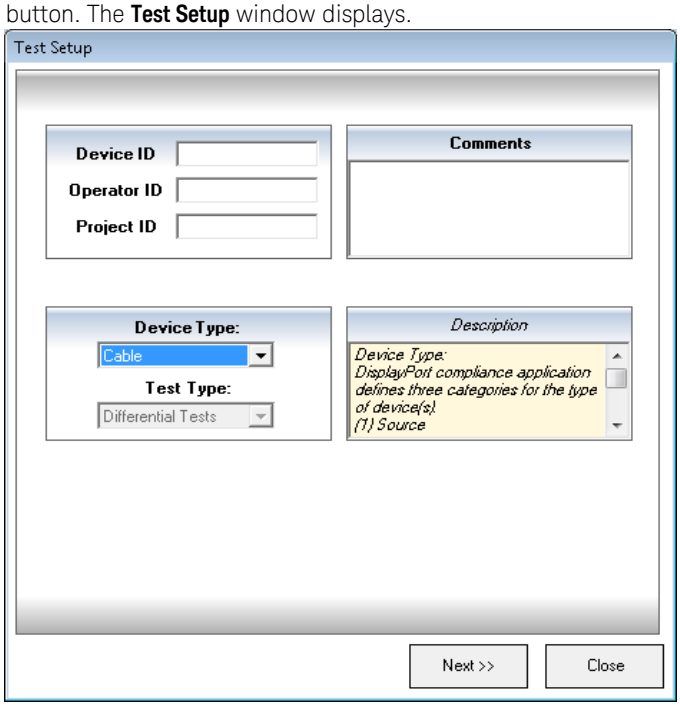
where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Test Conditions for Total Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 163

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



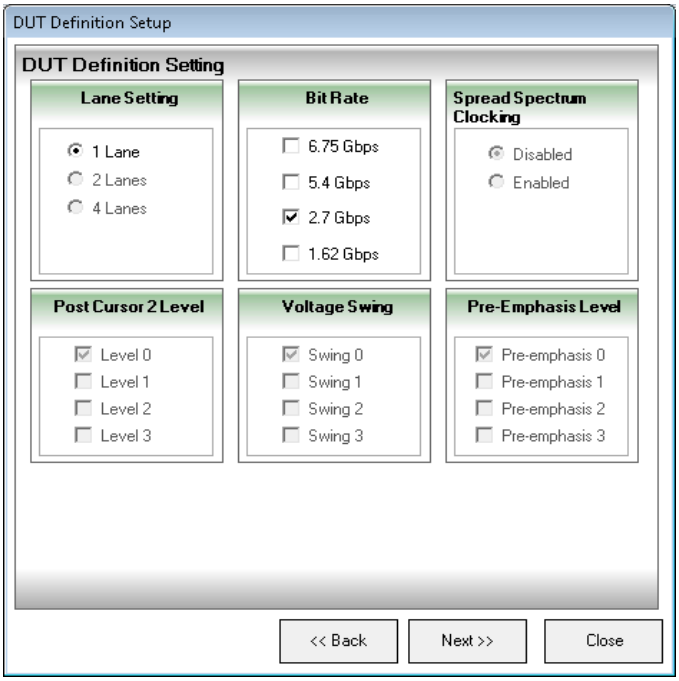
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

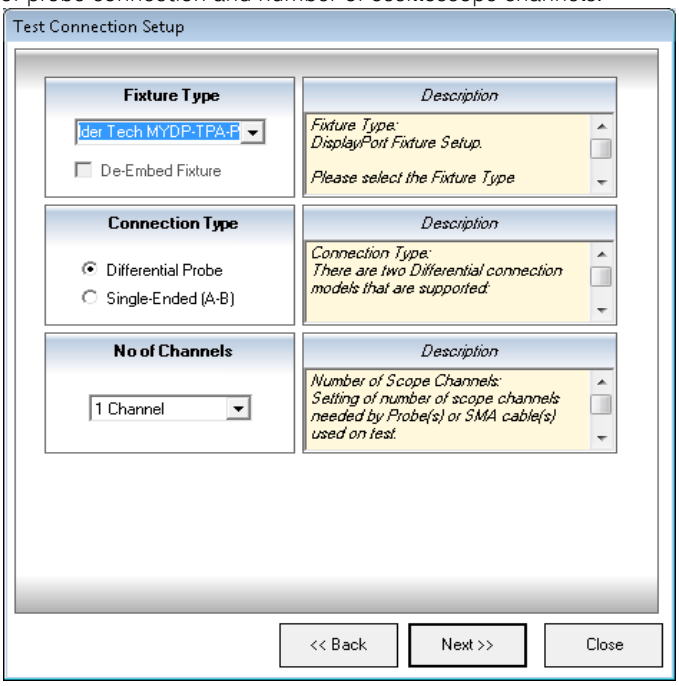
b Select **Device Type:** as **Cable**, **Test Type:** automatically grays out.

c Click **Next**.

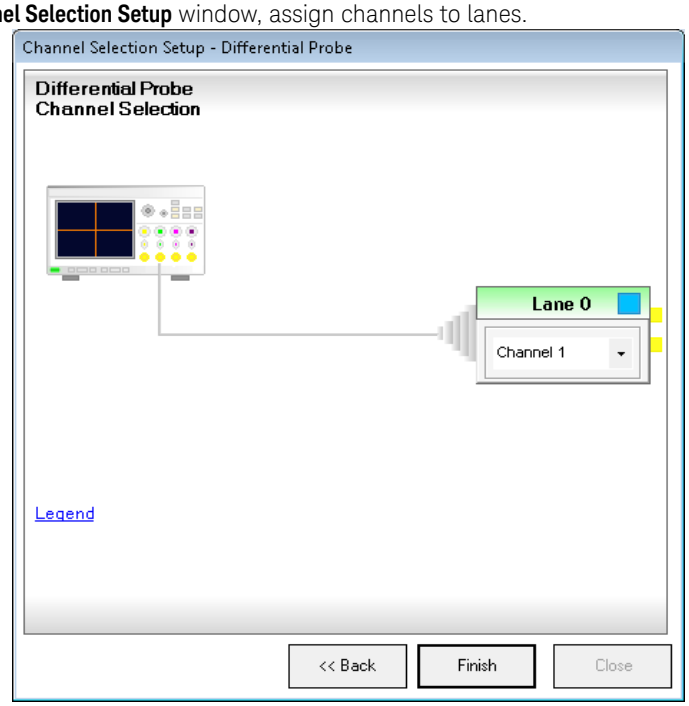
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Total Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

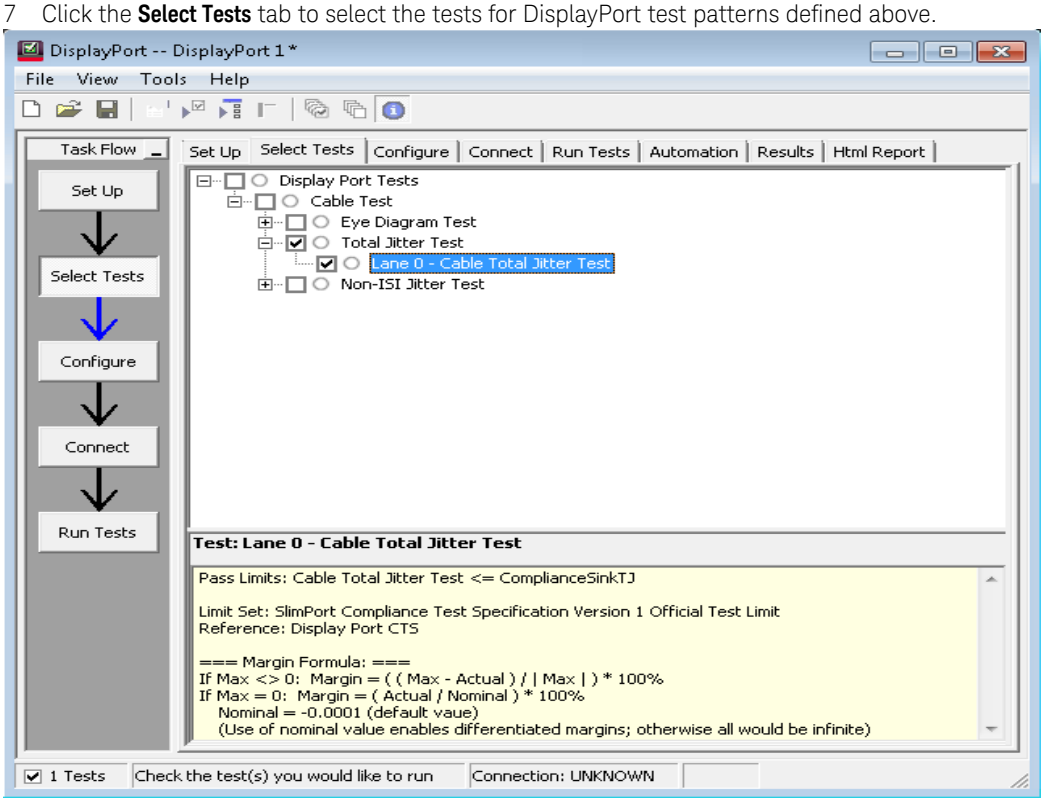


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Cable Tests" on page 852 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 165 Total Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.491 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.750 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured total jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Cable Non-ISI Jitter Test

Test ID

12240001 — Non-ISI Jitter Test

Test Overview

The objective of the test is to evaluate the Non-ISI jitter accompanying the data transmission at either an explicit bit error rate of 10^{-9} or through an approved estimation technique. This measurement is a data time interval error (Data-TIE) jitter measurement.

The jitter is separated into each jitter components and the total jitter is estimated to 10^{-9} BER based on the Dual-Dirac Model:

$$TJ = DJ_{dd} + n^* RJ_{rms}$$

where, DJ is the Deterministic Jitter, RJ is the Random Jitter and n = 12.0 to accommodate 10^{-9} BER.

Calculate Non-ISI Jitter using the following equation:

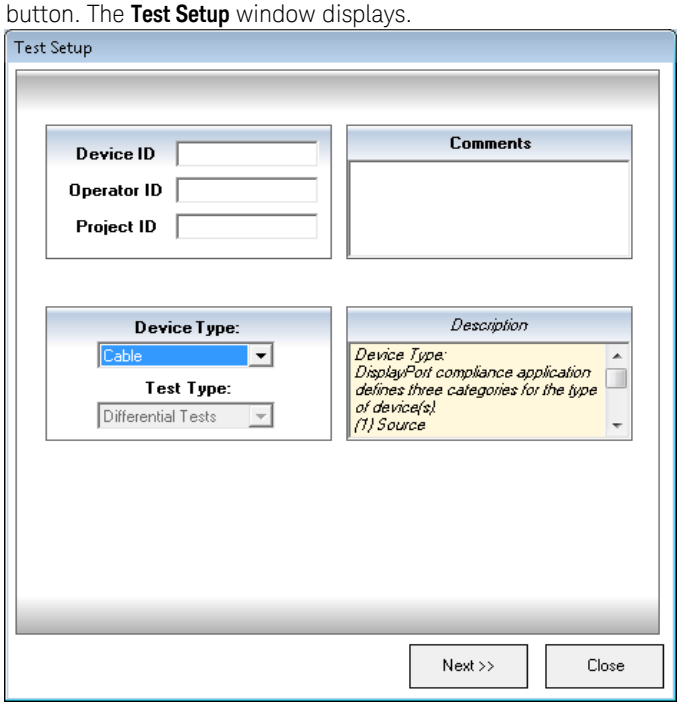
$$\text{Non-ISI Jitter} = TJ - \text{ISI Jitter}$$

Test Conditions for Non-ISI Jitter Test

Test Parameter	Condition
Test Point	RBR–TP3 HBR–TP3_EQ
Bit Rate	RBR, HBR
SSC	SSC Disabled
Voltage Level	Level 0
Pre-Emphasis Level	Level 0
Post-Cursor2 Level	Level 0
Test Lane	Lane 0
Test Pattern	PRBS7
Input Signal Parameter Applied by Stimulus at TP2	Refer to Table 163

Test Setup

1 After you select the options in the **Test Specification** and **Test Selection** area of the **Set Up** tab, click the **Test Setup** button. The **Test Setup** window displays.



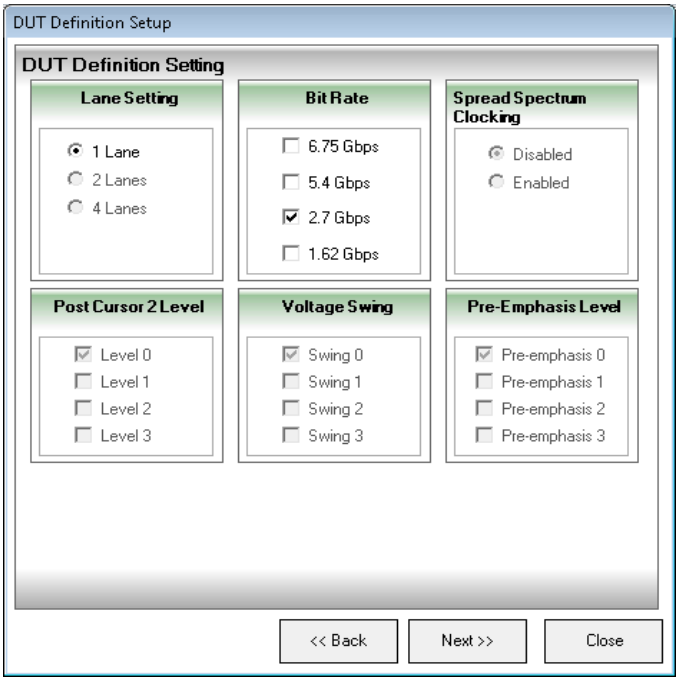
2 On the **Test Setup** window,

a Define your DUT to distinguish between several test runs on the HTML report that the application generates at the end of the test runs.

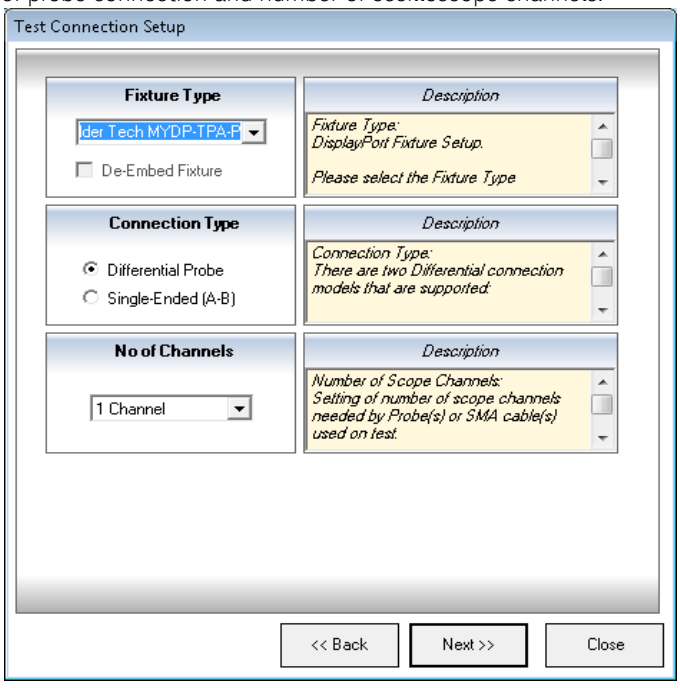
b Select **Device Type:** as **Cable**, **Test Type:** automatically grays out.

c Click **Next**.

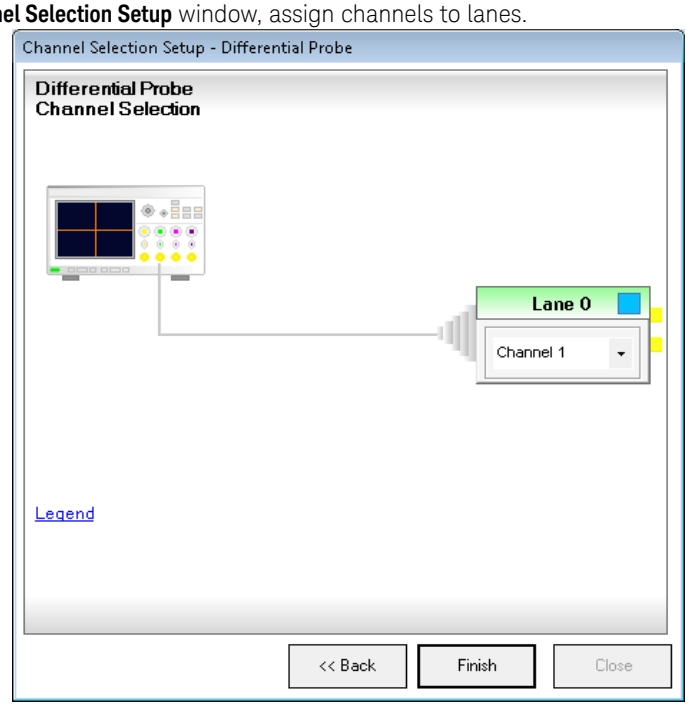
3 On the **DUT Definition Setup** window, select options based on the settings defined in "Test Conditions for Non-ISI Jitter Test".



4 On the **Test Connection Setup** window, select the appropriate fixture type from the drop-down options, type of probe connection and number of oscilloscope channels.

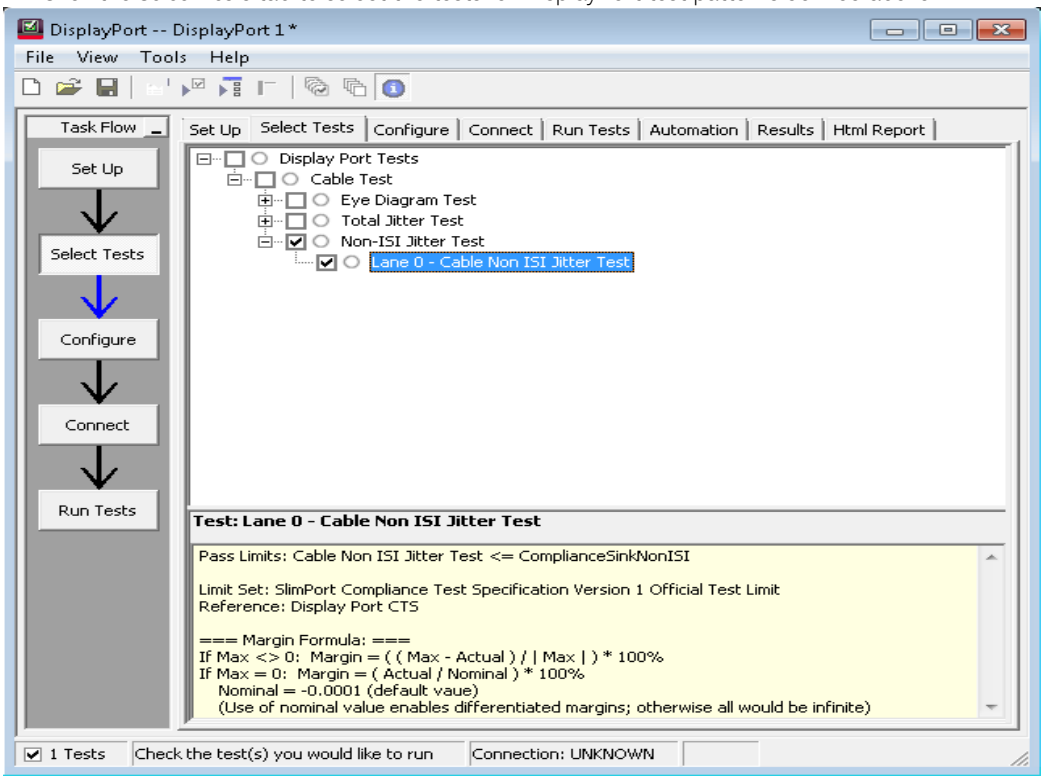


5 On the **Channel Selection Setup** window, assign channels to lanes.



6 Click **Finish**. The **Set Up** tab displays.

7 Click the **Select Tests** tab to select the tests for DisplayPort test patterns defined above.



8 See "Setting Up the DisplayPort Compliance Test Application for SlimPort Cable Tests" on page 852 to complete the task flow for DUT setup along with configuring the Compliance Application to run the test.

Measurement Procedure

1 Ensure that the InfiniiSim is configured based on the settings in the Configuration Variable.
2 Acquire and verify the input signal.
   a Verify the trigger and the amplitude of the input signal.
   b Scale the vertical display of the input signal to the optimum value.
   c Measure V_{TOP} and V_{BASE} of the input signal.
3 Create FUNC3 signal, which is the magnify signal of the input signal.
4 Create FUNC4 signal, which is the equalized signal of the magnify signal. Equalized signal is created by convolving the input signal with the transfer function of the cable model and equalizer based on the settings in the Configuration Variable (Cable Equalizer).
   a Scale the vertical display of the equalized signal to the optimum value.
   b Measure V_{TOP} and V_{BASE} of the equalized signal.
   c Measure the data rate of the equalized signal.
5 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery as described in the section “Clock Recovery”.
6 Set up the parameters for jitter separation using the EZJIT Plus/Complete Software.
   a Load the jitter separation parameter into the EZJIT Plus/Complete software based on the settings in the Configuration Variable.
   b Acquire the signal until 1,000,000 edges are analyzed.
7 Note the jitter component value from the EZJIT Plus/Complete Software.
8 Report the measurement results.

PASS Condition

Table 166 Non ISI Jitter

	Receiver Connector
High-Bit Rate (2.7 Gb/s per lane)	TP3_EQ
A_{p-p}	0.330 UI
Reduced-Bit Rate (1.62 Gb/s per lane)	TP3
A_{p-p}	0.180 UI

UI is Unit Interval.

Test References

See:

- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 9.4*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.5.3.7.2, Table 3-22*

Expected/Observable Results

The measured Non-ISI jitter for the test signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

23 SlimPort AUX Channel Tests

Overview

This section describes the normative and informative AUX Channel physical layer tests and inrush tests for compliance verification of SlimPort source and sink.

Test Point for SlimPort AUX Channel Tests

You must test the Source and Sink/Branch devices at Test Point 2 (TP2). See Figure 171.

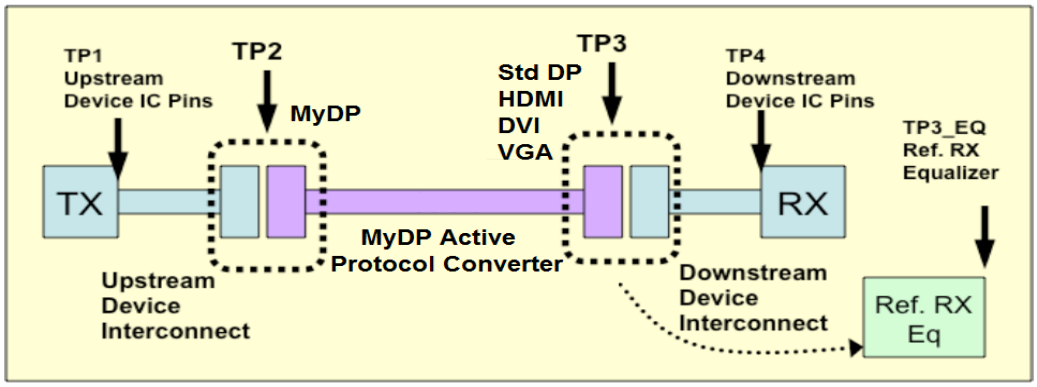


Figure 171 Test Point for SlimPort AUX Channel Tests

Table 167 defines the test point fixtures and instruments used for SlimPort (MyDP HBR25) AUX Channel Tests:

Table 167 Test Point Fixtures and Instruments for SlimPort (MyDP HBR25) AUX Channel Tests

Test Requirement	Device Used
Test Point Access Fixture	Mobility DisplayPort Test Point Adapter For MyDP Connector ▪ Wilder Technologies MYDP-TPA-P* ▪ *Use Wilder Technologies DP-TPA-A AUX Control board for all Wilder Technologies Test Point Adapters.
Signal Analyzer	Infiniium Series Oscilloscope

Setting Up the DisplayPort Compliance Test Application for SlimPort AUX Channel Tests

Perform the following steps before you run the compliance tests on the AUX channel device:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 172).

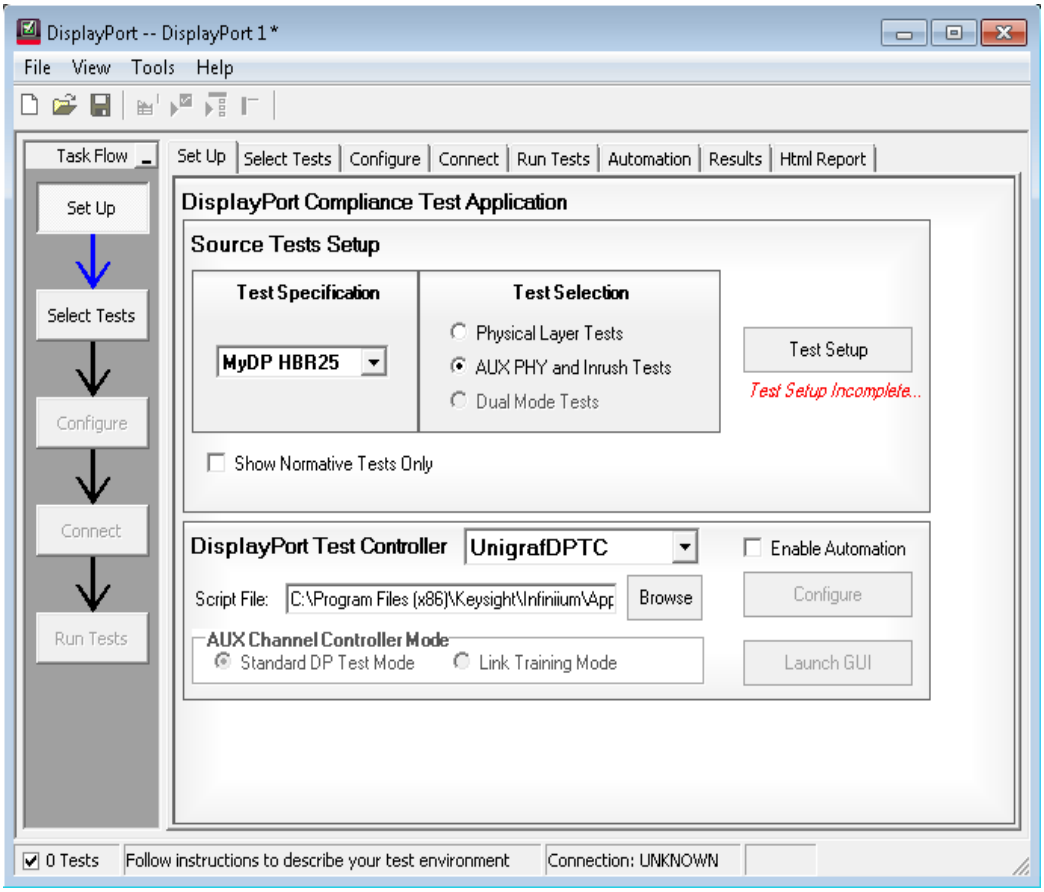


Figure 172 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with SlimPort Standards, select **MyDP HBR25** from the drop-down options in the **Test Specification** area and select **AUX PHY and Inrush Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

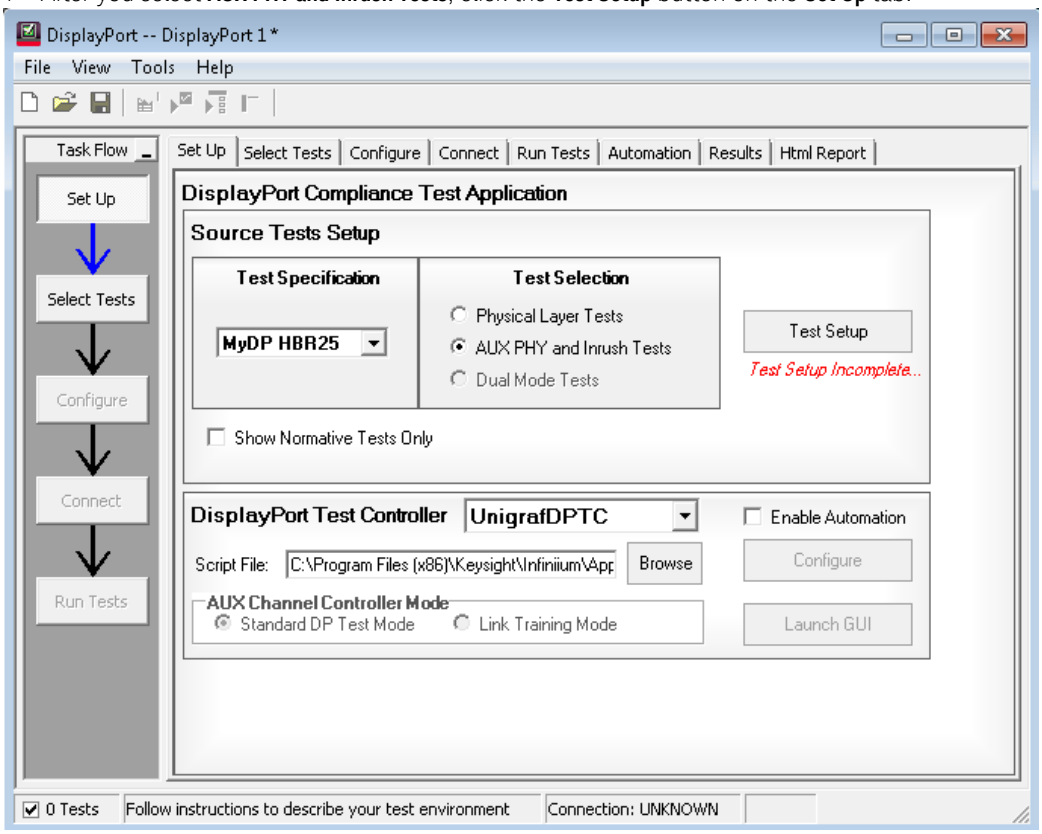
10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

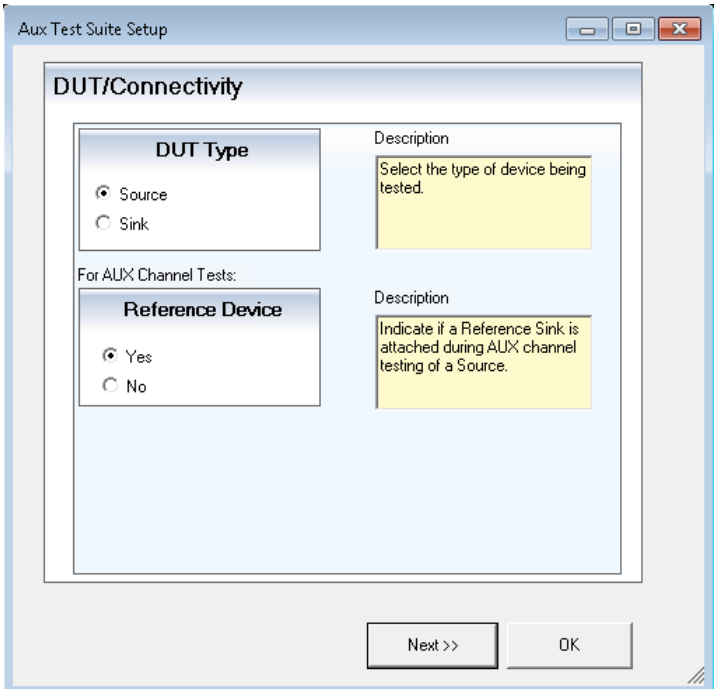
Setting Up for AUX PHY and Inrush Tests

Perform the following steps before you run the Auxiliary Channel and Inrush tests on the source or sink device:

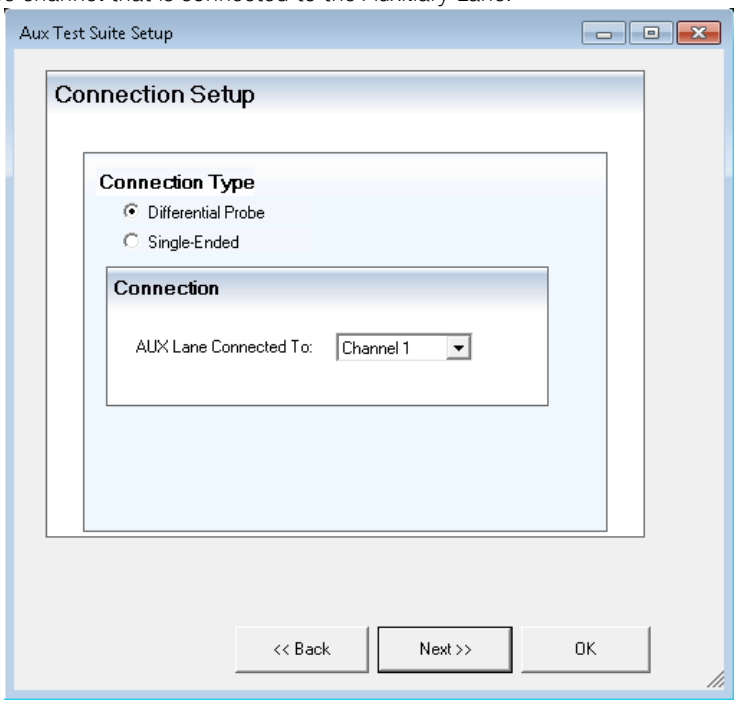
1 After you select **AUX PHY and Inrush Tests**, click the **Test Setup** button on the **Set Up** tab.



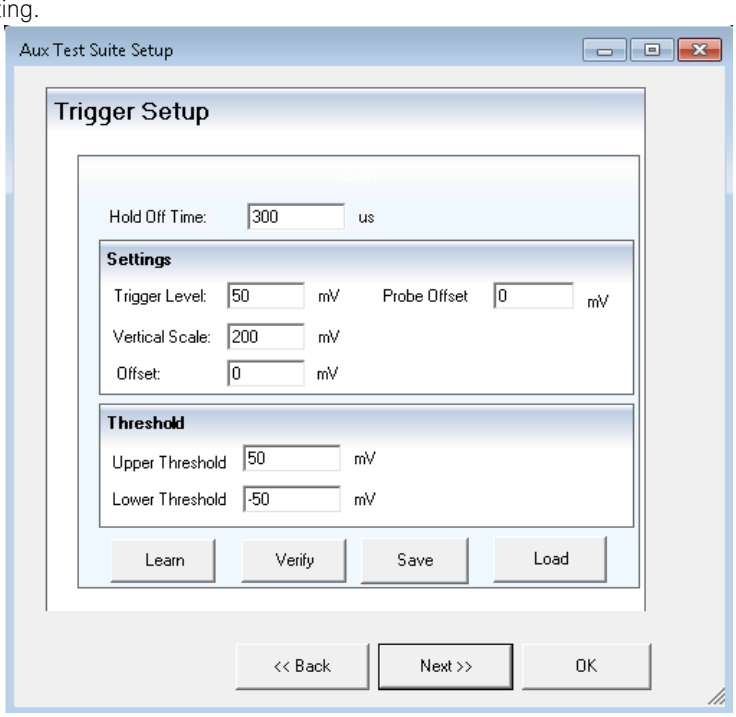
2 On the **DUT/Connectivity** page, select **Source** or **Sink** in the **DUT Type** area. In the **Reference Device** area, select **Yes** if a reference sink/source is attached to device under test during testing. Click **Next**.



3 On the **Connection Setup** page, depending on the probe connection you are using, select either **Differential Probe** or **Single-Ended** in the **Connection Type** area and in the **Connection** area, select the oscilloscope channel that is connected to the Auxiliary Lane.



4 On the **Trigger Setup** page, define the oscilloscope parameters to trigger on an Auxiliary signal during testing.



Hold Off Time – The oscilloscope minimum hold off time before triggering the next waveform. Note that any Auxiliary transaction from the source must receive a reply from the sink in 400 us, else such a transaction is considered a timeout. Hold off time, in such cases, represents the minimum idle time before each AUX transaction is initialized. It is defaulted to 300 us which is a safe timing value for most devices tested in the lab. Most devices respond much faster than 300 us.

Trigger Level – The AUX channel signal level on which to trigger. Note that for a bi-directional signal (where a reference sink is attached), you must set the trigger level such that it crosses both the source command and the sink reply signal. Figure 173 and Figure 174 show correct and incorrect trigger levels.

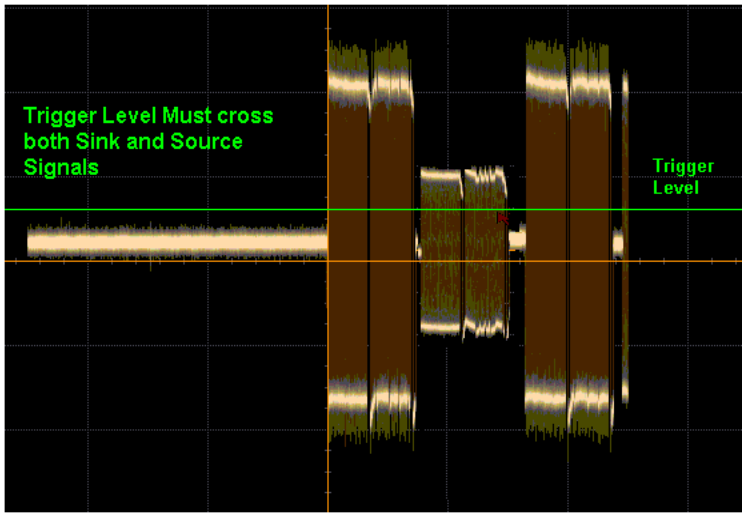


Figure 173 Correct Trigger Level

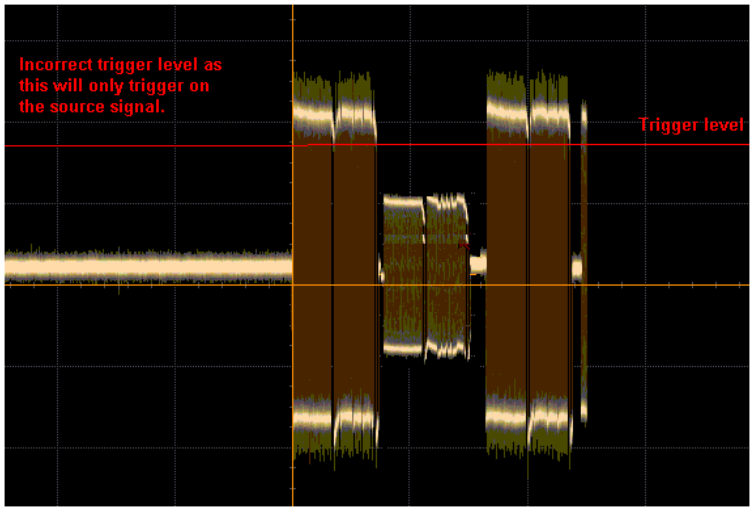


Figure 174 Incorrect Trigger Level

Vertical Scale – The oscilloscope vertical scale. Set the vertical to make sure that all signals are visible on the oscilloscope display.

Offset – Set the offset so that the center point is aligned with the center of the oscilloscope display.

Upper Threshold/Lower Threshold – The threshold level of signal must be set properly so that both upper and lower thresholds cross both the source and sink signals when the DUT is attached with a reference sink. The threshold levels are important parameters because they are used for edge detection when decoding a source command from a sink reply. Figure 175 and Figure 176 show the correct and incorrect threshold sets.

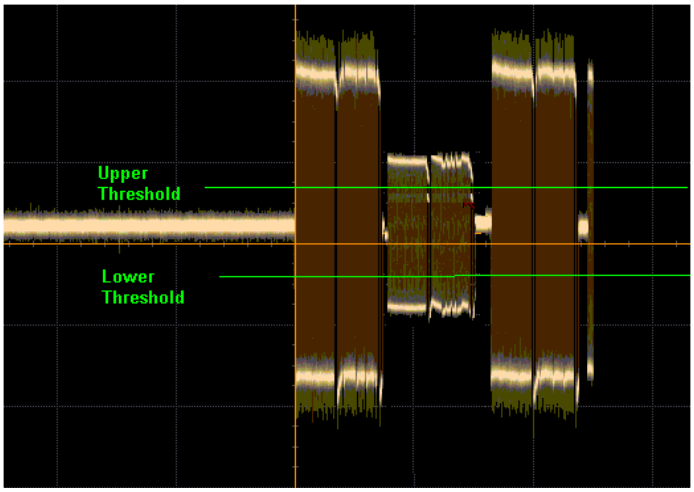


Figure 175 Correct Threshold set

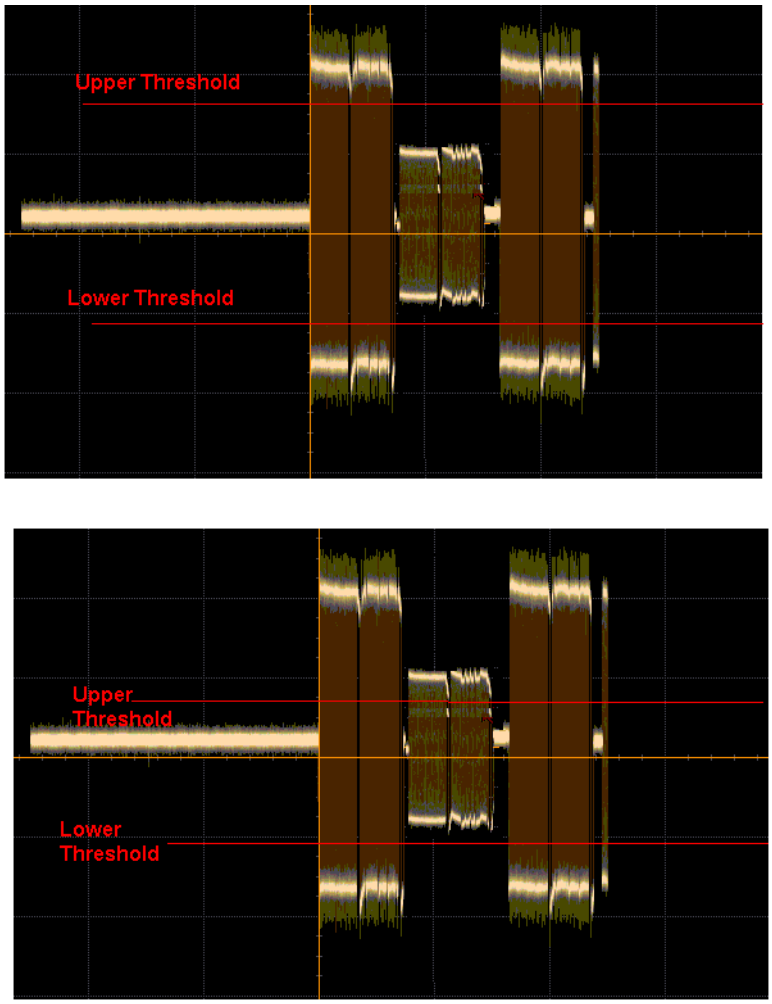


Figure 176 Wrong Thresholds set

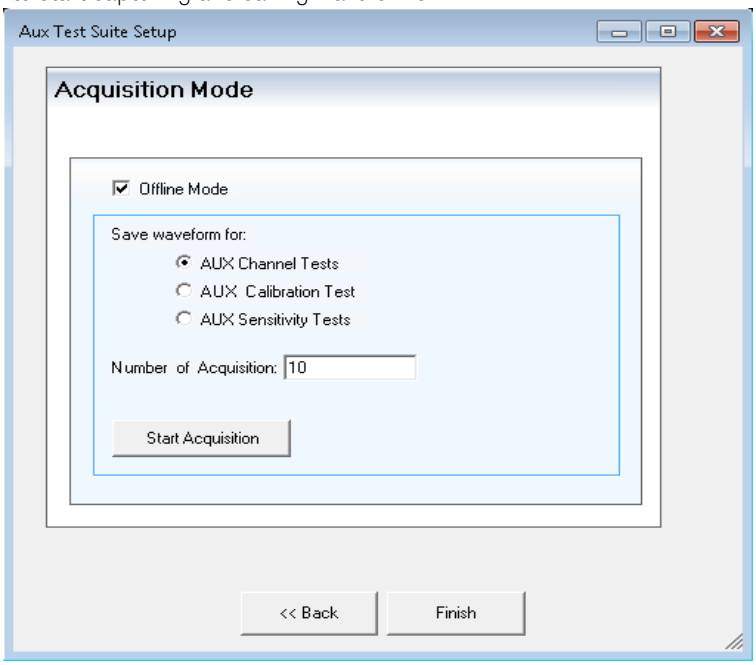
c On the Trigger Setup page, you may click the **Learn** button, which guides you through getting the trigger setup parameters. However, please note that the learning guide may not necessarily work many a times because the actual Auxiliary signals may vary for different manufacturers. Keysight recommends that you must check to make sure that the parameters are correctly set as previously described.

d Click **Verify** and follow the instructions, if you wish to check the AUX Channel trigger.

e You may **Save** or **Load** the trigger setup configuration as a **.tsf* file.

5 On the **Acquisition Mode** page, either **Finish** the setup wizard or enable **Offline Mode**, which is de-selected, by default. Offline Mode lets you save the waveform files so that you can avoid the manual process to initiate Auxiliary transactions during the time of test runs.

6 If you enable **Offline Mode**, define the number of waveforms to be saved. If required, click **Start Acquisition** to start capturing and saving waveforms.



7 Click **Finish** to close the setup wizard. The **Set Up** tab displays.

8 Click the **Select Tests** tab and select the AUX Channel tests you want to run.

Probing/Connection Set Up for AUX Channel Tests

After selecting the tests under the **Select Tests** tab on the DisplayPort Electrical Performance Compliance Test Application, refer to the **Connect** tab to see the connection diagram and instructions required to establish/check the physical connection prior to running the tests. When the tests are running, the DisplayPort Electrical Performance Compliance Test Application may prompt you to make/change the proper connections for certain type of tests. When performing the Source AUX Channel tests, a Reference Sink device is required. Similarly, when performing the Sink AUX Channel tests, a Reference Source device is required.

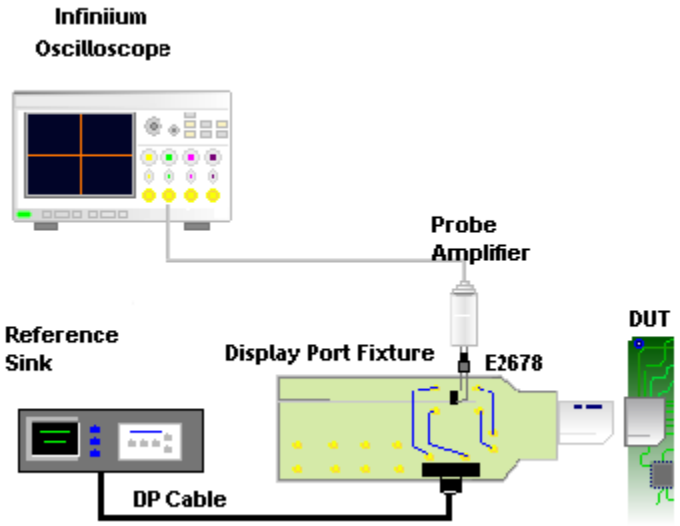


Figure 177 Sample connection diagram for source AUX channel tests with source DUT connected to a reference sink

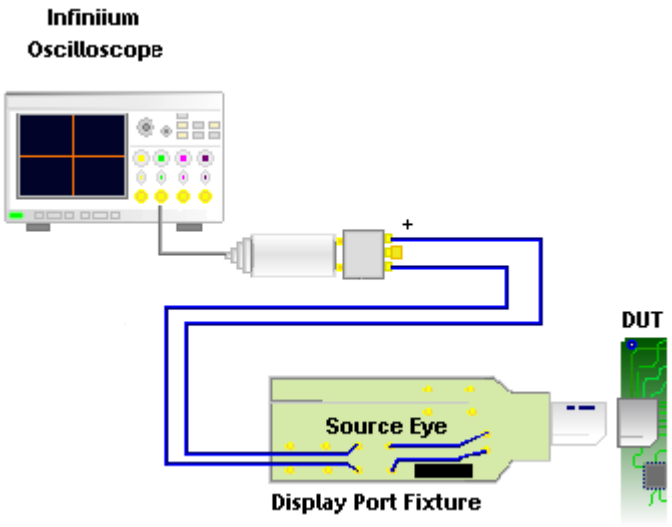


Figure 178 Sample connection diagram for source AUX channel tests without connecting to a reference sink

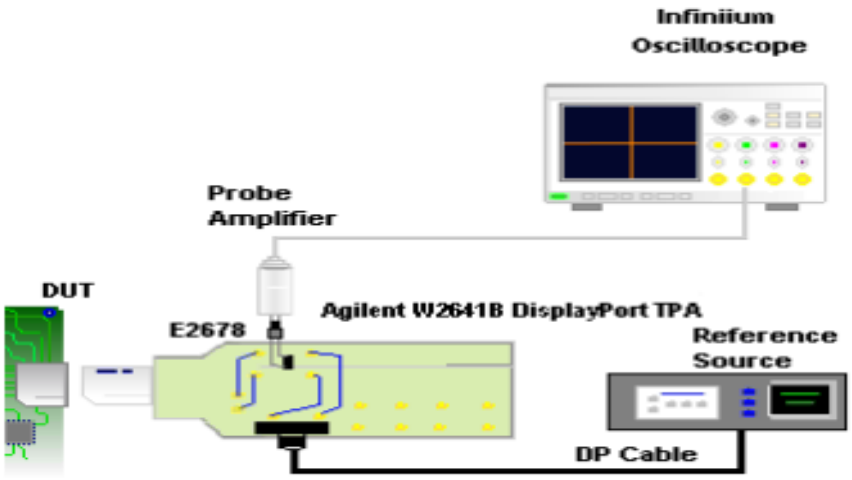


Figure 179 Sample connection diagram for sink AUX channel tests with sink DUT connected to a reference source

AUX Channel Unit Interval Test

Test ID

125000 – AUX Channel Unit Interval Test (Source)

125010 – AUX Channel Unit Interval Test (Sink)

Test Overview

The objective of the test is to evaluate the AUX Channel waveform, ensuring that the overall variation of the Manchester transaction Unit Interval stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Set up the parameter of the measurement trend:

   a Set up the Unit Interval measurement for the differential AUX Channel signal.

   b Set up the frequency measurement for the Clock signal.

   c Set up the measurement trend.

6 Set up the waveform Histogram on the measurement trend:

   a Initialize AUX Channel transactions and acquire the differential AUX Channel signal.

   b Identify the first and the last points for the desired transaction.

   c Zoom-in on the desired transaction.

   d Set up the Vertical Waveform Histogram on the measurement trend within the desired transaction.

   e Obtain the measurement for the mean, maximum and minimum values of the waveform Histogram.

7 Repeat step 6 ten times.

8 Report the measurement results.

PASS Condition

Manchester Transaction Unit Interval (UI_{MAN}):

Minimum = 0.4 µsec

Maximum = 0.6 µsec

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-2*

Expected/Observable Results

The measured unit interval for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Test

Test ID

125001 – AUX Channel Eye Test (Source)

125011 – AUX Channel Eye Test (Sink)

Test Overview

The objective of this test is to evaluate the transmitter AUX Channel waveform, ensuring that the timing variables and amplitude trajectories support the overall DP system objectives of the Bit Error Rate in data transmission.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 Set up the parameters for the Mask Test.

   a Load the eye mask based on the settings in the Configuration Variable.

   b Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

   c Initialize the AUX Channel transaction and run the eye mask until you obtain the required number of waveforms.

9 Check for any signal trajectories entering into the mask.

10 Report the measurement results.

PASS Condition

PASS Value = 290mV_diff_pp or higher

FAIL Value = lower than 290mV_diff_pp

Table 168 Eye Mask Vertices for AUX Channel for Manchester Transactions

Mask Point	Time (from EYE Center)	Minimum Voltage Value at Six Vertices (mV)
1	-185ns	0
2	-135ns	145
3	135ns	145
4	185ns	0
5	135ns	-145
6	-135ns	-145

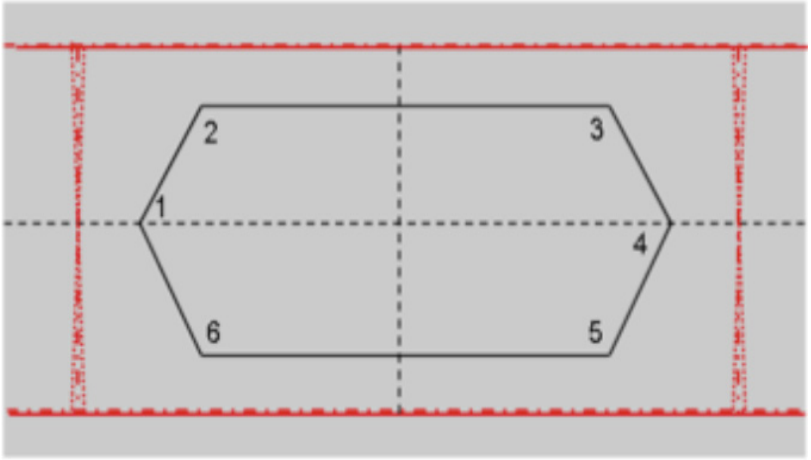


Figure 180 AUX Channel EYE Mask for Manchester Transactions

Mask Test: Zero mask failures.

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.2*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-1 and Table 2-2*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2.6, Figure 3-29 and Table 3-8*

Expected/Observable Results

The measured eye diagram for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test. The rendered eye diagram shall have no signal trajectories entering the mask area.

AUX Channel Peak-to-Peak Voltage Test

Test ID

125002 – AUX Channel Peak-to-Peak Voltage Test (Source)

125012 – AUX Channel Peak-to-Peak Voltage Test (Sink)

Test Overview

The objective of the test is to evaluate the transmitter AUX Channel Waveform, ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

2 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

3 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

4 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

5 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

6 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

7 Set up the horizontal waveform Histogram on the AUX Channel eye diagram to measure the left edge and the right edge.

8 If you have selected the “AUX Channel Eye Test” under the **Select Tests** tab of the compliance application:

   a Set up the parameter of the Mask Test:

      i Load the eye mask based on the settings in the Configuration Variable.

      ii Center the eye mask at the middle of the eye diagram based on the measured left edge and right edge.

      iii Initialize the AUX Channel transaction and run the eye mask until ten waveforms are folded.

   b Check for any signal trajectories entering into the mask.

9 Set up the waveform histogram on the AUX Channel eye diagram.

a Set up the vertical waveform histogram on the AUX Channel eye diagram to measure the peak to peak voltage.

10 Report the measurement results.

PASS Condition

Table 169 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage at a transmitting device ($V_{AUX\text{-}DIFFp\text{-}p}$)	0.29V	1.38V

Test References

See:

- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 2, Table 2-1*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the transmitter AUX Channel signal shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Calibration Test

Test ID

125021 – AUX Channel Eye Sensitivity Calibration (Reference Sink)

125031 – AUX Channel Eye Sensitivity Calibration (Reference Source)

Test Overview

The objective of this test is to calibrate the peak-to-peak voltage of the transmitter AUX Channel waveform by reference device (reference source or reference sink), ensuring that the peak-to-peak voltage stays within the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.

2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.

3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.

4 Generate FUNC2 (Clock) signal for the eye folding using the MATLAB script. The MATLAB script generates the clock for the desired transaction (either Source transaction or Sink transaction based on the type of DUT).

5 Set up the parameter of the measurement:

   a Enable measurement of all edges to obtain a statistical value of the measurement.

   b Set up the measurement threshold.

   c Set up the Clock Recovery.

6 Generate FUNC3 signal, which is the second differential signal of the AUX Channel.

7 Fold the differential signals of the AUX Channel to generate the eye diagram at the middle of the screen such that it is more than one full UI but no more than 2.5 UI.

8 Set up the waveform Histogram on the AUX Channel eye diagram:

   a Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.

   b Set up the vertical waveform Histogram of width 0.6 UI at the center of the AUX Channel eye diagram.

   c Measure the V_{TOP} and V_{BASE} using the waveform Histogram mean value.

9 Repeat Step 8 three times.

10 Report the measurement results.

PASS Condition

Table 170 DisplayPort AUX Channel Peak-to-Peak Voltage

Parameter	Min	Max
AUX Peak-to-Peak voltage for AUX Channel Eye Sensitivity	0.24V	0.28V

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.2*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured peak-to-peak voltage for the AUX Channel signal by reference device (reference source or reference sink) shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

AUX Channel Eye Sensitivity Test

Test ID

125041 – AUX Channel Eye Sensitivity Test (Source)

125051 – AUX Channel Eye Sensitivity Test (Sink)

Test Overview

The objective of the test is to evaluate the sensitivity to the AUX Channel Eye Opening of the DUT as per the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2
Stimulus	Source–Unigraf DPR-100 Compact Sized DisplayPort Reference Sink Sink–Unigraf DPT-200 Compact Sized DisplayPort Reference Source

Measurement Procedure

1 Set up the AUX Channel voltage level of the reference device (reference source or reference sink) to the desired settings based on the settings in the Configuration Variable.
2 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the **Trigger Setup**.
3 Generate FUNC1 signal, which is the first differential signal of the AUX Channel.
4 Set up the parameter of the measurement:
   a Enable measurement of all edges to obtain a statistical value of the measurement.
   b Set up the measurement threshold.
   c Set up the Clock Recovery.
5 Initialize the AUX Channel transaction and acquire the differential AUX Channel signal.
6 Check if the reference device could detect the transaction or not.
7 Decode the AUX Channel signal and check whether the transaction passed or failed.
8 Report the measurement results.

PASS Condition

Determine whether the AUX Channel communication is successful. For example, the Transmitter DUT sends an AUX Request to the Reference Receiver. The Reference Receiver acknowledges and the Transmitter DUT responds to the to indicate that the acknowledgment was successfully received.

PASS = No errors observed in the response

FAIL = One or more errors observed

Test References

See:

- *SlimPort Compliance Test Specification Version 1, Section 2.2*
- *VESA DisplayPort PHY Compliance Test Specification Version 1.2b, Section 8.2*
- *VESA DisplayPort Standard Version 1, Revision 2a, Section 3.4.2, Table 3-6*

Expected/Observable Results

The measured AUX Channel transaction shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

24 SlimPort Inrush Tests

Overview

This section describes the normative and informative inrush tests for compliance verification of SlimPort source and sink, which is a power consumer.

Test Point

The test fixture for inrush tests implements the schematic shown in Figure 181.

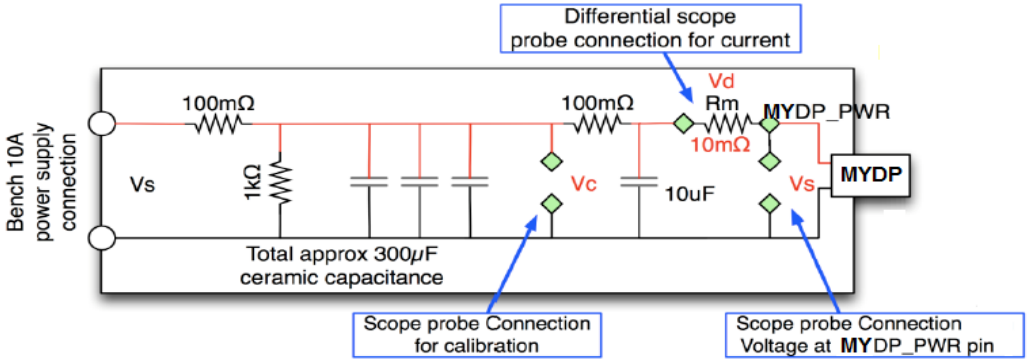


Figure 181 Schematics for testing a Power Consumer Device

The test fixture must be designed and used according to the following guidelines:

- A high gate voltage FET on the MyDP_PWR line is recommended to allow a fast connect capability, which allows a single connection event for testing. Without such an arrangement, multiple connections will be required to obtain a reasonable “worst-case” attachment event.
- Connection length between the power supply and the test fixture must be minimized. A maximum of four inches is recommended.
- The power supply must have enough outrush capability as to not negatively affect the test fixture’s outrush capability.
- The power supply must be run at 5.5V (5.0V + 10%) read across V_C.

Any Power Consumer test fixture must be calibrated using the Power User test fixture, as shown in Figure. Testing with the two fixtures combined should result in the approximate values given below. If required, the component values on the Power Consumer test fixture should be adjusted to match the expected results.

For Source:

- V_C steady before connection = 5.5V
- Inrush Current = ~9.0A

For Sink:

- V_C steady before connection = 3.6V
- Inrush Current = ~13.0A

Setting Up the DisplayPort Compliance Test Application for SlimPort Inrush Tests

Perform the following steps before you run the compliance tests on the DUT:

1 Connect the appropriate test fixture to the device under test (DUT).

2 Start the automated testing application as described in "Starting the DisplayPort Electrical Performance Compliance Test Application" on page 53.

3 On the DisplayPort Compliance Test Application, click the **Set Up** tab (see Figure 182).

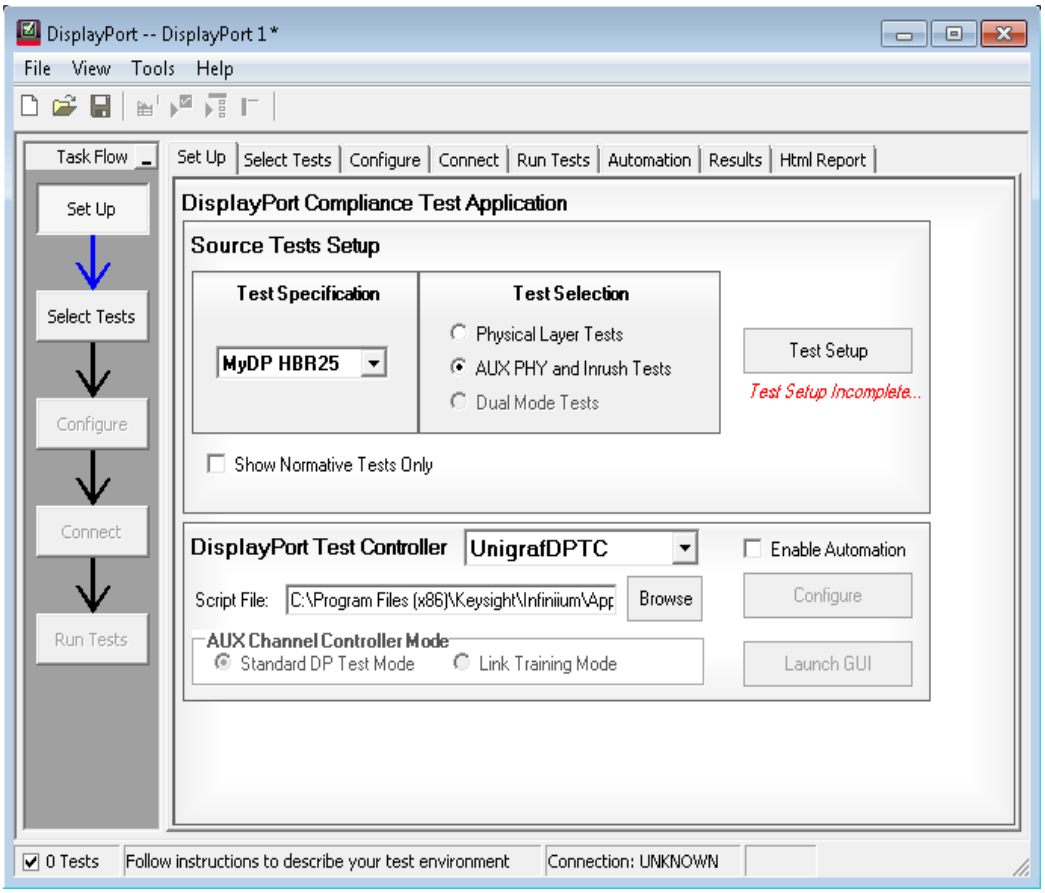


Figure 182 Set Up tab on the DisplayPort Compliance Test App

4 To test for compliance with SlimPort Standards, select **MyDP HBR25** from the drop-down options in the **Test Specification** area and select **AUX PHY and Inrush Tests** in the **Test Selection** area.

5 De-select **Show Normative Tests Only**, if you want to run Informative Tests also. By default, this check-box is selected.

6 Click the **Test Setup** button. The **Test Setup** wizard displays. Define the DUT parameters, connection type and various settings required to run the tests. Refer to "Setting Up for AUX PHY and Inrush Tests" on page 875 to know in detail how to set up the DUT for Inrush Tests.

7 After making the required changes under the **Set Up** tab, click the **Select Tests** tab to select a test or a group of tests that you wish to run. Note that the tests displayed under this tab are dependent on the parameters defined in the **Set Up** tab and the **Test Setup** dialog.

8 Once you select the tests under the **Select Tests** tab, the automated application automatically optimizes the configuration options under the **Configure** tab. However, you may manually make changes to one or more parameters, if required, for test runs under **Compliance** Mode or **Debug** mode.

9 Click the **Connect** tab to see the connection diagram for the selected tests along with the instructions to establish the physical connection. During test runs, the automated application may prompt you for changes in the connection/physical setup, if required.

10 Run the selected tests and view the test results under the **Results** tab once all test runs are complete.

Refer to the Keysight U7232D DisplayPort Compliance Test Application's Online Help for detailed description on the working and functionality of each of the features/tabs on the Compliance Test Application.

Inrush Energy Power Test

Test ID

127000 – Inrush Energy Power Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush energy power measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Current $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 9$ Amps

Test References

See:

For Source:

- *SlimPort Compliance Test Specification Version 1, Section 2.3*
- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.5*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

For Sink:

- *SlimPort Compliance Test Specification Version 1, Section 5.2*
- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 3.4*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

Expected/Observable Results

The measured worst case inrush energy power for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

Inrush Peak Current Test

Test ID

127001 — Inrush Peak Current Test

Test Overview

The objective of the test is to evaluate the Inrush energy at the power supply input of a power consuming DUT according to the specification limits.

Test Conditions

Test Parameter	Condition
Test Point	TP2

Measurement Procedure

1 Configure the Acquisition Setup and the Vertical Scale of the input signal based on the settings in the Configuration Variable.

2 Generate FUNC1 signal (filtered V_d) by applying the low-pass filter on the V_d signal.

3 Generate FUNC2 signal (Current) by applying the following equation:

$$\text{Current } (I_d) = V_d/R_m$$

4 Generate FUNC3 signal (Power) by applying the following equation:

$$\text{Power } (P_s) = I_d * V_s$$

5 Set up the trigger level of V_d signal and acquire the input signal.

6 Identify the first and the last points where the filtered V_d signal crosses the crossing point.

7 Calculate the Inrush Energy Power by summing the area under the power (FUNC3 signal) from the first point to the last point where the filtered V_d signal crosses the crossing point.

8 Calculate the Inrush peak current using the following equation:

$$\text{Inrush Peak Current } (I_{d\_Peak}) = V_{d\_Peak}/R_m$$

where, V_{d_Peak} is the peak voltage on the V_d signal from the first point to the last point where the filtered V_d signal crosses the crossing point (06A * R_m).

9 Repeat step 5 to 8 ten times to find the worst case (maximum) of inrush energy power and inrush peak current.

10 Report the inrush peak current measurement results.

PASS Condition

Power Consumer Requirements:

- Evaluated Inrush Energy (mJ) $\text{Resultant}_{ENERGY\_Power\_Consumer} < 0.4\text{mJ}$
- Evaluated Inrush Current $\text{Resultant}_{PEAK\_CURRENT\_Power\_Consumer} \leq 9$ Amps

Test References

See:

For Source:

- *SlimPort Compliance Test Specification Version 1, Section 2.3*
- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 2.5*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

For Sink:

- *SlimPort Compliance Test Specification Version 1, Section 5.2*
- *VESA Mobility DisplayPort (MyDP) Compliance Test Specification Version 1.0, Section 3.4*
- *VESA Mobility DisplayPort (MyDP) Standard Version 1, Section 6*

Expected/Observable Results

The measured worst case inrush peak current for the power consuming DUT shall be within the conformance limits as specified in the specification mentioned under the “PASS Condition” section for this test.

25 Calibrating the Infiniium Oscilloscope

This section describes the Keysight Infiniium Oscilloscopes calibration procedures.

To Run the Self Calibration

NOTE **Let the Oscilloscope warm up before adjusting. Warm up the Oscilloscope for 30 minutes before starting calibration procedure. Failure to allow warm up may result in inaccurate calibration.**

The self calibration uses signals generated in the Oscilloscope to calibrate Channel sensitivity, offsets, and trigger parameters. You should run the self calibration

- yearly or according to your periodic needs,
- when you replace the acquisition assembly or acquisition hybrids,
- when you replace the hard drive or any other assembly,
- when the oscilloscope's operating temperature (after the 30 minute warm-up period) is more than ±5 °C different from that of the last calibration.

Before you begin calibrating the Infiniium Oscilloscope in preparation for running the DisplayPort automated tests, you need the equipments described in the section Other Equipment (required for Internal/Self Calibration of the Infiniium Oscilloscope) of the "Required Equipment and Software" on page 3.

Internal or Self Calibration

NOTE Calibration time: It takes approximately 1 hour to run the self calibration on the Oscilloscope, including the time required to change cables from Channel to Channel.

1 Let the Oscilloscope warm up before running the Self Calibration.

Perform self calibration only after the oscilloscope has run for 30 minutes at ambient temperature with the cover installed. Calibration of an Oscilloscope that has not warmed up may result in an inaccurate calibration.

2 From the Infiniium Oscilloscope's main menu, click **Utilities>Calibration...**.

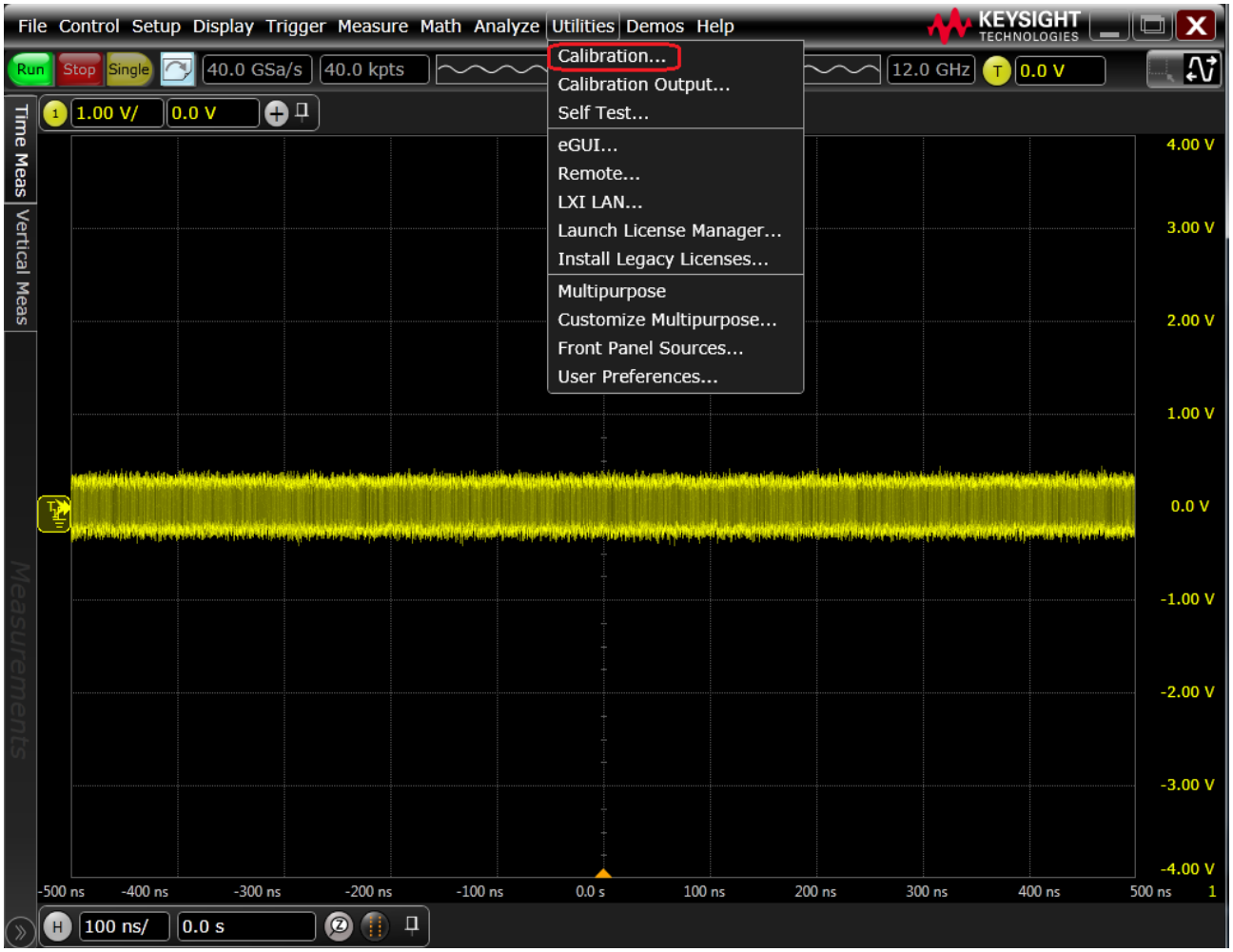


Figure 183 Accessing Calibration dialog on the Oscilloscope

The **Calibration** dialog appears.

3 To start the calibration process:

a Clear the **Cal Memory Protect** checkbox.

You cannot run self calibration if this box is checked. See Figure 184.

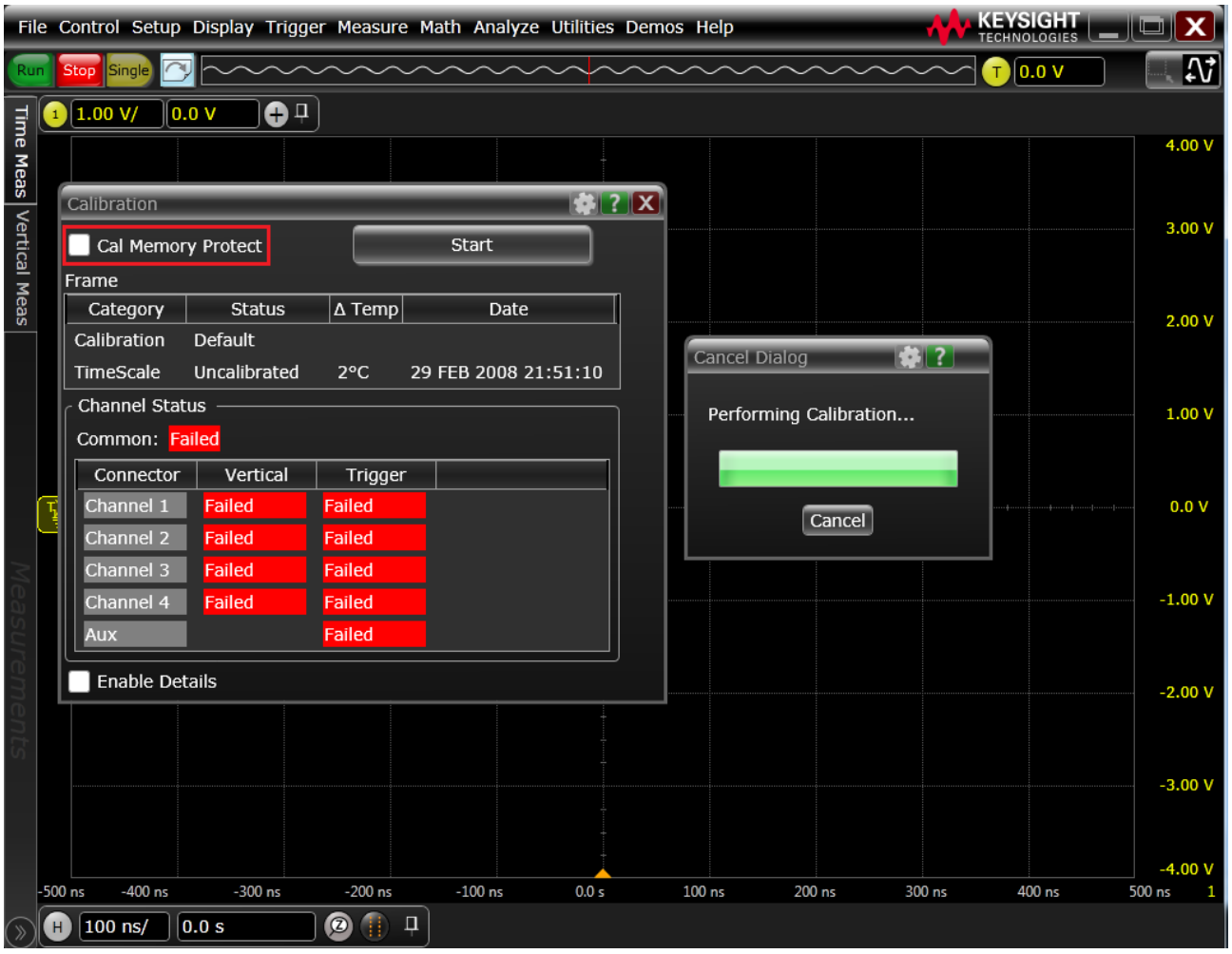


Figure 184 Clearing **Cal Memory Protect** and Starting Calibration

b Click **Start** to begin calibration.

c Follow the on-screen instructions.

d During the calibration of any Oscilloscope Channel, if the oscilloscope prompts you to perform a Time Scale Calibration, select **Standard Cal and Default Time Scale** in the **Calibration Options** dialog.

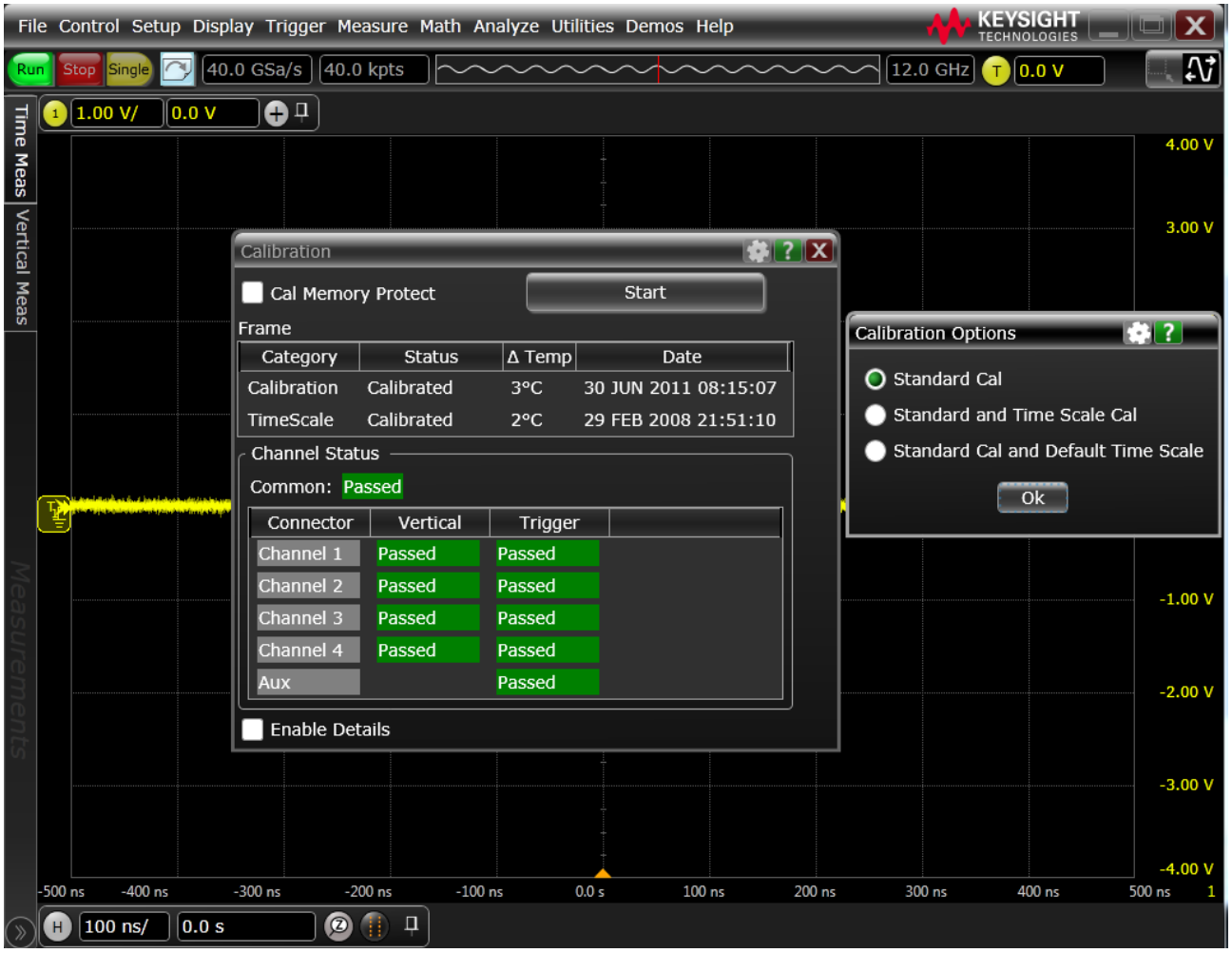


Figure 185 Selecting options from the **Calibration Options** dialog

The options under the **Calibration Options** dialog are:

- **Standard Calibration**—Oscilloscope does not perform time scale calibration and uses calibration factors from the previous time scale calibration and the reference signal is not required. The rest of the calibration procedure continues.
- **Standard and Time Scale Cal**—Oscilloscope performs time scale calibration. You must connect a reference signal to the Oscilloscope Channel, after ensuring that the reference signal meets the following specifications. Failure to meet these specifications result in an inaccurate calibration.

- **Standard Cal and Default Time Scale**—Oscilloscope uses the default time scale calibration factors and does not require the 10 MHz reference signal. The rest of the calibration procedure continues.

e Disconnect everything from all inputs and AUX Out.

f Connect the calibration cable from AUX Out to a specific Channel.

g Connect the calibration cable from AUX Out to each of the Channel inputs as requested.

h Connect the 50 **Ω** BNC cable from the AUX Out to the AUX Trig on the front panel of the Oscilloscope.

i A Passed/Failed indication is displayed for each calibration section. If any section fails, check the calibration cables and run the Oscilloscope **Self Test...** in the **Utilities...** menu.

j After the calibration procedure is completed, click **Close**.

Probe Calibration and De-skew

Along with calibrating the Infiniium Oscilloscope, it is a good practice to calibrate and de-skew the probes, before you start running the automated tests.

Differential SMA Probe Head Attenuation/Offset Calibration

Perform the following steps

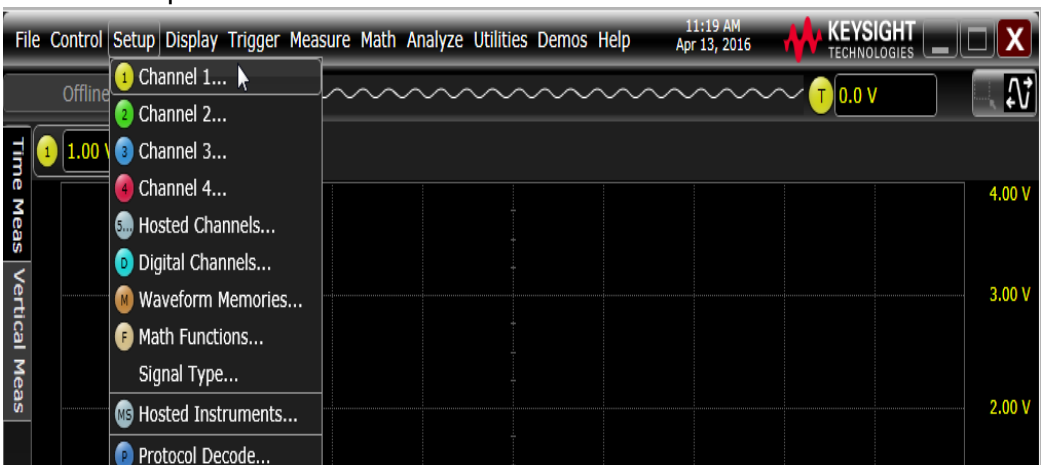
1 Connect a shorting cap to the center SMA connector of the Differential SMA Probe Head.

2 Connect the BNC connector of the SMA to BNC adapter to AUX Out on the front panel of the Infiniium Oscilloscope.

3 Using the Differential SMA Probe Head, connect the Oscilloscope's AUX Out to the positive (+) side of InfiniiMax Probe Amplifier. Keep the negative (-) side of the InfiniiMax Probe Amplifier open.

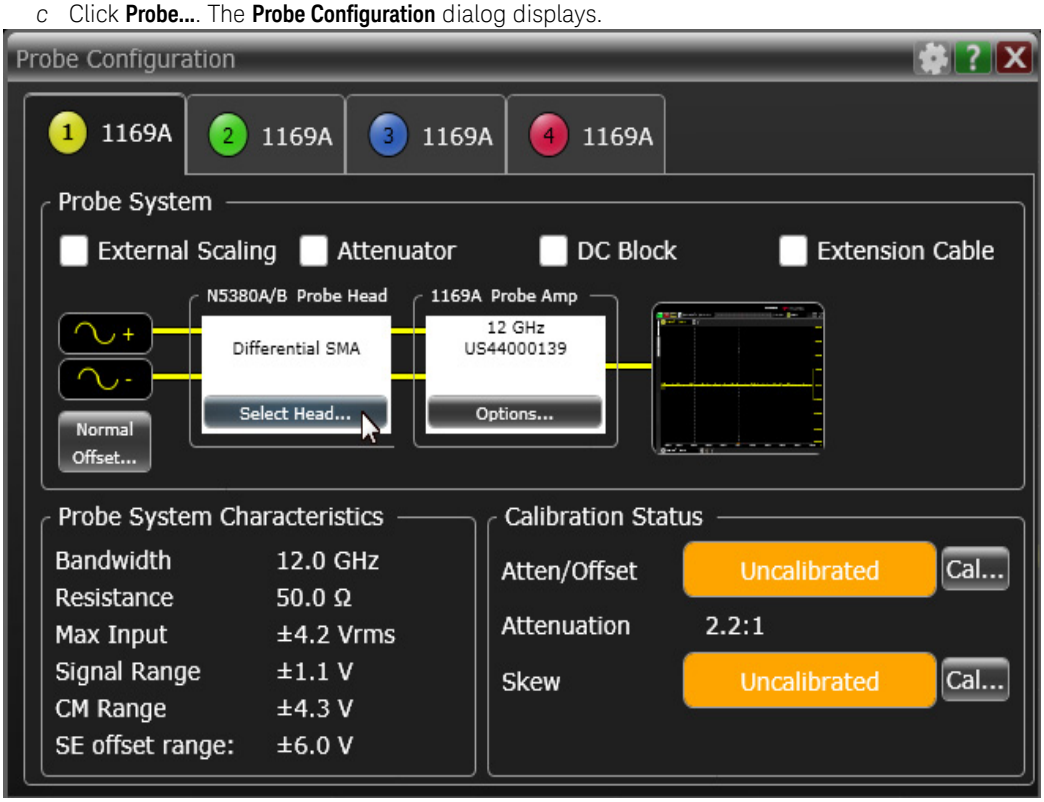
4 On the Infiniium Oscilloscope,

a Click **Setup>Channel 1...**.



b The **Channel** dialog displays to set up Channel 1 of the Oscilloscope.

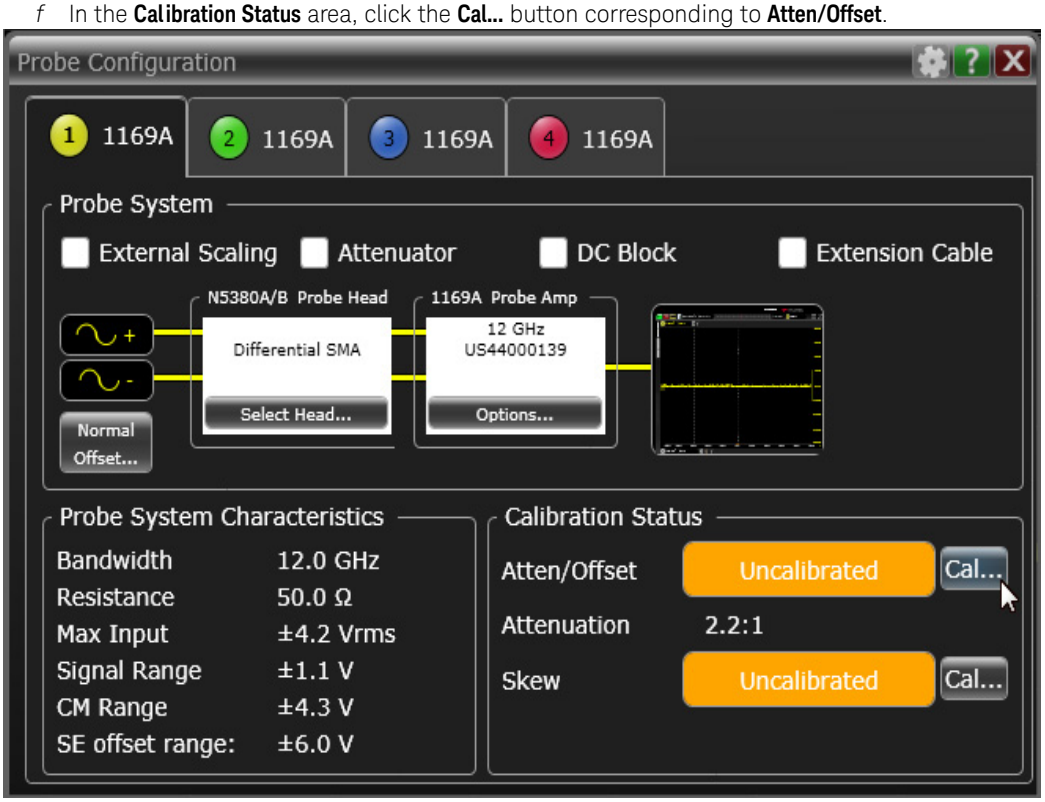
c Click **Probe...**. The **Probe Configuration** dialog displays.



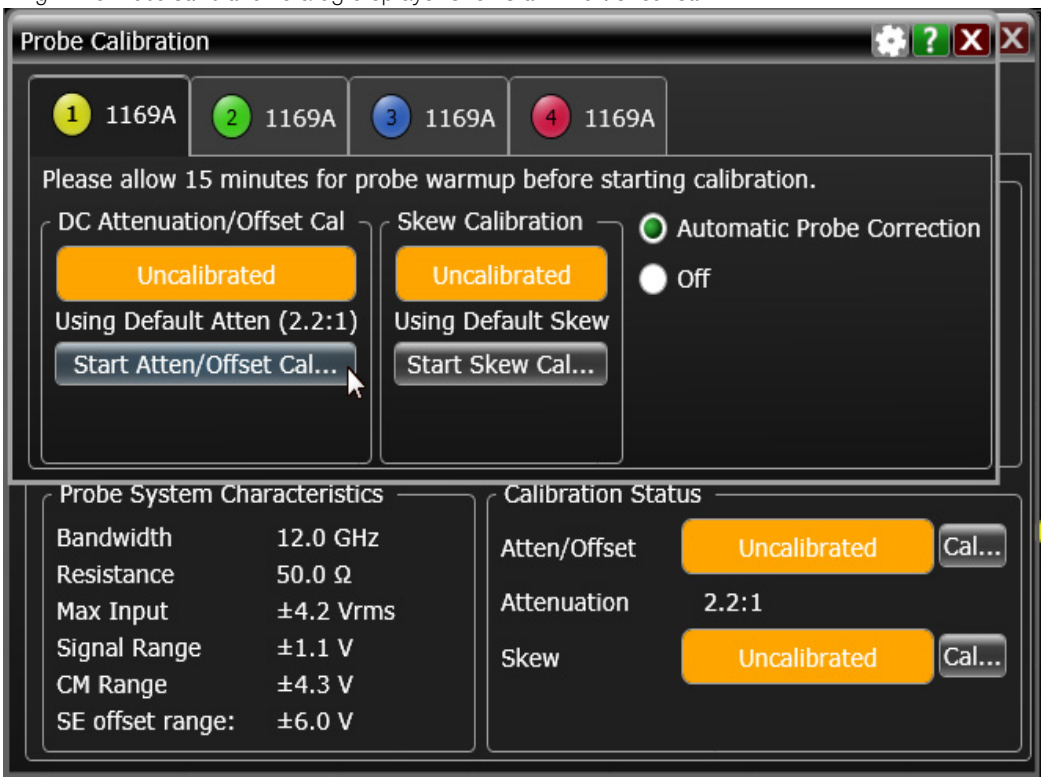
d In the **Probe Head** block, click the **Select Head...** button.

e Select **N5380A/B** from the list.

f In the **Calibration Status** area, click the **Cal...** button corresponding to **Atten/Offset**.



g The **Probe Calibration** dialog displays. Click **Start Atten/Offset Cal...**.



h The Calibration wizard displays. Follow the on-screen instructions. At the end of the Atten/Offset Calibration, perform the Skew Calibration for the Differential SMA Probe Head.

Differential SMA Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. After the Atten/Offset Calibration is done, perform the following steps for skew calibration:

1 On the **Probe Calibration** dialog, click **Start Skew Cal...**.

2 The Calibration wizard displays. Follow the on-screen instructions.

Differential Socketed Probe Head Atten/Offset Calibration

Perform the following steps

1 Ensure that an InfiniiMax Probe Amplifier, attached to a Differential Socketed Probe Head is connected to Channel 1 of the Oscilloscope.

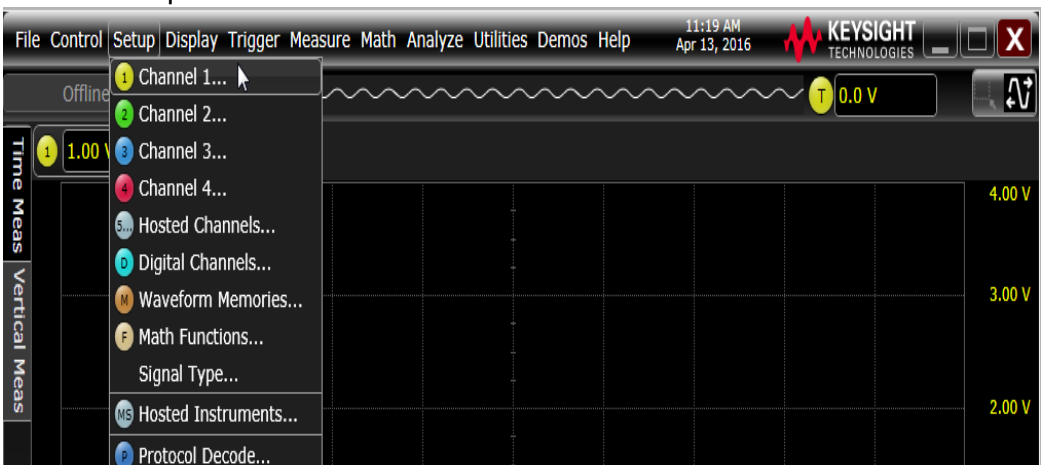
2 Install the 80 Ω resistors into the Differential Socketed Probe Head. These resistors are required only for probe calibration and de-skew.

3 Connect the De-Skew fixture to AUX Out on the front panel of the Infiniium Oscilloscope.

4 Clip the resistors on the De-Skew fixture.

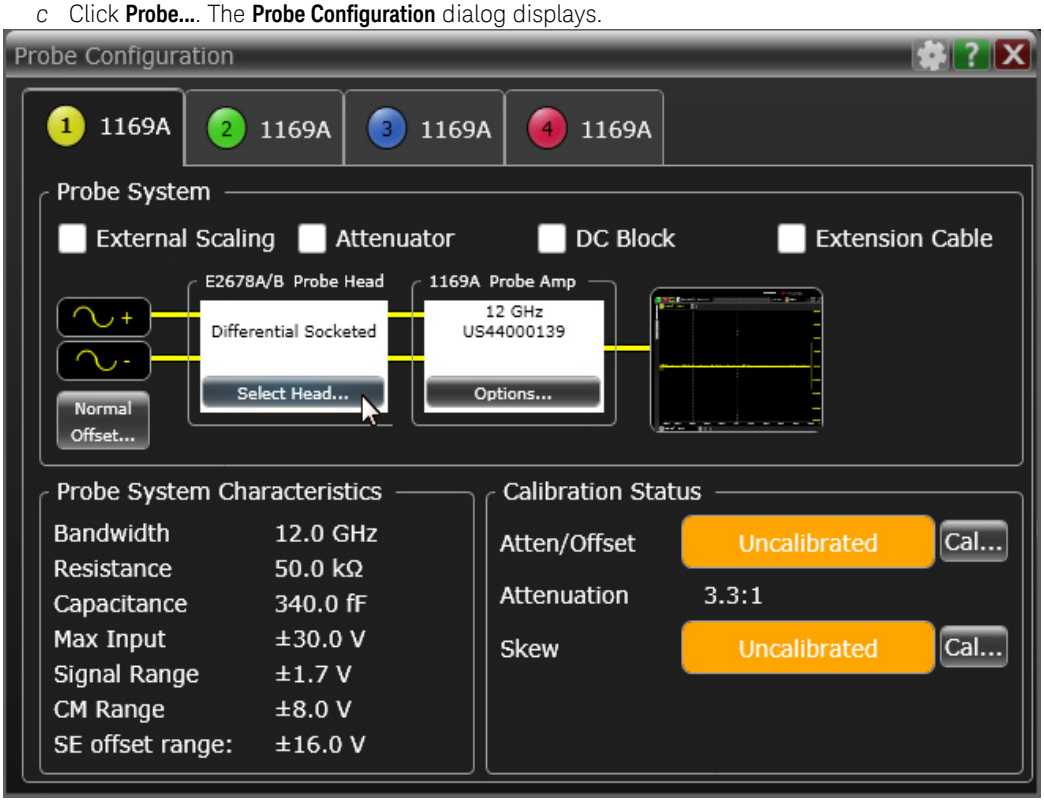
5 On the Infiniium Oscilloscope,

a Click **Setup>Channel 1...**.



b The **Channel** dialog displays to set up Channel 1 of the Oscilloscope.

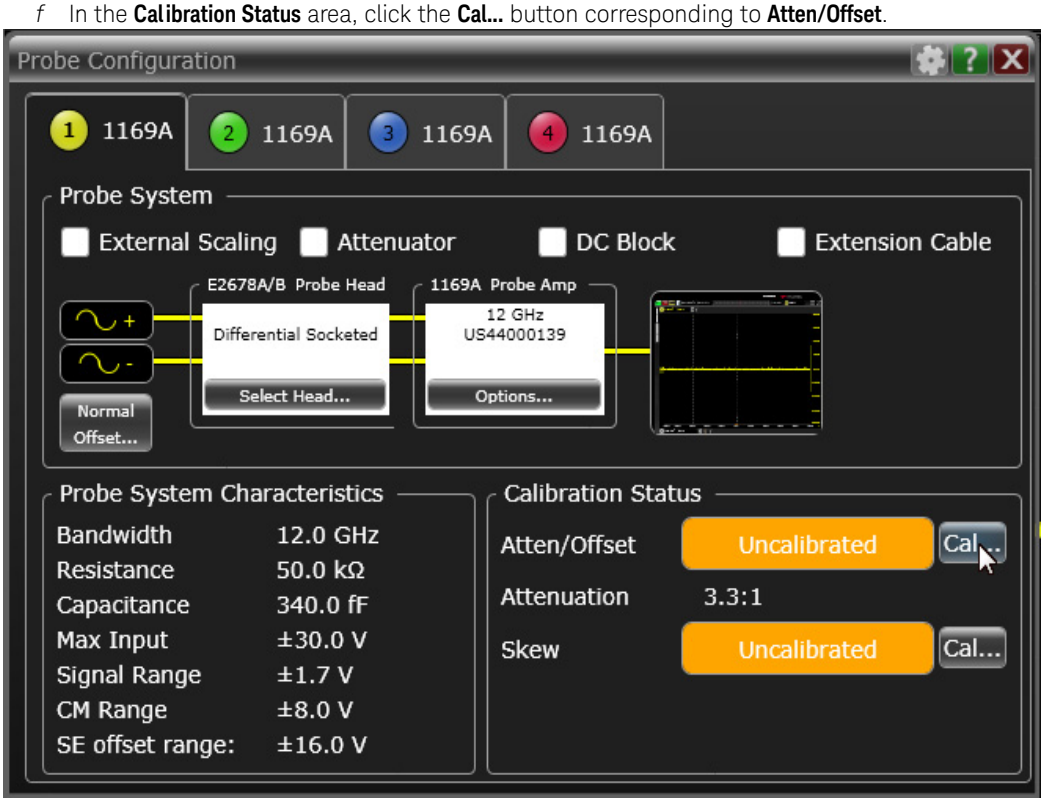
c Click **Probe...**. The **Probe Configuration** dialog displays.



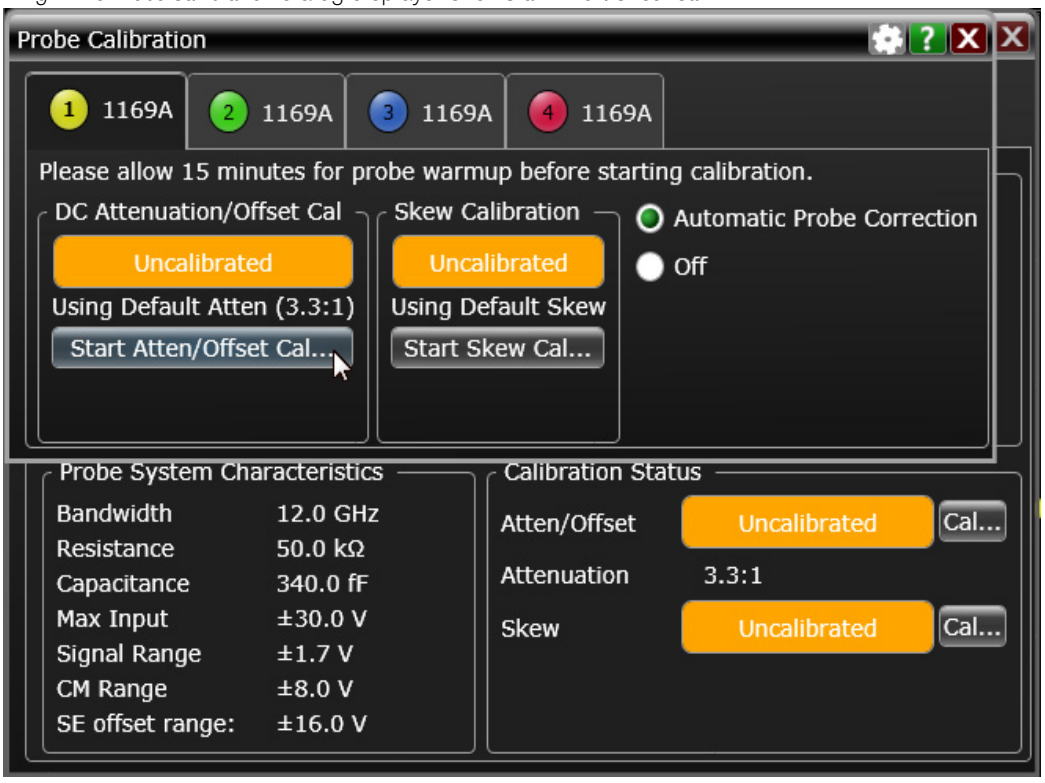
d In the **Probe Head** block, click the **Select Head...** button.

e Select **E2678A/B** from the list.

f In the **Calibration Status** area, click the **Cal...** button corresponding to **Atten/Offset**.



g The **Probe Calibration** dialog displays. Click **Start Atten/Offset Cal...**.



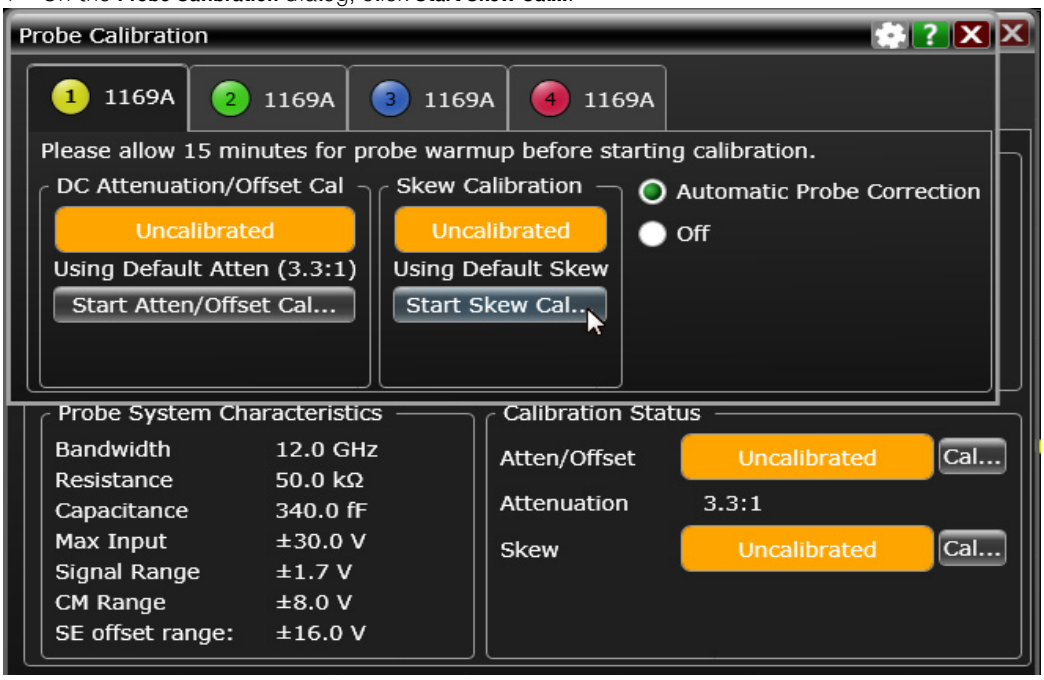
h The Calibration wizard displays. Follow the on-screen instructions. At the end of the Atten/Offset Calibration, perform the Skew Calibration for the Differential Socketed Probe

Head.

Differential Socketed Probe Head Skew Calibration

This procedure ensures that the timing skew errors between channels are minimized. After the Atten/Offset Calibration is done, perform the following steps for skew calibration:

1 On the **Probe Calibration** dialog, click **Start Skew Cal...**.



2 The Calibration wizard displays. Follow the on-screen instructions.

For more information on connecting probes to the Infiniium Oscilloscope, refer to the De-skew and Calibration manual. This manual comes together with the E2655A/B/C Probe De-skew and Performance Verification Kit.

NOTE Each probe is calibrated to the Oscilloscope Channel to which it is connected. Do not switch probes between Channels or other Oscilloscopes, else it becomes necessary to calibrate them again. One of the best practices is to label the probes with the Channel number on which they are calibrated.

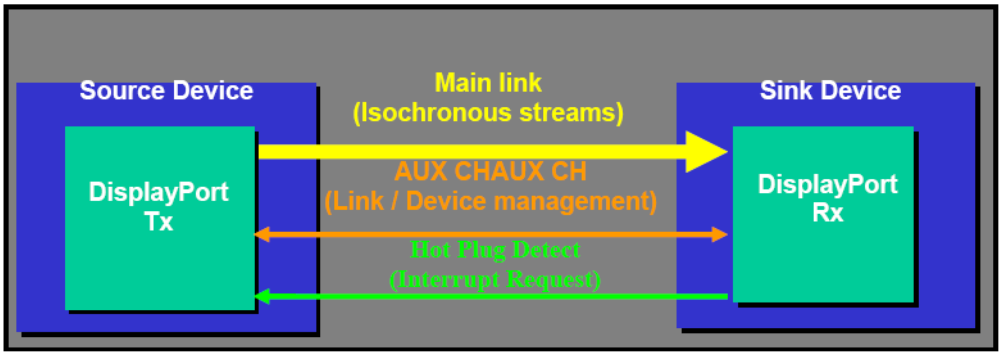
A DisplayPort AUX Channel Cookbook for Tx Automated Test

This section describes what is required to implement the test automation features architected in the *DisplayPort Specification 1.1a*. Automated DisplayPort tests require a source device that is able to change test conditions such as data rate, level, pre-emphasis, test pattern, and SSC options as requested. This cookbook provides a guide on how to perform these tasks using a sink emulator such as Keysight W2642 DPTC controller.

AUX Channel and Hot Plug Detect (HPD)

DisplayPort devices communicate with each other through the AUX Channel. The DisplayPort port sink device provides memory that a source and a sink could read from or write to. The *DisplayPort Specification 1.1a* has reserved a set of DCPD registers for the purpose of test automation.

There is also a HPD line between a source and a sink. For automation purposes, the HPD pulse is used as an IRQ to notify the source about an automated test request.



DPTC Controller

The Keysight DPTC Controller can be used as a sink emulator that tells the source to output desired signals. Some fundamental functions provided which enable automation are:

- SetByte(Address, Value)
- Send HPDPulse(Length)
- PlugIn(Emulate Plug in event)
- PlugOut(Emulate Plug out event)

NOTE Function names listed are for informative purpose only. They are not reflected to actual API call.

Automated Test Sequence

This section provides information on how to enable test automation in DisplayPort Transmitter test. **You should specify the Max link rate, lane count, preEmphasis, Level, and SSC options from the compliance application.**

OPTION 1

Step 1: Emulate successful link training (For SSC)

1 This step emulates an unplug and plug in event to initiate a fake link training.

2 To do this, the DPTC controller initiates the sequence below:

a Emulate PlugOut Event to put HPD line in Low for at least 2 ms. Source should RESET.

b Set Link Capability fields.

MAX_LINK_RATE = 0x0A.

MAX_LANE_COUNT = 0x04.

MAX_DOWNSPREAD = 0x01 to enable SSC / 0x00 to disable SSC.

c Set 0x202 (LANE0_1_STATUS) = 0x77.

d Set 0x203 (LANE2_3_STATUS) = 0x77.

e Set 0x204 (LANE_ALIGN__STATUS_UPDATED) = 0x81.

f Note: 0x202, 0x203 and 0x204 must be preset for automation purposes.

g Emulate PlugIn Event to put HPD line in High.

h Source clears Link Configuration field and reads Link Capability.

i Source enables/disables SSC based on the value of MAX_DOWNSPREAD (Enable SSC if value is 1).

j Source outputs 0x01 to TRAINING_PATTERN_SET.

k Source reads LANE0_1_STATUS, LANE2_3_STATUS and LANE_ALIGN__STATUS_UPDATED. Because these registers are already set in a previous step, the source exits the Clock Recovery Sequence for Link Training (Figure 186) and goes to the Channel Equalizer sequence for Link Training (Figure 187).

l Source set TRAINING_PATTERN_SET to 0x02.

m Source reads LANE0_1_STATUS, LANE2_3_STATUS and LANE_ALIGN__STATUS_UPDATED. Because these registers are already set in a previous step, the source exits the Channel Equalizer Sequence and ends the whole link training process.

3 From the state machine of link training of *Display Port Specification 1.1a*, these sequences cheat a Display Port source into thinking that link training has already been performed without looping through the actual link training. The Display Port Source device should exit link training successfully.

4 The AUX Controller then checks DOWNS_SPREAD_CTRL if SSC support is changed.

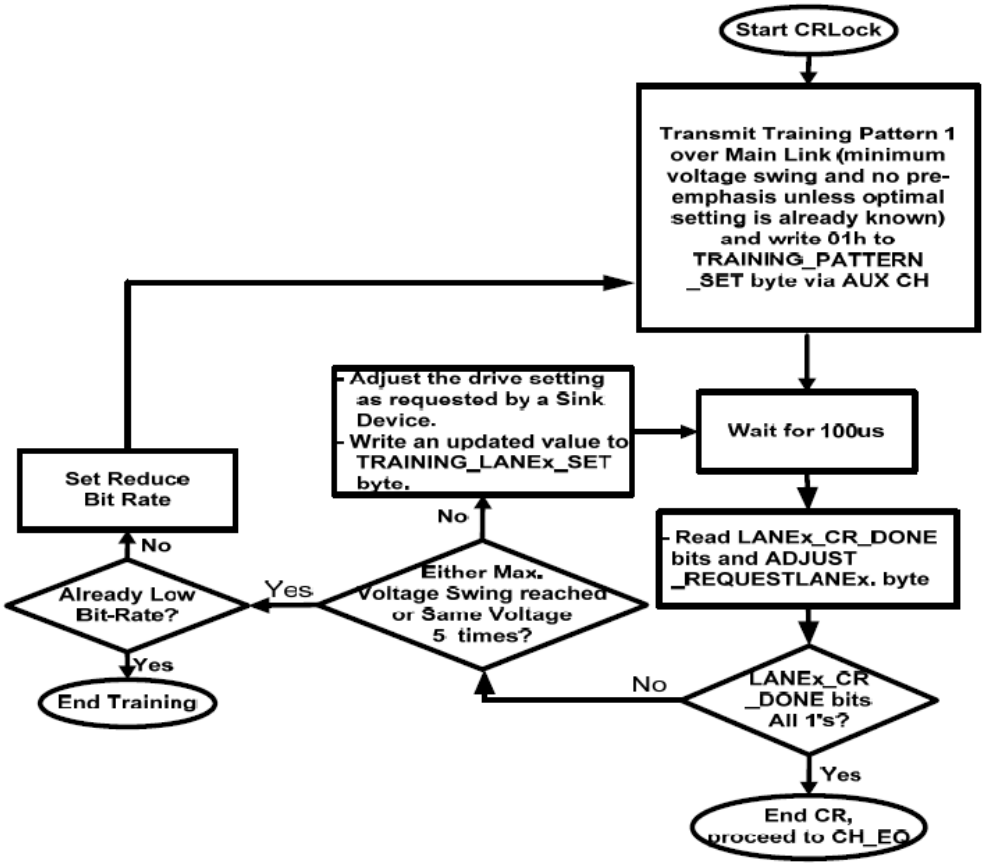


Figure 186 Clock Recovery Sequence

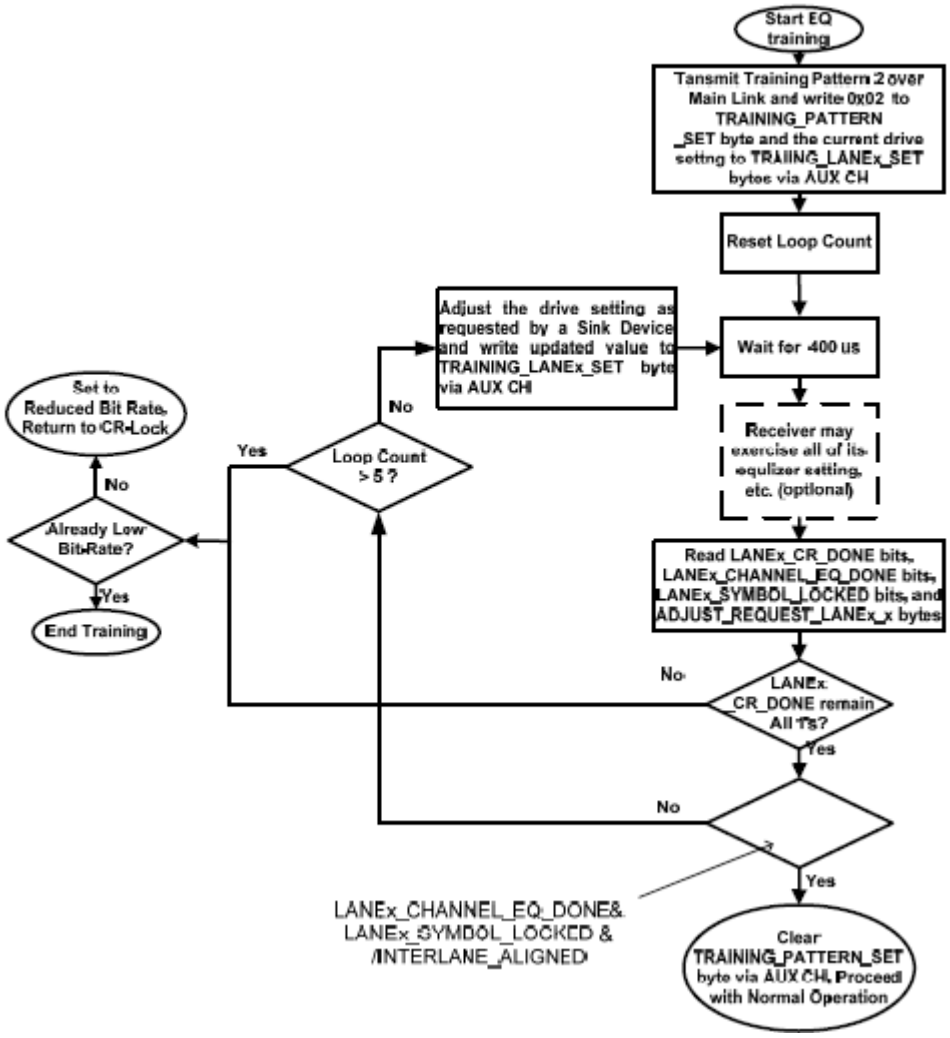


Figure 187 Clock Equalizer Sequence

Step 2: Change Bit Rate and Number of Lanes

1 To change the bit rate and Number of Lanes, the DPTC controller initiates the sequence below:

a Set 0x202 (LANE0_1_STATUS) = 0x77.

b Set 0x203 (LANE2_3_STATUS) = 0x77.

c Set 0x204 (LANE_ALIGN__STATUS_UPDATED) = 0x81.

d SetBit 0x201.1 (AUTOMATED_TEST_REQUEST).

e Clear 0x218 (TEST_REQUEST).

f SetBit 0x218.0 (TEST_LINK_TRAINING).

g SetByte 0x219 (TEST_LINK_RATE) to 0x0A (2.7 Gbps) or 0x06 (1.62 Gbps).

h SetByte 0x220 (TEST_LANE_COUNT) to the desired lane count.

i Trigger an IRQ Event (Send 1 ms HPD Pulse).

2 When a 1 ms HPD pulse is received:
   a Source reads bit 0x201.1 (AUTOMATED_TEST_REQUEST). If 0x201.1 is asserted go to 2.
   b If 0x218.0 is asserted, Source clears LINK_BW_SET and LANE_COUNT_SET.
   c Source reads 0x219 and 0x220 and output signals with desired lane count and data rate.

Step 3: Change PreEmphasis, Level, and Test pattern

1 To Change PreEmphasis, Level, and Test pattern, the DPTC initiates the following sequences:
   a Set 0x202 (LANE0_1_STATUS) = 0x77.
   b Set 0x203 (LANE2_3_STATUS) = 0x77.
   c Set 0x204 (LANE_ALIGN__STATUS_UPDATED) = 0x81.
   d SetBit 0x201.1 (AUTOMATED_TEST_REQUEST).
   e Set 0x206 (ADJUST_REQUEST_LANE0_1) and 0x207 (ADJUST_REQUEST_LANE2_3) with desired level and preemphasis.

Table 171 Mapping table for PreEmphasis and Level

VOLTAGE_SWING_LANEX (2 bits)	
00:	400 mV
01:	600 mV
10:	800 mV
11:	1200 mV

PREEMPHASIS_SWINT_LANEX (2 bits)	
00:	0 dB
01:	3.5 dB
10:	6 dB
11:	9.5 dB

   f Clear 0x218 and SetBit 0x218.3 (TEST_PATTERN_REQUEST).
   g Set 0x248 (PHY_TEST_PATTERN) to desired pattern.

Bits 1:0 = PHY_TEST_PATTERN_SEL	
00	= No test pattern selected
01	= D10.2 without scrambling
10	= Symbol_Error_Measurement_Count
11	= PRBS7V

   h Send IRQ to source (HPD 1 ms Pulse).

2 When a 1 ms HPD pulse is received:
   a Source reads bit 0x201.1 (AUTOMATED_TEST_REQUEST). If 0x201.1 is asserted, go to step 2.
   b Source reads 0x248, 0x206, 0x207 and outputs signals with desired pattern, PreEmphasis, and Level.

NOTE It might be necessary to repeat step 3 to set TEST_PATTERN back to “No pattern” (0x248=0h) before repeating whole automation sequence (step 1 to 3).

OPTION 2

This option provides a simple way to control test automation in one simple step, providing that a test mode is supplied. However, it is less consistent with DisplayPort Automation scheme.

Step 1:

1 Source should always Scan for 0x201.1 (AUTOMATED_TEST_REQUEST).
2 Sink sets the following:
   a SetByte 0x219 (TEST_LINK_RATE) to (2.7 Gbps) or 0x06 (1.62 Gbps)
   b SetBit 0x03.1 (TEST_DOWNSPREAD) to turn on SSC. Clear 0x21A.1 to turn off SSC.
   c SetByte 0x220 (TEST_LANE_COUNT) to desired lane count.
   d Set 0x206 (ADJUST_REQUEST_LANE0_1) and 0x207 (ADJUST_REQUEST_LANE2_3) with desired level and preemphasis.
   e Set 0x248 (PHY_TEST_PATTERN) to desired pattern.
3 Sink sets 0x201.1.
4 When the Source detects 0x201.1 being set, it should respond by outputting signals as in step 2.
5 Sink wait for 3 seconds.
6 Sink set bit 0x218.0 back to 0.
7 Alternatively, HPD_IRQ (1 ms) mechanism could be used instead of keep scanning 0x201.1.

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